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AN EVALUATION OF THE VOLTAGE-CURRENT RATING CHARACTERISTICS OF MINIATURE MONOLITHIC RF CERAMIC CAPACITORS

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This paper reviews the establishment of RF voltage and current rating characteristics of monolithic ceramic capacitors, using thermal balance considerations between heating of the component due to dielectric losses and heat transport through conduction by the electrodes.

Maximum thermal voltages and currents, characteristic of the electric and thermal conductivities of the dielectric material, were calculated on the basis of dielectric loss-frequency characteristics determined experimentally for test devices resembling in their design those of miniature RF power capacitors, and UHF/microwave porcelain chip capacitors for applications in strip line circuits.

Maximum rated RF voltages for the specific components were evaluated by consideration of the elements of dielectric strength and breakdown properties.

By the establishment of the maximum internal temperatures developed within the dielectric upon the application of RF voltages which are permissible for reliable operation of the component, the RF voltage and current rating characteristics may be designated in terms of characteristic limiting impedances determining regions of the characteristics where limitations by the maximum rated voltage, power, or current obtain.

Relations between rating characteristics and component design are briefly reviewed.

1. INTRODUCTION

The development of monolithic ceramic capacitors resulted from advances made, independently, by the ceramics and thick film electronics technologies.

The contribution of ceramic technology is summed up as follows:

a) The recognition, and understanding of the basic crystallographic and physical mechanisms leading to the low dielectric losses in a number of alkaline-earth titanate compounds in the radio and microwave frequency regions.[1,2]

b) Development of temperature compensating ceramic dielectric mixtures, by the addition of transition and/or rare-earth metal oxides to the basic alkaline-earth titanates. These additions lead to the enhancement or suppression of certain dielectric characteristics; to the establishment of compositions with suitable sintering characteristics for non porous, impervious compounds; and to the construction of capacitors with controlled temperature coefficients of capacitance.[3,4]

c) The development of techniques for the casting and processing of "green" ceramic laminates, resulting in dielectrics with thicknesses of the order of 0.015 mm to 0.15 mm (~ 0.0006 in. to 0.006 in.) in the fired capacitors.[5,6]

Developments of conductive inks for thick film circuits resulted in the availability of a wide variety of electrode metal and end-termination compositions with characteristics of adhesion, sintering, and solderability compatible with most commercially used ceramic dielectrics and hybrid or printed circuit substrate material.

The facility of increased heat dissipation, arising from the laminar, multilayer construction of monolithic ceramic capacitors, enables the attainment of high RF power rating in relatively small component volumes.

The establishment of voltage-current rating characteristics for miniature RF power capacitors is reviewed in this paper. Limiting factors of maximum current and voltage ratings are evaluated which are inherent in the physical characteristics of the ceramic dielectric, and in the design of the capacitor.

Maximum current limitations are considered in terms of heat balance between the thermal input due to dielectric losses, and heat transport through conduction by the electrodes.

Maximum voltage limitations are evaluated by a review of the elements of dielectric strength and breakdown properties.

2. DESIGN FEATURES OF THE CAPACITORS

Test devices were constructed in our laboratory, whose dielectric loss characteristics were measured, and upon which the evaluation of rating characteristics will be applied. The following is a description of the test devices.

The test devices were monolithic ceramic capacitors, with the following two sets of typical measurements for the self-encapsulated ceramic chips: a) 12.3 mm (0.484 in.) length x 11.5 mm (0.452 in.) width x 2.5 mm (0.098 in.) thickness; and b) length = width = 3.0 mm (0.118 in.) x 2.54 mm (0.1 in.) thickness.

The ceramic dielectric is a proprietary low loss temperature compensating material, yielding effective characteristics in the capacitor as follows: relative permittivity K = 15 with a temperature coefficient of +100 ppm/°C (P 100). No changes of the relative permittivity were found over the frequency range of evaluation of rating characteristics. The monolithic capacitor consists of inert metal-dielectric-inert metal "active layers" fused together into an impervious solid unit.

The inert metal electrode was of platinum or palladium, with the thickness of the electrode layer being approximately 7 μm. The inner electrode pattern of subsequent layers extend to opposite edges of the capacitor chip. Typical effective electrode area of the "active layers" is 80 mm^2 (0.124 in^2) and 5 mm^2 (0.008 in^2) for types a) and b) test devices respectively. The electrode overlap was taken into account in the above measurements.

The active layer incorporates the minimum dielectric thickness of one ceramic laminate. In practice, the dielectric thickness of an active layer is determined by the dielectric strength of a particular dielectric, and by the test and operating voltages required of a particular capacitor. With d.c. test voltage V_{test} and ceramic dielectric strength F_{br}, the dielectric thickness h of an active layer is:

$$h = m \frac{V_{test}}{F_{br}} \qquad (1)$$

where $m > 1$. Typically $m \cong 1.5$ to 2. The d.c. dielectric strength of the ceramic was found to be as $F_{br} = 4 \times 10^5$ $V.cm^{-1}$.

Typical minimum dielectric thicknesses of the active layers were 0.254 mm (0.010 in) and 0.020 mm (0.00079 in) for types a) and b) devices respectively. The thickness and lateral measurements of the test devices were selected as such, so as to permit the evaluation of the effect of device design upon the rating characteristics; and to reflect the approximate orders of magnitude of miniature RF power capacitors in type a), and those of UHF/microwave capacitors designed for mounting onto striplines in type b). A further consideration in the selection of dielectric thickness was to obtain the same values of capacitance (41.8 pF) for the active layer unit for both size devices.

The capacitors are contacted by means of metallized end terminations on two opposing edges, by soldering, conductive epoxy cementing, thermocompression bonding; or by silver ribbon or wire leads attached to the metallized edges.

Typical Q-factor versus frequency characteristics found in both of the above types of test devices are shown in Figures 1a and 1b.

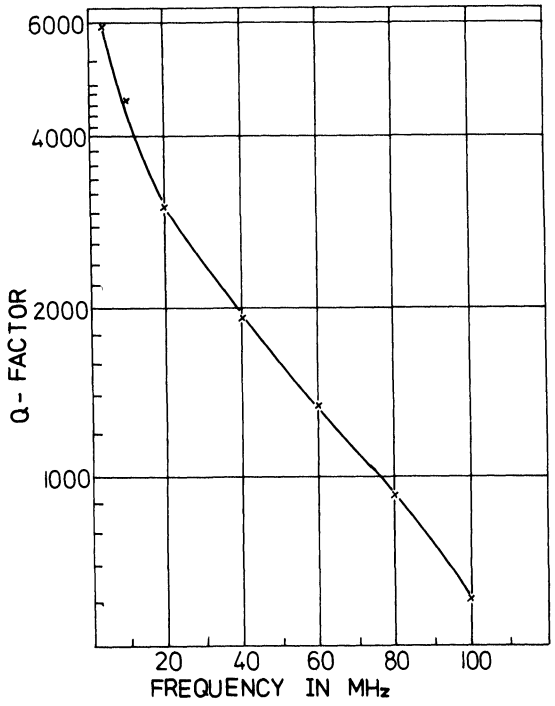

FIGURE 1a Quality-factor vs. frequency characteristics of monolithic ceramic capacitor test devices.

Type a) device. Capacitance: 41.8 pF. Measurements of chip: Length: 12.3 mm (0.484 in), Width: 11.5 mm (0.452 in), Thickness: 2.5 mm (0.098 in) (Typical).

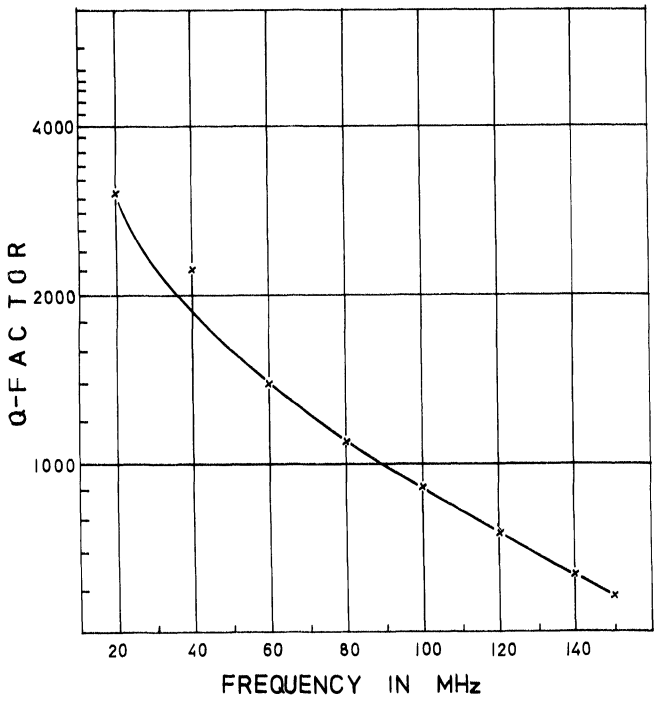

FIGURE 1b Quality-factor vs. frequency characteristics of monolithic ceramic capacitor test devices.
Type b) device. Capacitance: 41.8 pF. Measurements of chip: Length = Width: 3.0 mm (0.118 in), Thickness: 2.54 mm (0.100 in) (Typical).

3. THERMAL CONSIDERATIONS

In considerations of thermal equilibrium, a discussion parallel to that used in considerations of thermal dielectric strength may be used, as outlined by Klein and O'Dwyer.[7,8] The fundamental difference is in the criterion of end point.

Studies of thermal breakdown or thermal dielectric strength seek to establish conditions for the onset of thermal instability in the dielectric, or for the occurrence of breakdown, where short circuiting of the capacitor is accompanied by localized or bulk melting, evaporation or chemical decomposition of the dielectric, and physical damage of the electrode. Thermal considerations in an evaluation of voltage and current rating seek to establish conditions of thermal equilibrium, where long term reliable operation of a component is possible with maximum voltage, current, or power applied, without any change in the chemical or physical characteristics.

The generalized equation for conduction of heat between the capacitor and surrounding solid medium is:

$$c\frac{\partial T}{\partial t} = \text{div}(K \text{ grad } T) + P_{\text{input}} \tag{2}$$

where T denotes temperature, t time, c specific heat per unit volume, K thermal conductivity, and P_{input} the input of heat into the capacitor.

The term P_{input} represents power input due to dielectric losses and Joule heat, with the former being most significant in this case. Generally, the thermal conductivity K is a function of parameters such as temperature, i.e. $K = K(T)$.

The solution of Eq. (2) yields temperature as a function of time t and position r. $T = T(t, r)$.

An evaluation of heat input is readily available from the loss characteristics of the capacitors, but for an assessment of heat transport, a number of assumptions have to be made.

Considering the description of typical test devices in the previous section, with lateral measurements (length and width) of the capacitor active layer being at least one or two orders of magnitude larger than the thicknesses, the idealization involved in a model of a dielectric specimen bounded by two parallel infinite planes may be used in the discussion of thermal behaviour.

Such specimens are characterized by their external and internal thermal resistances, R_{te} and R_{ti} respectively. R_{te} is the resistance to heat flow per unit area to an external heat sink and R_{ti} is the resistance to heat flow per unit area between two opposite specimen surfaces.

Two extreme situations may arise. These are: $R_{ti} \gg R_{te}$, exemplified by a thick insulation with well cooled surfaces and $R_{ti} \ll R_{te}$, common with thin film and semiconducting specimens. In the case of $R_{ti} \gg R_{te}$, the dielectric is heated by heat input caused by dielectric losses. Due to the low thermal conductance of the dielectric, a temperature difference is established between the centre of the insulator and the electrodes covering the surfaces of the dielectric. In the case of $R_{ti} \ll R_{te}$, the electrodes reach the same temperature as the dielectric layer.

The physical reality of a dielectric active layer with a thickness of the order of 250 μm is far from that of a thin film specimen. In certain designs however, e.g. for capacitors intended for high current and relatively low voltage ratings, for pulse application; or in capacitors constructed by the deposition of dielectric inks by screen printing, or in the "glaze" capacitors referred to by Coffeen,[9] a situation of $R_{ti} \ll R_{te}$ may be approached.

With thermal conductivities of 8.1×10^{-3} $Wcm^{-1}K^{-1}$ and 7.3×10^{-1} $Wcm^{-1}K^{-1}$ at 300 K for a typical ceramic dielectric material such as titanium dioxide and platinum respectively, values of R_{ti} are 2.78 $KW^{-1}cm^{-1}$ for the unit area of type a), and 54.89 $KW^{-1}cm^{-1}$ for the unit area of type b) ceramic chip respectively. With the external thermal resistances of 8.48×10^{-4} $KW^{-1}cm^{-1}$ and 2.1×10^{-1} $KW^{-1}cm^{-1}$ for unit areas of types a) and b) ceramic chips, the ratios of R_{ti}/R_{te} are 3.3×10^{3} and 2.61×10^{2} for two types of devices respectively.

It is of some interest to proceed at first with a discussion for the situation $R_{ti} \gg R_{te}$.

3.1 *Discussion of the Situation* $R_{ti} \gg R_{te}$

Assuming current continuity in the specimen, substitute the following relationship in Eq. (2).

$$\operatorname{div}(\sigma F) = 0 \tag{3}$$

where σ is the electric conductivity, and F the electric field. Integration of Eq. (3) gives:

$$-j = \frac{d\Phi}{dz} \tag{4}$$

where j is the current density, Φ is the electric potential and z the thickness coordinate. Assuming in Eq. (2) that $P_{\text{input}} = \sigma F^2$ and substituting for σF gives:

$$\frac{\partial}{\partial z}\left(K\frac{\partial T}{\partial z}\right) - j\frac{\partial \Phi}{\partial z} = 0 \tag{5}$$

At the central plane of the insulator $z = 0$, $T = T_1$, $\dfrac{\partial T}{\partial z} = 0$ and $\Phi = 0$.

Integrating Eq. (5) from $z = 0$ to an arbitrary plane in the specimen gives:

$$j = K\frac{\partial T}{\partial z} \tag{6}$$

Substituting for j from Eq. (4) and integrating from $\Phi = 0$ and $T = T_1$ at the central plane, to $\Phi = V/2$ and $T = T_2$ at the upper electrode gives:

$$V^2 = 8\int_{T_2}^{T_1}\frac{K}{\sigma}dT \tag{7}$$

where V is the voltage across the specimen.

Calculation of the maximum permissible voltage, or critical voltage can be made, by replacing T_1 with the maximum operating temperature, or with a temperature of phase transformation (e.g. melting point, or a critical temperature of the viscosity-temperature characteristics of glass dielectrics) of the dielectric. The current may be calculated from the above maximum voltage and impedance.

The relationship of Eq. (7) for the calculation of voltage across the dielectric, defines the difference in temperature between the central plane in the dielectric and the electrode flanking the dielectric as a function of material characteristics, such as electrical and thermal conductivities. Unlike the thermal resistances defined above, the voltage applied across the dielectric to establish certain temperature difference appears to be independent of the dielectric thickness and of the lateral measurements of the device. The voltage calculated from Eq. (7) is defined as the maximum thermal voltage by certain authors.[7]

The electric conductivity of the ceramic dielectric as a function of temperature, $\sigma = \sigma(T)$ is given by Von Hippel and Klein[1,7] as:

$$\sigma = A\exp\left(-\frac{E}{kT}\right) \tag{8}$$

where k is Boltzmann's constant = 8.619×10^{5} $eV.K^{-1}$ and E is the thermal activation energy of conduction. For titanium dioxide ceramic dielectric $E \cong 0.51$ eV[1]. Constant A denotes the conductivity when $kT = E$, which can be determined from the intercept of the plot of $\log \sigma$ versus $1/T$ or from the dielectric loss characteristics.

The thermal conductivity of the dielectric may be assumed to be quasilinear function of temperature over the temperature range of interest (25°C to 125°C). For titanium dioxide, $K \cong 8.075 \times 10^{-3}$ $Wcm^{-1}K^{-1}$ at 37.8°C, with a temperature coefficient of −1930 ppm/K between the temperatures of 37.8°C and 148.9°C. For an evaluation of the applied voltage according to Eq. (7), the value of the thermal conductivity will be assumed to be constant.

Assuming that:

$$K(T) = K \tag{9}$$

over the temperature range of interest, the applied voltage according to Eq. (7) will be:

$$V^2 = 8\int_{T_2}^{T_1}\frac{K}{\sigma}dT = \frac{8K}{A}\int_{T_2}^{T_1}\frac{1}{\exp\left(-\dfrac{E}{kT}\right)}dT$$

$$= \frac{8K}{A} \int_{T_2}^{T_1} \exp\left(\frac{E}{kT}\right) dT \tag{10}$$

Using now the substitution:

$$v = \frac{1}{T}\ ; \text{and } dT = -T^2 dv = -\frac{dv}{v^2} \tag{11}$$

the integral of Eq. (10) will be converted to:

$$V^2 = -\frac{8K}{A} \int_{v_2}^{v_1} v^{-2} \exp\left(\frac{E}{k} v\right) dv \tag{12}$$

From standard tables of integrals:[10]

$$V^2 = -\frac{8K}{A} \left[-\frac{\exp\left(\frac{E}{k} v\right)}{v} + \frac{E}{k} \int \frac{\exp \frac{E}{k} v}{v} dv \right]_{v_2}^{v_1} \tag{13}$$

With

$$\int \frac{\exp\left(\frac{E}{k} v\right)}{v} dv = \log v + \frac{E}{k_3} \frac{v}{1!} + \left(\frac{E}{k}\right)^2 \frac{v^2}{2.2!} + \left(\frac{E}{k}\right) \frac{v^3}{3.3!} + \ldots \tag{14}$$

$$V^2 = -\frac{8K}{A} \left[-\frac{\exp\left(\frac{E}{k} v\right)}{v} + \frac{E}{k} \left\{ \log v + \frac{E}{k} \frac{v}{1!} + \left(\frac{E}{k}\right)^2 \frac{v^2}{2.2!} + \left(\frac{E}{k}\right)^3 \frac{v^3}{3.3!} + \ldots \right\} \right]_{v_2}^{v_1} \tag{15}$$

In the above analysis, an equal temperature, T_2, is assumed both at the upper and lower electrodes of the capacitor. This appears to adequately describe the thermal conditions for an active layer situated within a multilayer capacitor, particularly if maximum current rating is sought to be established to yield very low temperature differences (i.e. between zero and few tenths of deg. Celsius) between the central plane and the electrodes bounding the dielectric.

Different thermal conditions on the two electrode surfaces may be obtained as a consequence of an exposed upper electrode, or an upper electrode close to or in direct contact with the encapsulation and lower electrode mounted against a substrate. The different thermal conditions may give rise to asymmetric external thermal resistances, $R_{te1} \neq R_{te2}$, for the device, leading to different temperatures, T_2 and T_3 at the upper and lower electrode surfaces.

It is essential to note that with the basic assumption of the analysis being $R_{ti} \gg R_{te}$, the maximum thermal voltage yielded by Eq. (7) is dependent only upon the thermal conductivity of the dielectric and not upon that of the medium surrounding the electrodes. With the thermal conductivity of 0.40 $\mathrm{Wcm^{-1}K^{-1}}$ for 99.9% aluminium oxide content pure alumina ceramic used typically in substrate plates, a factor of 50 is obtained relative to the thermal conductivity of titanium dioxide, rendering the above assumption of the analysis feasible. With the tendency of further developments, substrate materials of single crystal synthetic sapphire and beryllia are gaining use, with thermal conductivities of 0.42 $\mathrm{Wcm^{-1}K^{-1}}$ and 2.0 $\mathrm{Wcm^{-1}K^{-1}}$ respectively, further enhancing the ratio R_{ti}/R_{te}. For the thermal conditions of $R_{ti} \cong R_{te}$ there is no closed solution of Eq. (2) available for the calculation of the maximum thermal voltage.[7]

3.1.1 *Evaluation of voltage–current characteristics*

As a first step in a numerical evaluation, the temperature difference between the central plane of the dielectric and the electrode will be considered.

Values of the constant A in the relation of $\sigma(T)$ of Eq. (8) may be evaluated from the typical Q-factor versus frequency characteristics of the capacitors shown in Figures 1a and 1b. The capacitance of an active layer of the dielectric thickness of 0.254 mm (0.010 in) in the type a) device, and of an active layer of the dielectric thickness of 0.020 mm (0.00079 in) in the type b) device will be 41.8 pF.

With the parallel equivalent reactance of:

$$X_p = \frac{R_p}{Q} = R_p \tan \delta \tag{16}$$

$$\frac{1}{R_p} \equiv G = \frac{1}{X_p} \tan \delta = \omega C \tan \delta \tag{17}$$

where X_p and R_p are the parallel equivalent reactance and resistance of the capacitor, $X_p = 1/\omega C$, $G(\mathrm{ohm^{-1}}) = 1/R_p$ is the conductance of the capaci-

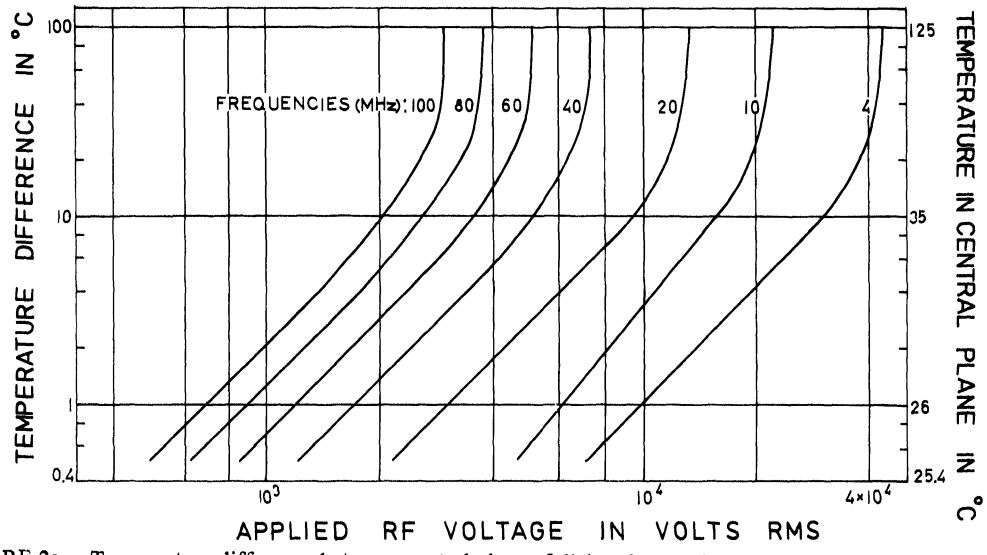

FIGURE 2a Temperature difference between central plane of dielectric and electrode as a function of RF voltage applied to the active layer of monolithic ceramic capacitor.
Type a) device. Dielectric thickness: 0.254 mm (0.010 in), Capacitance: 41.8 pF.

tor, Q and tan δ are the quality and dissipation factors of the capacitor, with $Q = 1/\tan\delta$.

Conductivity may be calculated, by multiplying the value of conductance with a geometrical factor, that is:

$$\sigma = \frac{l}{s} G = A \exp\left(-\frac{E}{kT}\right) \tag{18}$$

and

$$A = \frac{l}{s} G \exp\left(\frac{E}{kT}\right) \equiv \frac{l}{s} \omega C \tan\delta \exp\left(\frac{E}{kT}\right) \tag{19}$$

where l is the length and s the cross section for the current flow. The geometrical factors are thus 3.18 x $10^{-2}\,cm^{-1}$ and 4 x $10^{-2}\,cm^{-1}$ for the type a) and b) test devices respectively.

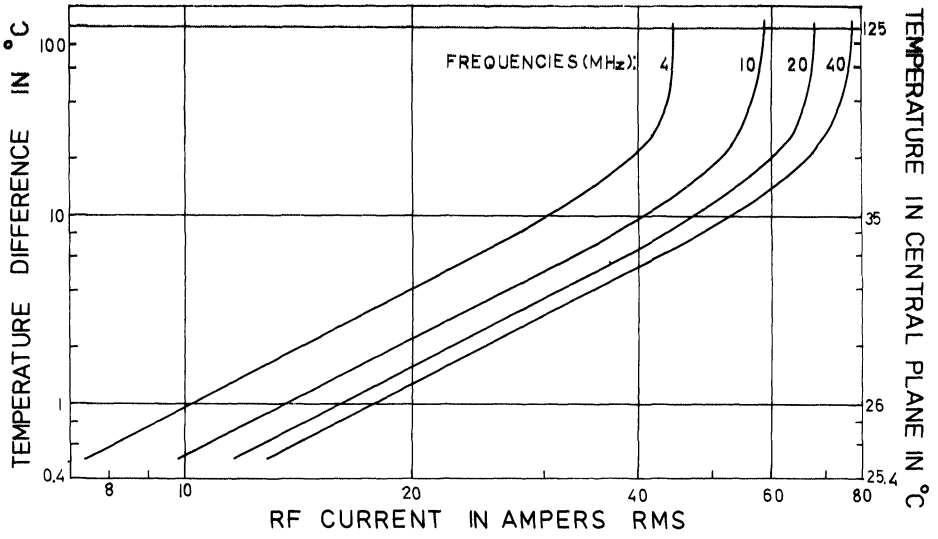

FIGURE 2b Temperature difference between central plane of dielectric and electrode as a function of RF current through active layer of monolithic ceramic capacitor.
Type a) device. Dielectric thickness: 0.254 mm (0.010 in), Capacitance: 41.8 pF.

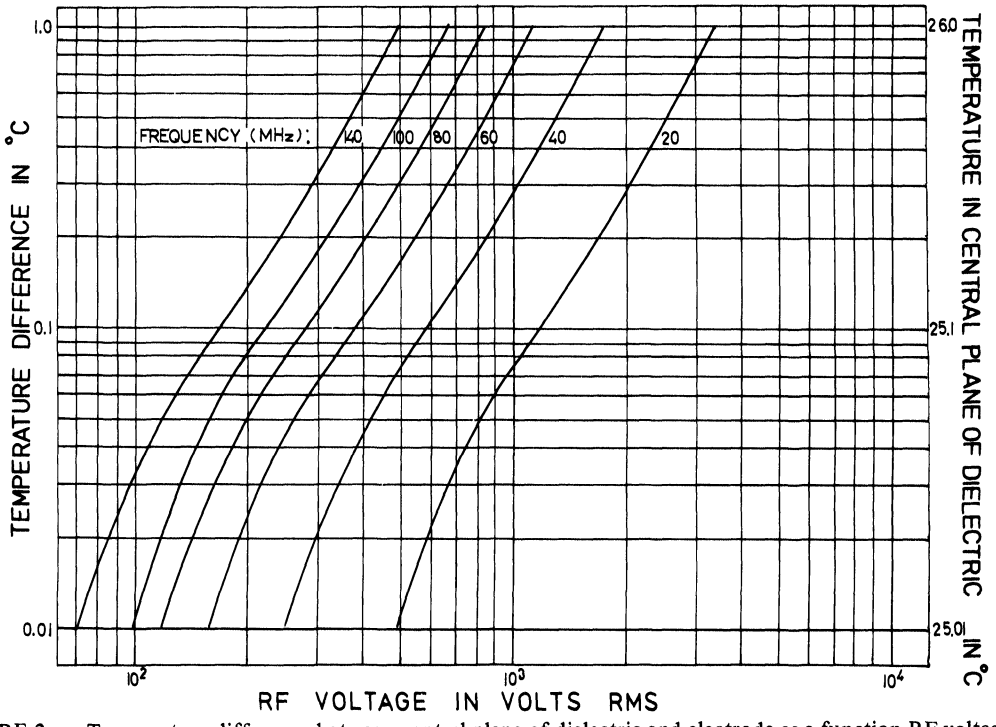

FIGURE 2c Temperature difference between central plane of dielectric and electrode as a function RF voltage applied to the active layer of monolithic ceramic capacitor.
Type b) device. Dielectric thickness: 0.02 mm (0.00079 in), Capacitance: 41.8 pF.

The applied RF voltage for a particular temperature difference between the central plane of the dielectric and the electrode depends only to a very small extent upon the geometrical measurements of the component, but provides a very distinct characteristic of the ceramic dielectric material.

Temperature difference as a function of the applied RF voltage and current are shown in Figures 2a and 2b respectively, with the frequency as a parameter. Conductivity was calculated according to the data of the type a) devices. Temperature difference versus applied RF voltage characteristics with conductivity calculated using data of type b) samples is shown in Figure 2c.

The RF voltage-temperature difference characteristics show that thermal runaway is obtained upon the application of a certain voltage. Thus, a further slight increase of voltage beyond a critical value, causes a very rapid rise of temperature in the central plane of the dielectric. The onset of thermal runaway is not identical to breakdown, as it only reflects conditions in a localized central plane of the dielectric. It is a clear indication however of thermal instability in the capacitor. Conditions for the onset of thermal runaway are shown in Figure 3, where the maximum thermal voltage and current are plotted as functions of frequency. The maximum thermal voltage, that is the applied RF voltage for the onset of thermal runaway is an approximately linearly decreasing function of the frequency, while the RF current approaches a maximum value with the increase of frequency.

For purposes of establishemnt of rating characteristics, the situation of minimum heat development in the centre of the dielectric has to be considered. RF voltage and RF current as a function of frequency were calculated for active layers of 41.8 *pF* capacitance and typical measurements of type a) and b) test samples, for temperature differences of 0.5°C and 0.1°C between the central plane of the dielectric and the electrode. The resulting characteristics for type a) samples and 0.5°C temperature difference are shown in Figure 4a; and for type b) samples and 0.1°C temperature difference in Figure 4b.

For the establishment of rating characteristics, the results shown in Figures 4a and 4b have to be evaluated with respect to the dielectric thicknesses of the respective devices; and the significance of the limits set for the temperature differences have to be discussed. Evaluation of the effects of specimen

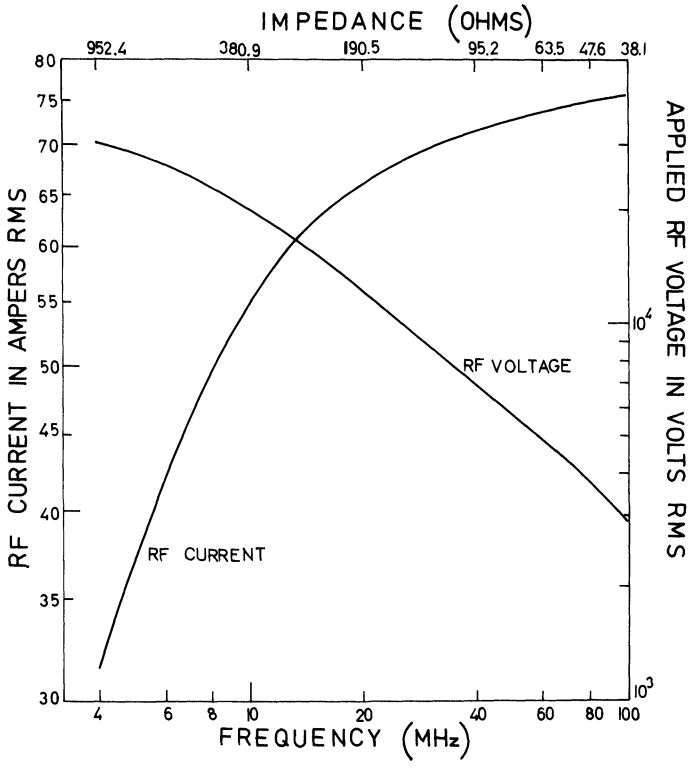

FIGURE 3 RF current and voltage vs. frequency characteristics of monolithic ceramic capacitor active layer, upon the onset of thermal runaway in the temperature difference between central plane of the dielectric and electrode.
Type a) device. Dielectric thickness: 0.254 mm (0.010 in), Capacitance: 41.8 pF.

thickness is made by considerations of the dielectric strength.

The d.c. dielectric strength of the ceramic material in devices of the types described in Section 2 were found to be $4 \times 10^5 \mathrm{Vcm}^{-1}$, in a large number of tests, with excellent reproducibility. Further tests were performed upon the samples with the application of a 1.5 MHz frequency, continuous high voltage signal. The results of these tests showed that a relationship of $F_{br}(1.5\ \mathrm{MHz}) = (\sqrt{2}F_{br}(\mathrm{d.c.})$ applied between the peak values of the electric field at 1.5 MHz frequency $F_{br}(1.5\ \mathrm{MHz})$ and at d.c. $F_{br}(\mathrm{d.c.})$. Consequently, the above dielectric strength establishes a maximum value for the applied peak voltage as $V_{\max} = m'\sqrt{2}V_{br}(\mathrm{d.c.})$ or for the RMS values of the maximum rated voltage as $V_{\max} = m'V_{br}(\mathrm{d.c.})$ where $m'<1$, usually of the order of 0.7 to 0.8, which is a safety factor and a correction factor, to compensate for the linear decrease of maximum thermal voltage with the increase of frequency, as shown in Figure 3.

The impedance in the RF voltage characteristics of Figures 4a and 4b for the maximum rated voltage $V_{\max}$ defines a voltage limiting impedance, Z_{VL}. For frequencies, where $Z \geqslant Z_{VL}$, the maximum rated RF voltage and current are:

$$V = V_{\max} \tag{20}$$

$$I = \frac{V_{\max}}{Z} \tag{21}$$

The RF current characteristics of Figures 4a and 4b show, that for impedances below the value of a characteristics limiting impedance Z_{CL}, a maximum near constant current level is obtained. Defining this impedance as maximum current limiting impedance, Z_{CL}, for frequencies, where $Z \leqslant Z_{CL}$, the maximum rated RF current and voltage are:

$$I = I_{\max} \tag{22}$$

$$V = ZI_{\max} \tag{23}$$

For values of impedances between the above defined characteristics limiting impedances Z_{VL} and Z_{CL}:

$$Z_{VL} > Z > Z_{CL} \tag{24}$$

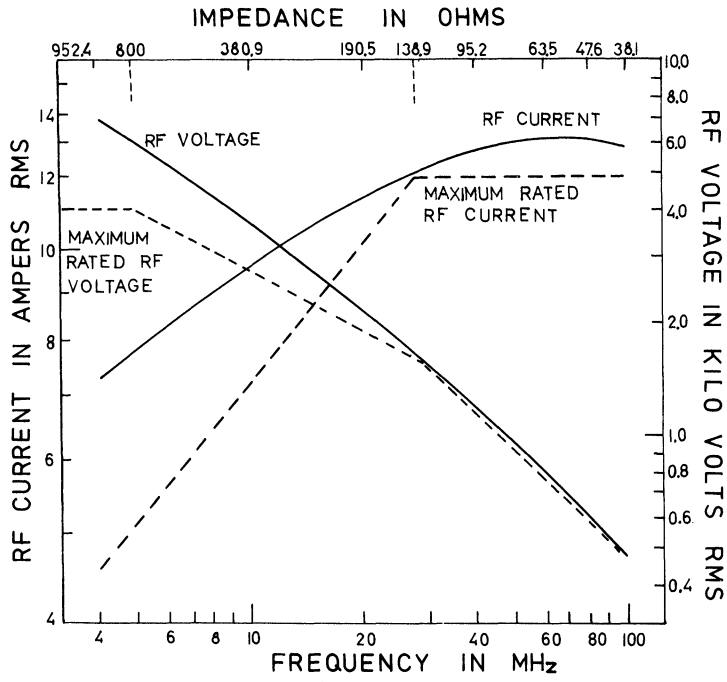

FIGURE 4a RF current and voltage characteristics of monolithic ceramic capacitor active layer, when temperature difference between central plane and electrode is $\Delta T = 0.5°$ C.

Type a) device. Dielectric thickness: 0.254 mm (0.010 in), Capacitance: 41.8 pF. Maximum voltage limiting impedance: 800 ohm, Maximum current limiting impedance: 138.9 ohm.

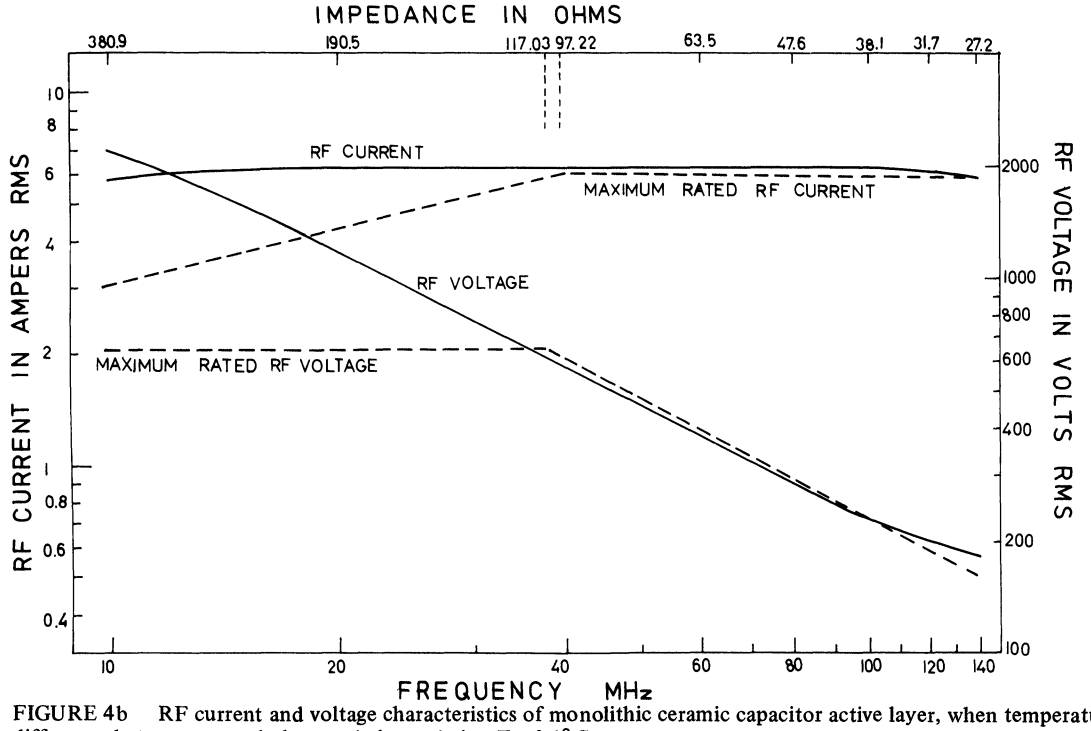

FIGURE 4b RF current and voltage characteristics of monolithic ceramic capacitor active layer, when temperature difference between central plane and electrode is $\Delta T = 0.1°$ C.

Type b) device. Dielectric thickness: 0.02 mm (0.00079 in), Capacitance: 41.8 pF. Maximum voltage limiting impedance: 117.03 ohm, Maximum current limiting impedance: 97.22 ohm.

A third region is distinguished in the voltage and current rating characteristics, the maximum power limit region, where the maximum rated RF current and voltage is limited by the power or KVAR rating of the capacitor. The maximum power rating of the capacitor P_{max} is established on the basis of thermal balance considerations between heat input due to dielectric losses, and heat dissipation by means of conduction by the electrodes. These considerations will be further discussed in Section 3.2. Having established the value of the maximum power rating P_{max}, the limiting impedances are assessed as:

$$\frac{V_{max}^2}{Z_{VL}} = P_{max} = I_{max}^2 Z_{CL} \tag{25}$$

In the region defined by the impedance values as Eq. (24), the rated RF voltage and current may be calculated using:

$$V = \sqrt{Z_{VL} P_{max}} \tag{26}$$

$$I = \sqrt{\frac{P_{max}}{Z_{CL}}} \tag{27}$$

The following conclusions may be made from inspection of Eq. (25):

a) The magnitude of the values of I_{max} are determined by the material characteristics of the dielectric, such as thermal and electrical conductivities. The influence of geometrical design parameters is affecting the value of I_{max} through the choice of temperature difference between the central plane of the dielectric and the electrode, rendered permissible for purposes of component rating.

b) The magnitude of the values of V_{max}, apart from the dielectric strength of the material, are determined by the dielectric thickness, thus strongly affected by the detail of the component design.

c) Material characteristics affecting the value of maximum power rating P_{max}, are the dielectric loss frequency characteristics; thermal conductances of dielectric and electrode materials.

d) The values of the characteristic limiting impedances Z_{VL} and Z_{CL} are determined by the value of maximum power rating P_{max}.

Rated RF voltage and current characteristics, according to the above considerations are fitted to the calculated RF voltage and current characteristics of the active layers in Figures 4a and 4b. Values of the characteristic limiting impedances are shown in the figures, and the three regions of maximum voltage, power, and current limitations may be clearly distinguished in the characteristics of type a) devices in Figure 4a.

De-rating of the RF voltages and currents for ambient temperatures above 25°C may be calculated from Eq. (15) by substituting the appropriate boundary values for v_2 and v_1, that is:

$$v_1 = \frac{1}{T_{ambient}} \text{ and } v_2 = \frac{1}{T_{ambient} + \Delta T} \tag{28}$$

where ΔT is the temperature difference between the central plane of the dielectric and the electrodes, for which the capacitor rating was calculated.

For the characteristics of Figure 4a with ΔT = 0.5°C, both the RF voltages and currents were found to derate by 0.2%°C^{-1} with the increase of temperature between 25°C and 125°C.

3.2. *Discussion of the Situation* $R_{ti} \ll R_{te}$

With the assumption of identical temperatures in the dielectric and electrode layers, Eq. (2) can be replaced by a relation of heat balance, which is:

$$c_e h \frac{dT}{dt} = -\Phi(T) + hP_{input} \tag{29}$$

where c_e is the effective specific heat, h the thickness of the dielectric, and $\Phi(T)$ is the power lost by heat transport. The effective specific heat is:

$$c_e = \frac{ch + c_m h_m}{h} \tag{30}$$

where c and c_m are the specific heats of the dielectric and electrode metal respectively, while h and h_m are the thicknesses of the dielectric and metal. In view of the fact that $h_m \ll h$ and $c_m \ll c$ (c_m for a typical electrode metal such as platinum is 0.032 gcal.°C^{-1}; and for a typical ceramic dielectric such as titanium dioxide is 0.17 gcal.°C^{-1}), c_e is practically equal to the specific heat of the ceramic dielectric.

In a steady state condition the term $c_e h dT/dt$ on the left hand side vanishes, and the heat loss from the active layer unit, according to Eq. (29), is:

$$\Phi(T) = \gamma \Delta T \tag{31}$$

where $\gamma = 1/R_{te}$ the external steady state thermal conductance of the specimen. Using Eq. (31), in the steady state Eq. (29) gives:

$$\gamma \Delta T = hP_{input} \tag{32}$$

Now for the rating of type a) samples $\Delta T = 0.5°C$ and for type b) devices $\Delta T = 0.1°C$ was used in the previous section. The external thermal conductances for platinum electrodes are: 833.75 $Wcm°K^{-1}$ for type a) and 5.29 $Wcm°K^{-1}$ for type b) test devices. With the above, the heat input is:

$$P_{\text{input}} = \frac{\gamma \Delta T}{h} \tag{33}$$

Consequently the condition for thermal equilibrium is:

$$P_{\text{input}} \leqslant \frac{\gamma \Delta T}{h} \tag{34}$$

The values for $\gamma \Delta T/h$ are 1.70×10^4 W and 2.65×10^2 W for type a) and b) samples respectively.

The power input is the heat dissipated in the dielectric due to losses:

$$P_{\text{input}} = I^2 R_s = I^2 \frac{1}{\omega C} \tan \delta = \omega C V^2 \tan \delta \tag{35}$$

For type a) samples according to the rating characteristics in Figure 4a, the maximum power limited region extends between the characteristic limiting impedances of 800 ohm and 138.9 ohm. The values of RF currents are 5.0 A and 12.0 A RMS corresponding to the above limiting impedances, and the dissipation factors are 1.67×10^{-4} and 4×10^{-4} respectively. Consequently for the maximum power limited region of the RF current-voltage characteristics, the heat input is: $3.34 \text{ W} \leqslant P_{\text{input}} \leqslant 8.0 \text{ W}$.

For the maximum current limited region at the frequency of 100 MHz, with the impedance of 38.095 ohm and $\tan \delta = 1.32 \times 10^{-3}$, the input power is 7.24 W.

For the maximum voltage limited region of the characteristics at the frequency of 4 MHz, with the impedance of 952.4 ohm and dissipation factor of 1.59×10^{-4}, the heat input due to dielectric losses is 2.67 W.

For the type b) test devices, according to the characteristics of Figure 4b, the heat input at 150 MHz in the maximum current limited region with the impedance of 25.4 ohm and $\tan \delta = 1.25 \times 10^{-3}$, is 1.14 W. At the minimum impedance of the maximum power limited region, 97.22 ohm, with $\tan \delta = 4.55 \times 10^{-4}$, the heat input is 1.59 W. At the frequency of 20 MHz in the maximum voltage limited region, with the impedance of 190.5 ohm and $\tan \delta = 2.5 \times 10^{-4}$, the heat input is 5.38×10^{-2} W.

From the above considerations it may be concluded that the heat input due to dielectric losses is smaller than the heat transport capability of the electrode layer, by 4 orders of magnitude in the type a) devices, and by 2 orders of magnitude in the type b) devices, for the conditions of rating set out in the calculations of the characteristics in Figures 4a and 4b.

Maximum thermal voltages calculated by the model of $R_{ti} \ll R_{te}$ are larger than those calculated by the $R_{ti} \gg R_{te}$ model, due to the assumption of the temperature $T_{\text{ambient}} + \Delta T$ prevailing in the entire body of the dielectric.

In the multiple active layer components, the capacitance of the device is the sum of the capacitances of active layers connected in parallel by means of the metallized end terminations on the edges of the ceramic chip. Assuming that the component is constructed of n active layers of equal impedances, the current flowing through each active layer is I/n, where I is the rated current for the component. From the point of view of design, components for high voltage and high current ratings may be distinguished by the dielectric thickness of the active layers. According to Eq. (33), the heat transport is inversely proportional, while the maximum voltage is directly proportional to the dielectric thickness. Experimental tests of thermal effects are frequently made by the users of the components using temperature indicating dyes on the component surface to check the effectiveness of heat sinking in the mounting of components in electronic instruments. Detailed investigation of thermal effects by direct temperature measurements inside the active dielectric are in process in our laboratory.

4. CONCLUSIONS

While ceramic dielectric mixtures with relative permittivities up to 10,000 and temperature coefficients of permittivity from −10,000 through 0 to +10,000 ppm/°C were developed and are being used in ceramic disc capacitors, high relative permittivities were found to be accompanied by high dielectric losses and temperature coefficients in the dielectric materials. For applications at RF frequencies and high voltage, current, or power levels, only dielectrics with high Q and electric strength characteristics can be considered. Capacitors in high power RF vacuum tube circuits are constructed of tubular alumina dielectrics, and heat dissipation is promoted by air cooling. In RF transistor and hybrid integrated circuits, the requirements for high current ratings in the capacitors

are enhanced, together with those of miniaturization. Both these requirements can be met by the use of temperature compensating high Q ceramic dielectrics based on the non ferroelectric alkaline-earth titanates. These ceramics have higher relative permittivities than alumina, and the lower firing temperatures required in their processing allows co-sintering in air with inert metal electrodes into monolithic multilayer structures.

Rating characteristics for the following two sizes of capacitors were reviewed above: A series of miniature RF power capacitors of device a), rated for capacitances of 10 pF to 3000 pF with typical RMS values of 3000 V, 12 kW and 8 A of maximum ratings in the maximum voltage, power and current limited regions of impedances; for lower (10 pF to 150 pF) capacitance values. The capacitors of device b) are a series of monolithic ceramic capacitors designed for mounting onto strip line or hybrid integrated circuits, rated for capacitances of 0.1 pF to 1000 pF. Capacitors of the above two sizes are produced by a number of manufacturers, and components with the characteristics of device b) are covered by military specifications.

Maximum voltage, current and power ratings were evaluated for capacitors with the lateral measurements of the above two devices, but with different dielectric thicknesses in the active layers, to yield identical values of capacitance. The thermal resistance situation of $R_{ti} \gg R_{te}$ for the evaluation of maximum thermal voltage holds for both devices discussed.

For the maintenance of identical values of capacitance, the dielectric thickness in the active layer of device b) is smaller by a factor of 12.7 relative to that in device a), due to the corresponding reduction of the electrode areas in this device. Maximum thermal voltage, calculated for the thermal resistance situation prevailing, is dependent only upon the thermal and electrical conductivities of the dielectric layer and not upon the geometrical size of the capacitor, as shown in Eq (7). Dielectric thickness is considered in the establishment of the values of maximum rated voltage, where the effect of smaller thickness in device b) is fully reflected. Values for the maximum RF current rating are those calculated using Eqs. (15) and (10) and continuity of the rating characteristics obtained is by fitting to the value of maximum power rating according to Eq. (25).

Establishment of a value for the maximum power rating is based upon the maximum loss from the input RF power allowed in the design of a particular circuit application. In the actual component design, the worst case situation can be estimated by the assumption of a uniform elevated temperature, $T_{\text{ambient}} + \Delta T$, prevailing in the entire dielectric, where ΔT is equal to the temperature difference between the central layer in the dielectric and the electrode, for which calculation of the maximum current rating was made in the discussion in Section 3.1. The thermal balance situation in both types a) and b) devices was reviewed in Section 3.2, by comparing the heat input into the component under conditions of maximum rating evaluated for the thermal resistance situation $R_{ti} \gg R_{te}$ in Section 3.1, and the capability of the device for dissipation of the heat input due to dielectric losses, calculated with the assumption of equal temperature within the entire body of the dielectric and on the electrode surfaces. Calculations in Section 3.2 showed that the thermal balance was shifted towards heat dissipation, preventing the device reaching the temperature of $T_{\text{ambient}} + \Delta T$ under conditions of maximum rating.

While no detailed discussion was made of the magnitude of temperature difference between the central layer of the dielectric and the electrode surface, upon which the rating characteristics of the capacitor are based, it appears reasonable to assume that the lower the thermal conductivity of the ceramic dielectric and the larger the dielectric thickness, the higher the above temperature difference may be.

As the above observations were made within the frame of reference of examples evaluated with the constraint imposed by the maintenance of equal values of capacitances for the active layers; they fail to indicate further possibilities of design inherent in the multilayer structure of the capacitor. These are indicated in the following.

A capacitance of e.g. 41.8 pF in a component with the total thickness specified for device b) in Section 2, may be obtained by the parallel connection of 10 active layers with the capacitance of 4.18 pF each. With the tenfold increase of the dielectric thickness, the maximum rated voltage would increase accordingly, while the maximum current rating maintained unchanged. Alternatively, by the construction of a multilayer component with active layers of smaller thicknesses than indicated in the example connected in series-parallel combination within the monolithic block, the maximum current rating may be increased and the maximum voltage rating maintained unchanged.

Additional possibilities of design are the construction of capacitor arrays, with different values of capacitances, current, voltage and power ratings,

incorporated into the same monolithic ceramic chip.

With further progress made in the technology of thick film conductor compositions, sufficient control and refinement in their application and co-sintering with ceramic dielectrics is anticipated to open up possibilities for the construction of monolithic series or parallel reactances. The theoretical basis and some of the applications of such devices were discussed by R. E. Lafferty.[11] The uses indicated are connected with measurement methods and instruments, such as frequency sensitive resistors with functions of R_p or R_s proportional to $f, f^2, f^{-1}, f^{-2}, f^{-½}$; and development of Q standards whose Q is practically constant over a frequency range of several decades.

Maximum thermal voltages for the thermal resistance situation of $R_{ti} \ll R_{te}$ were calculated by N. Klein.[7] The results of calculations were found to agree very well with observations of d.c., a.c. and pulse maximum thermal voltages in thin film specimens of silicon monoxide dielectrics.

The ceramic powder dry pressing, laminate, and thick film technologies presently involved in the construction of multilayer ceramic capacitors, do not lend themselves readily for the fabrication of a device where the thermal condition of $R_{ti} \ll R_{te}$ obtains. The situation is reviewed in the following design calculations.

Assume that a single layer capacitor with a capacitance of 41.8 pF has to be designed, using the same dielectric as the devices discussed above, and platinum electrodes. If a d.c. working voltage of 50 V is to be assured, with the assumption of a d.c. test voltage twice the value of the working voltage, i.e. $V_{test} = 100$ V, and $m = 2$, the minimum dielectric thickness according to Eq. (1) will be $h = 5 \times 10^{-3}$ mm (0.0002 in), approximately an order of magnitude less than in device b). The electrode area of a device with the dielectric thickness of 5×10^{-3} mm (5 μm) and capacitance of 41.8 pF will be 1.57 mm^2 (0.0024 in^2) with lateral measurements of length = width = 1.25 mm (0.049 in). With the internal thermal resistance of such device, $R_{ti} = 3.96$ KW^{-1} cm^{-1}, electrodes for the ratio of $R_{ti}/R_{te} = 0.1$ to be obtained. These electrode thicknesses are not attainable by the thick film conducting compositions.

Considering the condition of thermal equilibrium according to Eq. (34) with the external thermal conductance $\gamma = 0.025$ WcmK^{-1}, and assuming $\Delta T = 0.01$ K; $P_{input} = 0.505$ W is obtained as the maximum heat the device is capable of dissipating through heat conduction by the electrodes.

Capability of heat dissipation could be improved by the use of electrode metals with higher thermal conductivities than that of platinum, a standard practice in thin film capacitors or more significantly by the reduction of the electrode thickness. This remedy would naturally alter the thermal resistance situation of $R_{ti} \ll R_{te}$ in the component. By constructing the above device with 0.01 mm ($\cong$ 0.0004 in) thick platinum electrodes, the external thermal conductance will increase to $\gamma = 11.39$ WcmK^{-1}, yielding $P_{input} = 228$ W for the maximum heat dissipation capability of the device. The ratio of R_{ti}/R_{te} would alter to 45.1, approximately the same as in device b), rendering the thermal condition $R_{ti} \ll R_{te}$ not applicable.

By proceeding with an estimate, characteristics of maximum RF current and voltage ratings will be evaluated for a heat input of 10 W, to satisfy the thermal balance condition in Eq. (34).

An estimate of the value of maximum rated voltage may be obtained from the discussion in Section 3.1. The RMS value of the maximum rated voltage is:

$$V_{max} = m' V_{br}(\text{d.c.}) \tag{36}$$

where m' is taken as $m' = 0.7$; and while, from the values of d.c. dielectric strength and thickness of the ceramic, V_{br}(d.c.) = 200 V is obtained it is expedient to substitute the value of $V_{test} = 100$ V for V_{br}(d.c.) into Eq. (36), yielding $V_{max} = 70$ V RMS.

From Eq. (25), the voltage limiting impedance, Z_{VL}, for a maximum power rating of 10 W and maximum RF voltage rating of 70 V RMS, is calculated as 490 ohm. Thus the rating of the 41.8 pF capacitor will be limited by the maximum voltage of 70 V RMS for frequencies below 7.8 MHz.

Assuming a maximum power loss of 0.04 dB (0.5%) of the input power is permitted in the capacitor in a particular circuit application, the value of heat input into the capacitor due to dielectric losses must not exceed 50 mW, with the maximum rated current flowing through the device. With the assumption of higher dielectric losses in the component of identical capacitance but smaller dielectric thickness than device b), and with the assumption of an equivalent series resistance, R_s, of the order of 0.1 ohm, the maximum rated current may be assessed according to Eq. (35) as $I_{max} = 0.71$ A RMS.

The maximum current limiting impedance calculated from Eq. (25) will be $Z_{CL} = 20$ ohm. The rating of the 41.8 pF capacitor will be limited by the maximum power of 10 W between the frequencies of 7.8 MHz and 190.4 MHz; and by the maximum current of 0.71 A above the frequency of 190.4 MHz.

While the above considerations may be illustrative

of the thermal design of thin film capacitors, it is clear that the construction of devices with dielectric thicknesses of the order of few tenths of a micron is outside the realm of ceramic technology of the present, which is based upon the processing of raw material of powders with typical particle diameters of few microns to few tenths of a micron.

Multilayer ceramic capacitors with active layers of 0.025 mm (≅ 0.001 in) dielectric thickness, and lateral measurements of those of device b), or approximately half of these, were found to yield maximum current rating characteristics approaching those of the thin film capacitors. Maximum voltage ratings of these components were found suitable for applications in RF transistor circuits.

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