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THE PROBLEMS OF SELECTING A PROPER MICROLITHOGRAPHIC IMAGING SYSTEM

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Considering the increased importance of custom integrated circuits in electronic equipments and other products there is a research activity in Hungary to develop a "state-of-the-art" semiconductor development laboratory for technology development and prototype circuit fabrication. The most significant parts of this laboratory are circuit design, mask making and wafer lithography. The problems associated with these three parts are discussed.

1. INTRODUCTION

Considering the increasing importance of integrated circuits in the development of electronic equipments and other products, the user industries must have easy access to sophisticated, highly developed I/C devices. An ideal digital system for instance uses similar integration levels for all major building blocks, such as microprocessors, memories and random logic.

Random-logic circuits that hold a digital system together, are implemented largely with a number of small and medium-scale integration (SSI and MSI) chips.

Most requirements can be met with standard off-the-shelf integrated circuits, but for those that cannot, one has to find another solution. The alternatives are:

- circuit designs from discrete and off-the-shelf SSI-MSI components
- hybrid circuit designs
- customized integrated circuit designs.

In a country like Hungary, it is not possible to compete with off-the-shelf supplies. The purpose of our research and development activity is to encourage the use of highly developed, special (customized) circuits by the main consumers in Hungary, (data processing, telecommunication, professional electronics, consumer electronics and medical equipments.)

2. DEVELOPMENT LABORATORY

To fulfil the above requirements it is necessary to develop a "state-of-the-art" semiconductor development for technology development and prototype circuit fabrication. This semiconductor development laboratory and pilot production has to support fabrication for a variety of silicon technologies such as metal and silicon gate p-channel, n-channel and complementary metal oxide semiconductors (MOS), and high-speed and high-frequency bipolar devices.

Fortunately such facilities have a substantial amount of multi-process capability. By careful planning, a number of technologies can be accommodated in a single facility.

For example, the principal difference between modern MOS and bipolar processes is the utilisation of epitaxial growth for bipolar processing.

The addition of Schottky devices to integrated circuits usually only involves equipment for the specialized metallizations required.

Most of the important advantages of a flexible (multiprocess) facility are as follows:

- design optimization capabilities
- the ability to have proprietary circuit design and processing
- better reliability control
- maintenance of contributed value.

The significant parts of the semiconductor development laboratory are circuit design, mask making, wafer processing, testing and packaging. (Figure 7).

A typical development cycle of custom design circuits are as follows:

- product concept
- specification of chip funtionality and electrical parameters
- logic/architecture design
  - custom random logic
  - PLA, ULA, gate array
  - microprocessor/microcomputer
- circuit design/broadboard logic

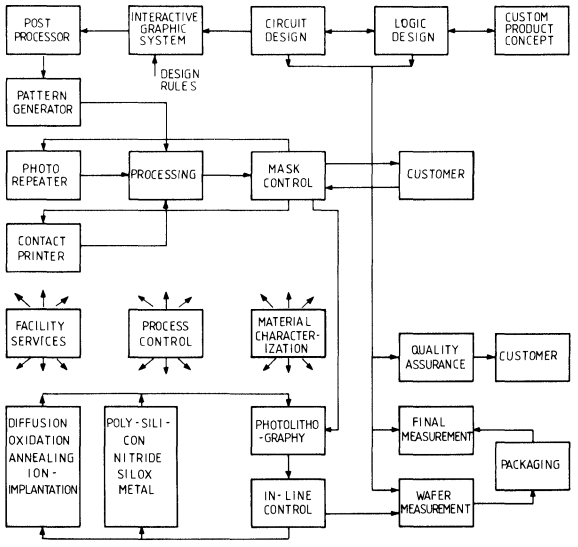

FIGURE 1 The significant parts of the semiconductor development laboratory.

– composite plan and design of chip
– test word development
– digitize/check composite plan
– mask making
– wafer fabrication
– assembly/functional and electrical test
– approval of prototypes.

3. MICRO LITHOGRAPHY

The role of computer graphics, mask making and wafer imaging techniques in the design and manufacture of custom integrated circuits will now be discussed. It deals with the critical aspects of both the design and prove-out phase and the following manufacturing activity.

The complexity of integrated circuits has led to the wide acceptance of computer aided design in this technology. Today the overwhelming majority of IC designs are developed using some form of CAD.[1]

There are three general classes of CAD programs in use in physical design today:[1]

– one is the automated layout program
– a second is the generation of the design manually followed by digitizing using an interactive graphics system (IGS)
– the third uses the IGS as an on-line design tool.

The class of CAD used depends on the type of circuit design: i.e.:–

–automated layout programs work with standard cells (similar to automated PCB layout systems). They can provide complex LSI layouts. This method is ideal for product runs of less than a few thousand devices, especially when combined with an IGS for editing and modification.

– The IGS offers the best approach for complex and large circuits. IGS systems can be used to generate both the IC design and the pattern generator PG control tapes for mask making.

If the computing power of the system is high, then the response time of the IGS system is high, and this allows the user on-line design, completely eliminating manual layout. On-line design lets the designer layout and modify the design directly on a display with designer oriented system capabilities. But generally the two techniques are used together. (See Figure 2).

IGS is the proper choice for cell design, chip planning and circuit layout. In addition, IGS can be used for design rule checking, automatically locating physical design errors at any time in the design process. Earlier in the design process, IGS is used to develop logic schematics for the circuit and to feed logic simulation and test generation programs, and at the end of the design process to make the documentation.

Let us consider now the available techniques for transferring a device from design to wafer manufacture and let us consider the application to a custom design development and manufacturing facility.

The optical and e-beam techniques are all commercially available for mask generation. It is possible to apply these techniques either singly or in combination.

As the demands for narrower IC line widths goes into the micron and sub-micron region, pattern and mask generation equipment becomes more complex and much more expensive. Electron beam technology yields sub-micron graticules, masks (and wafers) that photo-optical methods cannot produce. But improve-

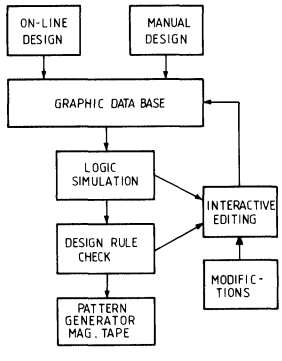

FIGURE 2 The operations in interactive graphic design.

ments are under way in optical pattern/mask generation equipments, as well.

The majority of custom circuits are and will be in the 3 to 4 μm range and quite a lot of them only demand line widths of 7 or 8 μm, especially when the speed is not critical. This is an area, which conventional mask making technology can deal with, using relatively non-expensive equipment.

Data from literature[3] and our experience shows that something of the order of 95 percent of graticules to be produced require less than 20,000 exposures about 2 to 2 1/2 hours to run.

Producing such non-complex on an e-beam graticules system is totally impractical since the system is very expensive. However with devices that require several hundreds of thousandsof exposures per layer, such as big RAMs, ROMs, microcomputers or 16 bit microprocessors, throughput with an e-beam is better than with conventional photo-optical systems.

The major problem with making reticules on an e-beam system is the data handling, because such a system was designed not to make reticules, but to make master masks, or direct exposures on wafers.

We believe e-beam technology will complement, not displace photo-optical equipment for a very long time to come.

The spectacular advances which have occurred, and will continue to occur, in the main stream LSI/VLSI thrust of the semiconductor field will impact no other area more than mask making. To mention a few of these interactions:

– the massive introduction of 1:1 projection printing in wafer fabrication changed the requirements from many quality masks to a much smaller number of "perfect" ones.

– Using direct step on wafer printing is going from reticle directly on the wafer by-passing mask making and masks.

– If fine – line lithography is to advance successfully and if chip areas are going to increase, cleanliness, inspection and repair will have to be further emphasized.

4. WAFER FABRICATION

Perhaps the greatest changes in wafer processing are taking place in the pattern-printing step. At the early stage of the semiconductor industry the high "priests" of science were the engineers who worked in diffusion and oxidation. The diffusion engineers were "educated" how to understand what they were doing and how to figure out mathematically what they were supposed to get when they put wafers into a furnace. Diffusion was a science, oxidation was a chemistry and later ion implantation was physics. The necessary theories, the theoretical background were developed.[4,5,6]

Lithography, the most expensive and most critical part of the entire semiconductor manufacturing process (especially for LSI) was left to languish as being scientifically important.

Today microlithography is generally considered to be the most important technology in the semiconductor industry.[7] Modern microlithography encompasses such diverse disciplines as chemistry, optics, quantum mechanics, electronics, computer graphics and mechanical engineering. It is an interdisciplinary field.

In the production the well-established contact printing is used together with projection printing, and becoming increasingly important are such new techniques as direct step on wafer[8] and exposure of the pattern onto the wafer with electron beams.[9]

Contact printing has excellent resolution, but high defect density.[7] Projection printing is applied typically to such LSI devices as memories, microprocessors and calculators.[7] The vast majority of these chips are needing 3 to 5 μm line widths and in the future the geometries of production chips will require 2- to 2.5 μm. These chips are large with low yields, so even small yield increases will offer big savings.

On the production side of the industry, the major producer will use direct step-on wafer (DSW) for only the most critical masking levels, and 1:1 projection for the other levels of the next generation 2 μm technology. For this purpose custom houses can use contact printers or deep- UV proximity or projection printers.[10]

The various methods of design transfer to slices are complementary and the use of them depends on the requirements, that is on wafer size, feature size, run length, turn around time and on the economics. Figure 3 shows the chosen system.

How a custom house competes over the long term in production efficiency depends on the development time and the success of the equipment which uses the custom circuit.

CONCLUSION

A semiconductor development laboratory for custom design should have a substantial amount of multi-process capability. An interactive graphic system is the proper choice for cell design, chip planning and circuit layout. In the custom field e-beam technology will complement, not displace photo-optical mask

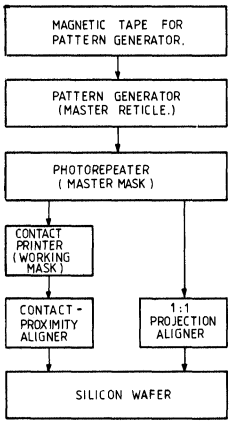

FIGURE 3 The chosen image transfer system.

making equipment. For wafer printing a custom house can use soft-contact printers or deep-UV proximity printers.

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