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# DESIGN OF A 108 PIN VLSI PACKAGE WITH LOW THERMAL RESISTANCE

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The design of a 108 pin VLSI package is described. The package has low thermal resistance and can, therefore, dissipate 4 watts of power. The package design is now being used commercially in high-end computers made by Hitachi.

## 1. INTRODUCTION

The increasing circuit/gate density of LSI chips presents a variety of challenges to packaging technology. The package must absorb an increasing amount of power and an ever growing number of interconnections. Packaging engineers have discussed a number of different packages, but there is no simple formula to determine the most cost effective and reliable combination of package types.

One such approach has developed a package for the ECL VLSI, which has 550 gates, 4W of power and 108 pins.

## 2. PACKAGE DESIGN

The requirement for this package design is, simply stated:

A 550 gate ECL logic VLSI with 4W of power must be mounted in a single package to effect maximum performance.

Therefore, the package should be designed as follows:

1) number of pins: 108
2) package size: as small as possible
3) thermal resistance: less than 10°C/W
4) electrical resistance: less than 0.2 Ω from inner to outer leads
5) stray capacitance: less than 3pF
6) sealing: hermetic seal
7) cost: less than the cost per pin on a side brazed dual in line package.

A study has been undertaken to ascertain the feasibility of the above design concept and has achieved a package with high cost-performance.

## 3. THERMAL RESISTANCE

As stated above, the package requires very low thermal resistance. Therefore, the primary consideration in the package design had to be from the thermal standpoint.

The main thermal path for the power consumed in the chip is from the base to its surface, and from the surface to the ambient atmosphere. The former thermal conductive path had a resistance ($R_{CD}$) dependent upon the thermal conductivity of the base materials. The latter is heat transfer by convection with resistance ($R_{CV}$) dependent upon the surface area of the base. Thus the main thermal resistance ($R_T$) is determined by the following formula:

$$R_T = R_{CV} + R_{CD}$$

The resistance, $R_{CV}$, is indicated by the following equation:

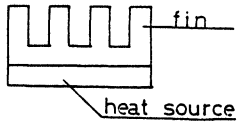
$$R_{CV} = \frac{1}{A_f \cdot \alpha \cdot \phi}$$

Where, $A_f$ is the surface area of the base, $\alpha$ is a heat transfer coefficient and $\phi$ is fin efficiency.

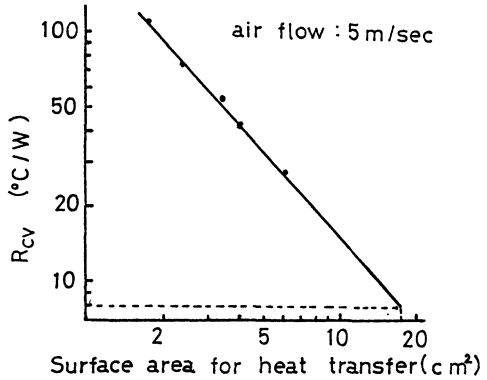
An experimental measurement for $R_{CV}$ was studied using the comb configuration fin structure shown in Figure 1 (a). Thermal resistance, $R_{CV}$, is well correlated to be in inverse proportion to the surface area available for heat transfer as shown in Figure 1 (b). The objective for the thermal resistance of the design was set at 10°C/W maximum ($R_{TMAX}$), but should be kept at a nominal value of 8°C/W ($R_{TNOM}$) in actual performance.

Thus, a large surface area (ie. 20 $cm^2$) is required. Still, $R_{TNOM}$ can not equal $R_{CV}$. There must be an allowance made for $R_{CD}$. The following formula was developed:

$$R_{TNOM} = 8°C/W = R_{CV} + R_{CD} = 7°C/W + 1°C/W$$




(a)




(b)

FIGURE 1 Thermal resistance based on convective heat transfer.

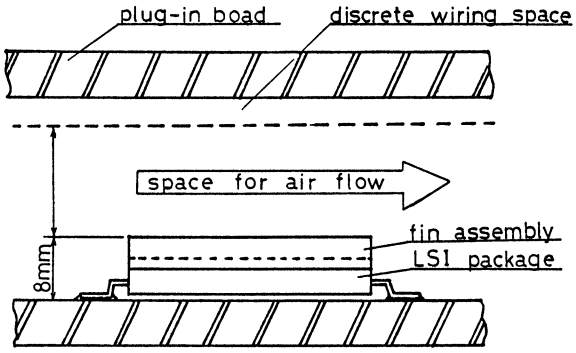



FIGURE 2 Limitation of package height based on stacked plug-in board spacing.

On the other hand, to keep good air flow conductance, for cooling, between boards mounted with LSI's, the package height should be as small as possible. A height of 8 mm was determined for the package considering stacked plug in board spacing as shown in Figure 2, and 21.6 mm was chosen as the size of the base (square) to provide a 20 $mm^2$ surface area for the fin assembly, according to the design data as shown in Figure 3. Package size reduction is desirable in high density circuits. However, there is a limitation due to the need for a large surface area for heat transfer.

Thermal resistance, $R_{CD}$, the remainder of $R_T$, can have only a value up to 1°C/W. Proper materials for good thermal conductivity from base to fin assembly must be chosen to achieve this value. Resistance $R_{CD}$ can be defined by the following equation when thermal flow flux is in parallel:

$$R_{CD} = \sum \frac{t_i}{l_i^2 \cdot \lambda_i}$$

where, $t_i$ is the thickness of each material and $l_i$ is the length of each material which is assumed to be a value approximately equal to chip size. $\lambda_i$ is the thermal conductivity of

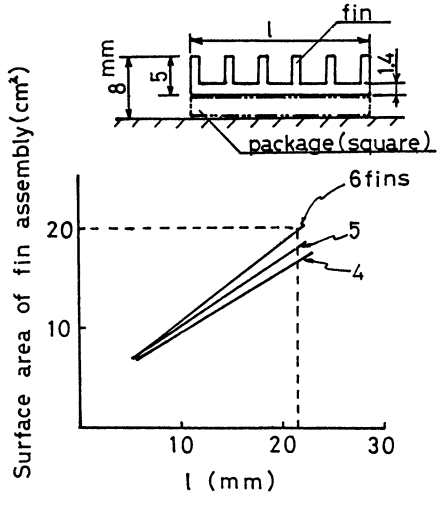



FIGURE 3 Relationship between package base dimensions and fin surface area.

TABLE I
Thermal resistance based on thermal conductivity

| Thermal path | Model A Material | t | λ | $R_{CD}$ | Model B Material | t | λ | $R_{CD}$ | Model C Material | t | λ | $R_{CD}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Die attached eutectic | Au/Si | .004 | .61 | .032 | Au/Si | .004 | .61 | .032 | Au/Si | .004 | .61 | .032 |
| Base | Mo | .06 | .34 | .87 | Alumina | .03 | .03 | 4.94 | Alumina | .03 | .03 | 4.94 |
| Base/stud attached eutectic | Ag/Cu | .005 | .66 | .037 | Ag/Cu | .005 | .66 | .037 | Ag/Cu | .005 | .66 | .037 |
| Stud | Oxygen Free Copper | .5 | .94 | 2.63 | OFCu | .5 | .94 | 2.63 | Koval | .5 | .04 | 61.73 |
| Total | | | | 3.57<br>.85°C/W | | | | 7.64<br>1.83°C/W | | | | 66.74<br>15.94°C/W |
| Actual measurement | | | | .4–1.0°C/W | | | | | | | | |

Unit: t (cm), λ (cal/cm sec °C), $R_{CD}$ (°C sec/cal).

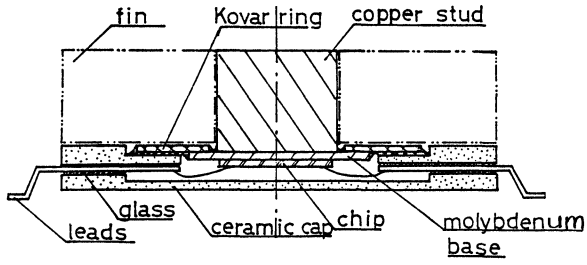



FIGURE 4 LSI package Cross-section.

each material. To achieve an $R_{CD}$ under 1°C/W, structure model A, from Table 1, is the only solution. This resulted in the thermal dissipation structure is shown in Figure 4.

## 4. DESIGN OF THE PACKAGE STRUCTURE

Because the size of the base area is limited by thermal dissipation, a side length of 21.6 mm was determined for the base. This in turn led to a lead pitch determined by the number of leads, as shown in Figure 5. For a 550 gate logic LSI with 108 pins, a 30 mil pitch is necessary (Fig. 5). The package structure must be an almost flat package type due to the previously mentioned height limitations (8 mm).

The glass sealed ceramic structure (similar to the cerdip) was chosen from the consideration of both reliability and cost. The structure can achieve hermetic seal and the objective cost compared to cofired ceramic structure.

Furthermore, the thermal dissipation metal (model A) should be built into the base ceramic without any stress. However, there is a mismatch in thermal expansion in that expansion of molybdenum in model a is too low and the expansion of copper is too high compared to an alumina ceramic base. Thus, a Kovar ring is utilized to manage the thermal expansion mismatch between the molybdenum and the alumina ceramic base, as shown in Figure 4.

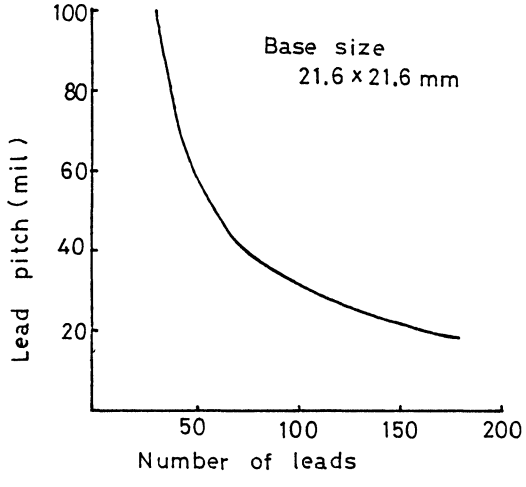



FIGURE 5 Relationship between number of leads and outer lead pitch.

This package has successfully endured the following representative envelopmental tests:

1) Thermal shock test (30 cycles in liquid nitrogen to 150°C fluorinert): No hermeticity failure in 10 pieces.

2) Temperature cycle test (600 cycles, −55 ⇔ 150°C: No hermeticity failure in 10 pieces.

## 5. CONCLUSION

The main features of this new package are as follows:

1) Flat package type

2) Outer lead pitch: 30 mil

3) High thermal conductive metal radiation with fin assembly

4) Ceramic body size: 21.6 x 21.6 mm

5) Package height: 8 mm

These package features are shown in Figure 6, and package performance is as follows:

1) Thermal resistance from junction to ambient atmosphere at 5m/sec air flow: average 8°C/W, maximum 10°C/W.

2) Hermetic sealing.

3) Stray capacitance between the leads: 1.7-2.9pF

4) Electrical resistance of the leads: .1- .5 Ω

Size and thermal dissipation: the package presents a very high performance structure for ECL high speed VLSI's.

This package is used in commercially available high-end computers made by Hitachi, and should be feasible for future high speed logic VLSI's as 1500 gates.

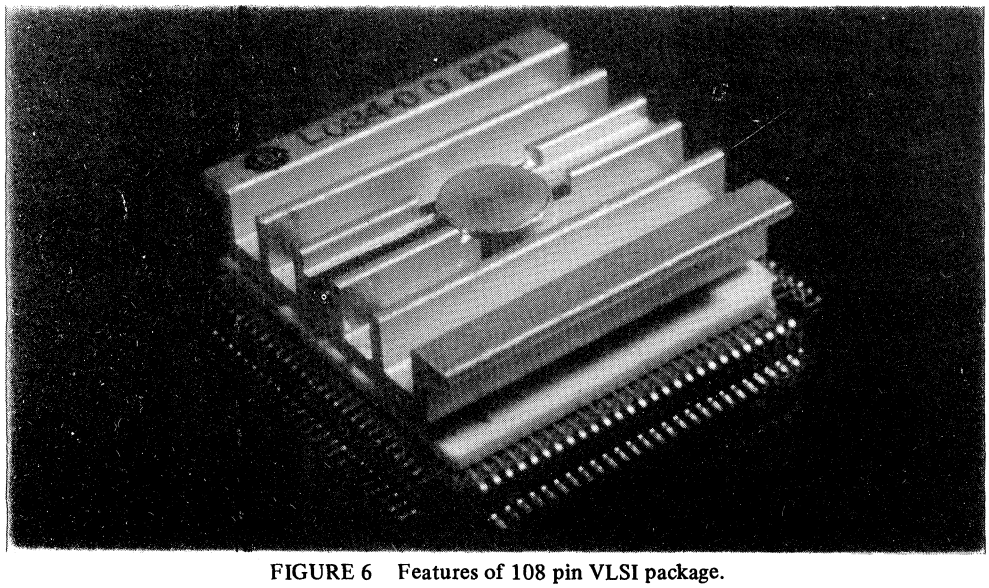


FIGURE 6 Features of 108 pin VLSI package.