

Research Article

An Analog Template-Based Classifier Using MOS Translinear Loops

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An analog template matching pattern classifier circuit based on a new synthesis of Euclidean distance calculation is presented. It is composed of simple two-quadrant squarer/divider blocks. The circuit employs MOSFETs that operate in strong inverted saturation region performing electronically simulated translinear loop. The converter features very low supply voltage (0.9 V), immune from body effect, two-quadrant input current, large dynamic range, and low circuit complexity. The circuit was successfully applied to the recognition of some simple patterns. Simulation results by HSPICE show high performance in the separation of circuit and confirm the validity of the proposed technique.

1. Introduction

Classification algorithm as a key function in information processing is used for analyzing groups of vector data. In fact, this algorithm is employed to find optimum prototype vector, from which the input vector is compared. There are two ways to implement classifier. One is employing digital computer, and the other is using analog circuits. Analog implementation of classification algorithm holds a series of advantages over digital implementation. The complexity of analog circuit blocks required to implement such systems is in general lower when compared with digital counterpart, and, additionally, A/D and D/A interfaces towards sensors and actuators are not needed. Moreover, better performances can be obtained in terms of velocity of signal processing, by fully exploiting the capability of analog circuits to implement parallel processing. Because, it would be intolerably time consuming when the number of template patterns becomes quite large and the problem is in excess of even the state-of-the-art computer technologies. Hence, analog implementation employing parallel very-large-scale integration (VLSI) architectures is desired for real-time classifier circuits. An attractive method to implement classification algorithm is employing Euclidean distance calculator. Recently, some

analog integrated forms of Euclidean distance calculator have been proposed [1–6]. They can be used in classifications algorithms to measure how close an input pattern is to the prototype patterns. One attempt is to design vector summation circuit in voltage-mode approach based on the bipolar dynamic translinear implementation [1]. However, in many situations, particularly in mixed A/D systems, it is desirable to implement the circuits in MOS technology [2]. But, in traditional voltage-mode architectures, the supply voltage level reduction has a clear impact on the dynamic range of the circuits. Current-mode approach deserves particular mention, since it provides a large dynamic range for the currents considered now as processing variables, while maintaining reduced voltage swings. In current-mode processing the input signals which are mostly in current domain are nonlinearly transformed to the compressed voltage signal domain. Taking advantages of the current mode approach, Euclidean distance calculator circuits were proposed in current mode [3–6]. In these proposals, Euclidean distance calculator circuit has been performed by several basic building blocks, such as geometric-mean, squarer/divider, absolute, and subtracter. For design of these functions, stacked translinear loop [3–5] or class-AB linear transconductors [6] have been employed. The

main drawbacks of these proposed circuits are as follows: firstly, these circuits operate in only one-quadrant input current that means the extra needed functions for full-wave rectification is needed; secondly, the extra needed functions lead to a large number of transistors and high power consumption; thirdly, the body effect of translinear MOSFETs in the squarer/divider block decreases the accuracy; finally, in these circuits due to the stacking of gate-source voltage of MOS transistors, they are often not well suited to low-voltage operation. In [7], a MOS current-mode classifier based on current mirrors is presented; however, this circuit requires double supply and with the cost of a large supply voltage.

In this paper, to overcome the above problems, a novel synthesis for classifier algorithm based on the Euclidean distance calculator [8] is presented. In the presented synthesis, the number of basic building blocks is severely reduced, and it just comprises simple two-quadrant squarer/divider unit [8, 9] as the fundamental unit. Therefore, the system complexity of the proposed system is much less than those reported before [3–6]. The full parallel property of the system reduces the identification time and lead to a very regular structure. In the presented synthesis, a new squarer/divider based on electronically simulated translinear loop with two-quadrant input is proposed. As the proposed squarer/divider circuit operates in two-quadrant input, so the absolute and subtracter units are not needed. In this circuit, due to the fact that the source of the translinear MOSFETs is connected to the substrate, this circuit is immune to the body effect.

The paper is organized as follows. In Section 2, mathematical theory and analysis of current-mode fuzzy classifier and also Euclidean distance calculator is discussed. Section 3 explains the proposed circuit design for two-quadrant squarer/divider unit, as the basic building block of classifier. Simulation results are presented and discussed in Section 4, and concluding remarks are provided in Section 5.

2. Theory and Analysis of Current-Mode Fuzzy Classifier

Fuzzy classification technique is attractive solution to pattern recognition when it is implemented for computing in parallel systems. Particularly, the data recognition by the fuzzy nearest neighbor prototype (FNP) is very efficient in this type of systems [4, 10, 11]. In other words, it is the basis of finding optimal prototype vectors, from which the input vectors is compared, using fuzzy values that are expressed as membership degrees. Hence, this algorithm can be employed as a recognition task for classification. In this algorithm and for the first step, the similarity between each template V and an input unknown pattern U is measured by calculating the Euclidean distance $D(U, V)$. The less distance $D(U, V)$ is, the more similarity between V and U is. In other words, the Euclidean distance is a direct measure of similarity between the template vectors that is closest to an input vector, in the sense that among a finite set of reference vectors, the least distant one from the input is the most similar to the

input. Therefore, Euclidean distance is useful in classification algorithm [3–6].

The Euclidean distance between two n -dimensional vectors

$$\begin{aligned} U &= (u_1 \ u_2 \ \cdots \ u_K), \\ V &= (v_1 \ v_2 \ \cdots \ v_K) \end{aligned} \quad (1)$$

is represented as follows:

$$D(U, V) = \sqrt{\sum_{k=1}^K (u_k - v_k)^2}, \quad (2)$$

where u_k and v_k are the k th entry of vectors U and V , respectively.

To improve interpretability and simplify the decision system, a simple model of the membership functions is employed in the classifier that allows us to normalize Euclidean distance calculator in order to have not only normal output but also activated output for similar input patterns. In most of the fuzzy control systems, membership functions are chosen arbitrarily by the users based on their perspectives. In pattern-recognition problems, attempts have been made to analysis the flexibility and uncertainty in membership function evaluation using bound functions. In the present work and in the second step, the fuzzy value of membership degree $\mu(D)$, that a particular input U has relative to the template vectors V , is expressed as follows [4]:

$$\mu(D) = \frac{1}{1 + D(U, V)}. \quad (3)$$

Equation (3) produces a membership degree with value one when the corresponding distance is zero and produces zero when the corresponding distance approaches infinity. Hence, the input vector U can be classified into the class with the maximum membership degree.

In conventional voltage-mode integrated circuits, due to the linearity of their building blocks, internal voltage swings readily reach the limitation imposed by the supply voltage for moderate input levels. An elegant procedure for solving this issue would be to design the circuits externally equivalent to the linear realization, having input and output in current form and whose internal voltage swings were compressed with regard to their counterparts in the linear system; thus, a large signal swing at the input would not be translated into the corresponding large internal voltage swings, as for the linear circuits; on the contrary, internal voltages would remain almost oblivious to this increase in the input level if the compression law is strong enough [12]. This alternative processing is not only possible, but also readily carried out by taking advantage of the current-mode approach. Many useful synthesis methods have been proposed [1–6, 8, 9, 12, 13], evidencing the growing interest in current-mode circuits in the last years, due mainly to their aforementioned suitability for preserving dynamic range in the low-voltage scenario imposed by modern technologies. The basic feature of current mode is the exploitation of the

nonlinear current-to-voltage characteristics of bipolar [14], MOS transistors [2–6] in order to achieve reduced voltage swings at internal nodes, thus allowing large dynamic ranges at low supply voltages. The down scaling and suitability for mixed-mode realizations is best performed in modern deep-submicron CMOS integration processes [12].

By rearranging the definition for K -dimension vectors V and U in order to hardware implementation of the Euclidean distance circuit, (1) are expressed as follows:

$$\begin{aligned} I_U &= (I_{u_1} \ I_{u_2} \ \cdots \ I_{u_K}), \\ I_V &= (I_{v_1} \ I_{v_2} \ \cdots \ I_{v_K}), \end{aligned} \quad (4)$$

where I_U and I_V are the current representation of vectors U and V , respectively. Also, I_{u_k} and I_{v_k} are the k th entry of vectors I_U and I_V , respectively.

Employing current-mode approach, an equivalent function of (2) in current mode is given as follows:

$$I_D = \sqrt{\sum_{k=1}^K (I_{u_k} - I_{v_k})^2}, \quad (5)$$

where I_D is the current representation of Euclidean distance $D(U, V)$.

One straight method to circuit design of (5) is using a square-rooter and K squarer units, in addition of K subtracter units and K absolute units [3–6]. However, an effective way is suggested in this work to reduce the number of basic building blocks. To this end, squaring operation is taken on both sides of (5), which results in

$$I_D^2 = \sum_{k=1}^K (I_{u_k} - I_{v_k})^2. \quad (6)$$

A mathematically equivalent expression, but more precise considering the offset of the system [15], is obtained as

$$I_D = \frac{\sum_{k=1}^K I_{d_k}^2}{I_D}, \quad (7)$$

where I_{d_k} is the difference between k th entry of two vectors U, V , and it is equal to

$$I_{d_k} = I_{u_k} - I_{v_k}. \quad (8)$$

By breaking out the weighted summation of the numerator terms of (7), and also using the fact that $\sum_i x_i/y = \sum_i (x_i/y)$, it can be rewritten as

$$I_D = \sum_{k=1}^K \frac{I_{d_k}^2}{I_D} = \sum_{k=1}^K I_{SD,k}, \quad (9)$$

where $I_{SD,k}$ is equal to

$$I_{SD,k} = \frac{I_{d_k}^2}{I_D}. \quad (10)$$

The right hand side of (9) is summation of n two-quadrant squarer/divider units. For each squarer/divider unit, the

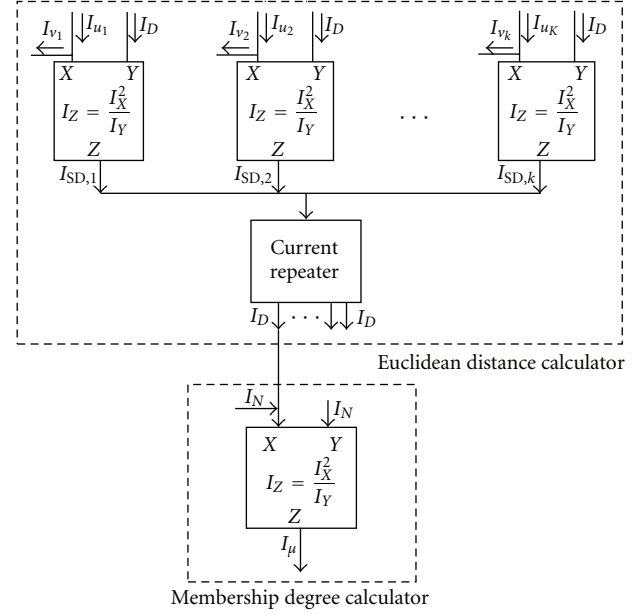


FIGURE 1: Block diagram of the proposed current-mode fuzzy classifier.

output current is $I_{SD,k}$, and the input currents are difference between k th entry of two vectors $U, V(I_{d_k})$, as the squared input of the unit and the output current of Euclidean distance calculator (I_D), as the divisor input of the unit. It should be pointed out that the squared input current in the numerator of squarer/divider unit is bidirectional current signal. Hence, the squarer/divider unit should be designed to operate two-quadrant.

Also, for current-mode realization of the components of fuzzy layer, membership degree calculator I_D is used for the current signal representation of the Euclidean distance and the current signal I_{μ} is represented for the membership degree $\mu(D)$. For scaling operation, the current signal that makes the level of membership degree current in this design consistent, a constant normalized current signal I_N is introduced. So, (3) is expressed in current-mode as follows [4]:

$$I_{\mu} = \frac{I_N^2}{I_N + I_D}, \quad (11)$$

that produces a membership degree with value of constant normalized current signal $I_N (=20 \text{ uA})$ when the corresponding distance is zero and produces zero membership degree when the corresponding distance approaches infinity."

From (11), the membership degree calculator can be designed by the employing squarer/divider unit with input currents of I_N and $I_N + I_D$ as the squared and the divisor inputs, respectively.

Figure 1 shows block diagram of the current-mode fuzzy classifier. It is composed of two principle building blocks: Euclidean distance calculation and membership degree calculator. In this figure, Euclidean distance calculation block consists of K two-quadrant squarer/divider units that are connected in parallel form, according to (9). These parallel

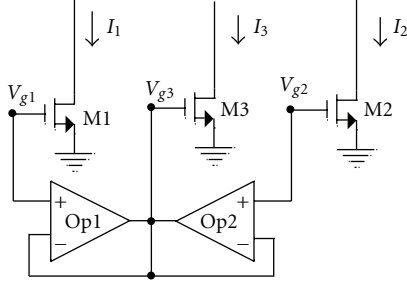


FIGURE 2: Basic circuit diagram of electronically simulated translinear loop.

units are cascaded with another squarer/divider unit, which is used to implement membership degree calculator, according to (11). From this figure, it can be seen that to design fuzzy classifier it is just needed to design two-quadrant squarer/divider unit, as the fundamental unit. Therefore, the number of basic building blocks in the presented synthesis is severely reduced compared to the other proposed that reported before [3–6].

3. Circuit Design of the Proposed Squarer/Divider

The squarer/divider can be implemented by using of sigma-delta data converter [16], translinear loop [3–5], or class-AB transconductance [6] circuits. All these above mentioned squarer/divider circuits operate in only one-quadrant input current. Additionally, employing sigma-delta converter needs a large number of transistors, switches, and capacitors that leads to a high circuit complexity, chip area, and power consumption [16]. MOS translinear circuits can be categorized as follows: stacked loop, up-down loop, and electronically simulated loop [13]. The stacked loop [3–5] similar to class-AB transconductance [6] suffers from body effect. Influence of the body effect in up-down loop [17] is smaller than in stacked loop but more circuits for current injection in transistors are required.

In order to implement the MOS Translinear loops, MOS transistors are assumed to be operating in strong inversion and saturation, their gate-source voltages will be connected in series. So, there gate-to-source voltages are related by [17]

$$V_{gs1} + V_{gs2} = V_{gs3} + V_{gs4}. \quad (12)$$

The drain current and gate-source voltage of a MOSFET in strong inversion and saturation are by

$$I = K(V_{gs} - V_{th})^2, \quad (13)$$

where $K = \mu C_{ox} W/2L$ stands for transconductance parameter and V_{th} is the threshold voltage

$$\sqrt{\frac{I_1}{(W_1/L_1)}} + \sqrt{\frac{I_2}{(W_2/L_2)}} = \sqrt{\frac{I_3}{(W_3/L_3)}} + \sqrt{\frac{I_4}{(W_4/L_4)}}. \quad (14)$$

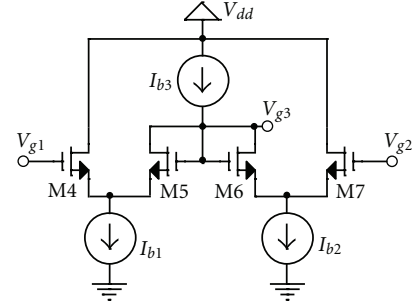


FIGURE 3: Circuit diagram of the voltage mean operation.

Figure 2 shows the basic circuit of the proposed electronically simulated translinear loop employing MOSFETs that are operating in saturation region. The circuit consists of three MOS transistors (M1, M2, and M3) and two op-amps (Op1 and Op2). These two op-amps are employed for voltage mean operation and they force the gate voltage of transistor M3 to remain the mean voltage of the gate voltage of transistors M1 and M2. In other word, it can be written in mathematical form as follows:

$$V_{g3} = \frac{1}{2}(V_{g1} + V_{g2}), \quad (15)$$

where V_{g1} , V_{g2} , and V_{g3} are gate voltage of transistors M1, M2, and M3, respectively. Figure 3 shows the circuit realization of the voltage mean operation, using transistors M4–M7 and current sources I_{b1} – I_{b3} .

Employing the I – V relationships for transistors M1, M2 and M3 in Figure 2, it results in

$$I_1 = K1(V_{g1} - V_{th})^2, \quad (16)$$

$$I_2 = K2(V_{g2} - V_{th})^2, \quad (17)$$

$$I_3 = K3(V_{g3} - V_{th})^2. \quad (18)$$

Assuming that $K_3 = 4K_1 = 4K_2$, substituting (15) into (18) and then performing square-root operation on the both sides of (16)–(18), the following expression is obtained:

$$\sqrt{I_3} = \sqrt{I_1} + \sqrt{I_2}, \quad (19)$$

$$I_{SD} = \frac{I_{in}^2}{I_{out}} \implies I_{SD} \cdot I_{out} = I_{in}^2. \quad (20)$$

After a little manipulation of (20), it can be expressed in square-root terms as follows [9]:

$$\sqrt{\frac{(I_{SD}/2 + I_{out}/2) + I_{in}}{2}} + \sqrt{\frac{(I_{SD}/2 + I_{out}/2) - I_{in}}{2}} = \sqrt{I_{out}}. \quad (21)$$

Comparing (21) and (19) shows that the squarer/divider is obtained if the relations between current injections

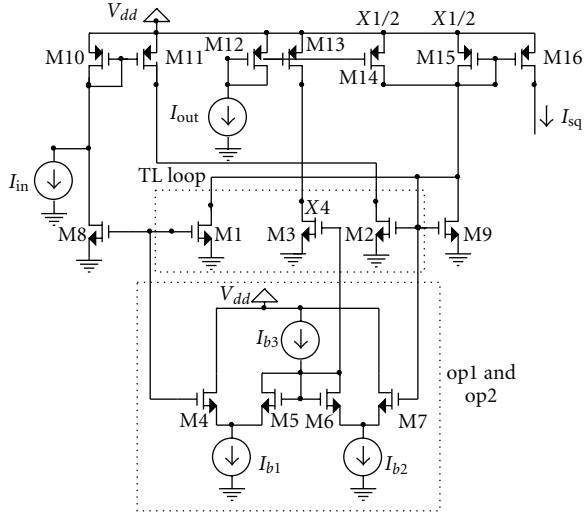


FIGURE 4: Circuit diagram of the proposed two-quadrant squarer/divider.

TABLE 1: Aspect ratios of transistors in Figure 4.

Transistor	Width (um)	Length (um)
M1	4	4
M2	4	4
M3	16	4
M4–M13	4	4
M14	2	4
M15	2	4
M16	4	4

in translinear circuit and input/output currents of the squarer/divider are as the follows:

$$I_{in} = I_2 - I_1, \quad \frac{I_{SD}}{2} = I_1 + I_2 - \frac{I_3}{2}, \quad I_{out} = I_3. \quad (22)$$

Figure 4 shows the complete circuit of the two-quadrant squarer/divider, in which transistors M1–M3 form the MOS translinear loop, and transistors M4–M7 and current sources I_{b1} – I_{b3} are employed for voltage mean operation, and the remaining transistors are employed for injecting the proper currents into the translinear loop transistors with respect to (22). From (21), it is clear that by changing the sign of I_{in} , this equation remains unchanged. This means that the input of the squarer/divider is two-quadrant and acts as a full-wave rectifier. From Figure 4, the sources of translinear MOS transistors are connected to the substrate, so the body effect is completely eliminated. Also, the minimum supply voltage of the circuit is one V_{gs} plus two V_{ds} . Finally, the complexity of this circuit is less than those reported before.

4. Simulation Results

The current-mode fuzzy classifier circuit based on the block diagram of Figure 1, and the proposed two-quadrant

P1	P2	P3
P4	P5	P6
P7	P8	P9

P

FIGURE 5: The schedule of the entries (p_1 to p_9) of the pattern vector P .

squarer/divider of Figure 4 was designed. The circuit was simulated by HSPICE with TSMC 0.18 um CMOS process parameters, confirming the accuracy of the proposed method. $I_{b1} = I_{b2} = I_{b3} = 2 \mu\text{A}$ and $V_{dd} = 0.9 \text{V}$, $I_N = 20 \mu\text{A}$ were employed. The aspect ratios of the transistors of Figure 4 are shown in Table 1. To demonstrate the application of this proposed Euclidean distance calculator circuit, this circuit is employed to template matching in pattern recognition system. As Figure 5 shows, the patterns are partitioned into a 3×3 grid, in which each grid filled with either white or black color, and characterized, by a vector P . For circuit realization, each grid is quantized according to its color; that is, the black/white color is represented by the current $30 \mu\text{A}/10 \mu\text{A}$. A transient simulation of the circuit was carried out for providing the similarity measure between three input testing patterns, denoted as $U_i (i \in \{1, 2, 3\})$, and nine template patterns, denoted as $V_i (i \in \{1, 2, \dots, 9\})$ that are shown in Figure 6. Figure 7 shows the Euclidean distance between each input pattern and the nine template patterns. During simulation, the set of each input pattern corresponding to the input vector was held constant while on the 9 template patterns (corresponding to the template pattern vector) were serially recalled, beginning from vectors V_1 until vector V_9 (Figure 6), recalling the next template pattern vector every 1 us. Under the above described conditions, the output, for the input patterns of U_1 , U_2 and U_3 are shown in Figure 7(a), 7(b), and 7(c), respectively. Evidently, the minimum of this distance suggests the nearest match between input pattern and template patterns. Similarly, Figure 8 shows the membership degrees of each input pattern at each time to the each template pattern. The results of simulation show that these template patterns with the maximum matching degree of the input patterns U_1 , U_2 , and U_3 are V_2 , V_6 , and V_4 at the times 1 us, 5 us, and 3 us, respectively. These Figures reveals that these input patterns can be recognized correctly for this circuit and the simulation results are in agreement with the analysis calculations. The given example in the illustration showed that this circuit performs the function of a fuzzy classifier well. In both cases, for Euclidean distance calculator and fuzzy classifier, a decision is obtained by evaluate the similarity of any given input with pattern. However, Euclidean distance calculator of Figure 7 is a direct measure of similarity between the template patterns that is closest to an input pattern in which the least distant one from the input is the most similar to the input (the least distant is

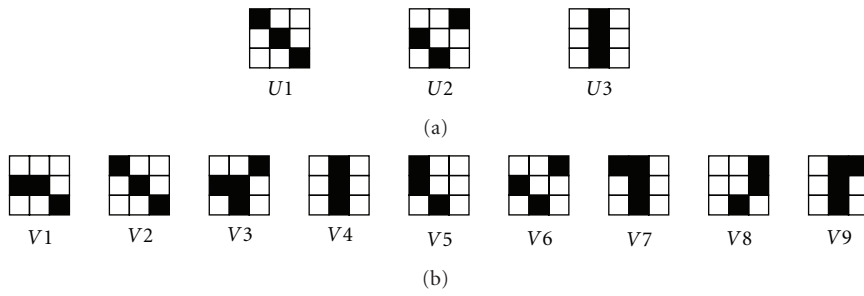


FIGURE 6: (a) the input patterns U_i (up). (b) template patterns V_i (down).

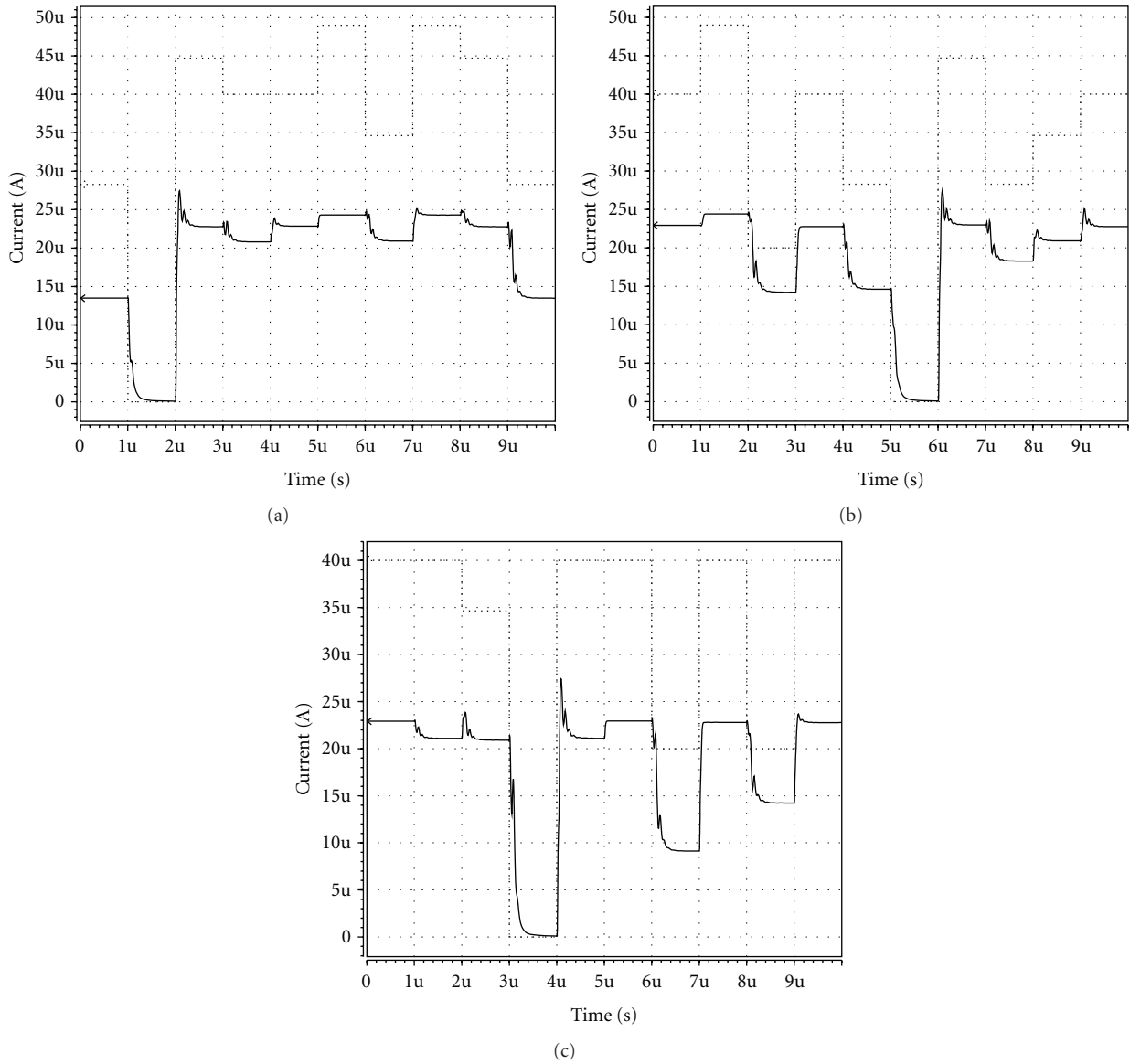
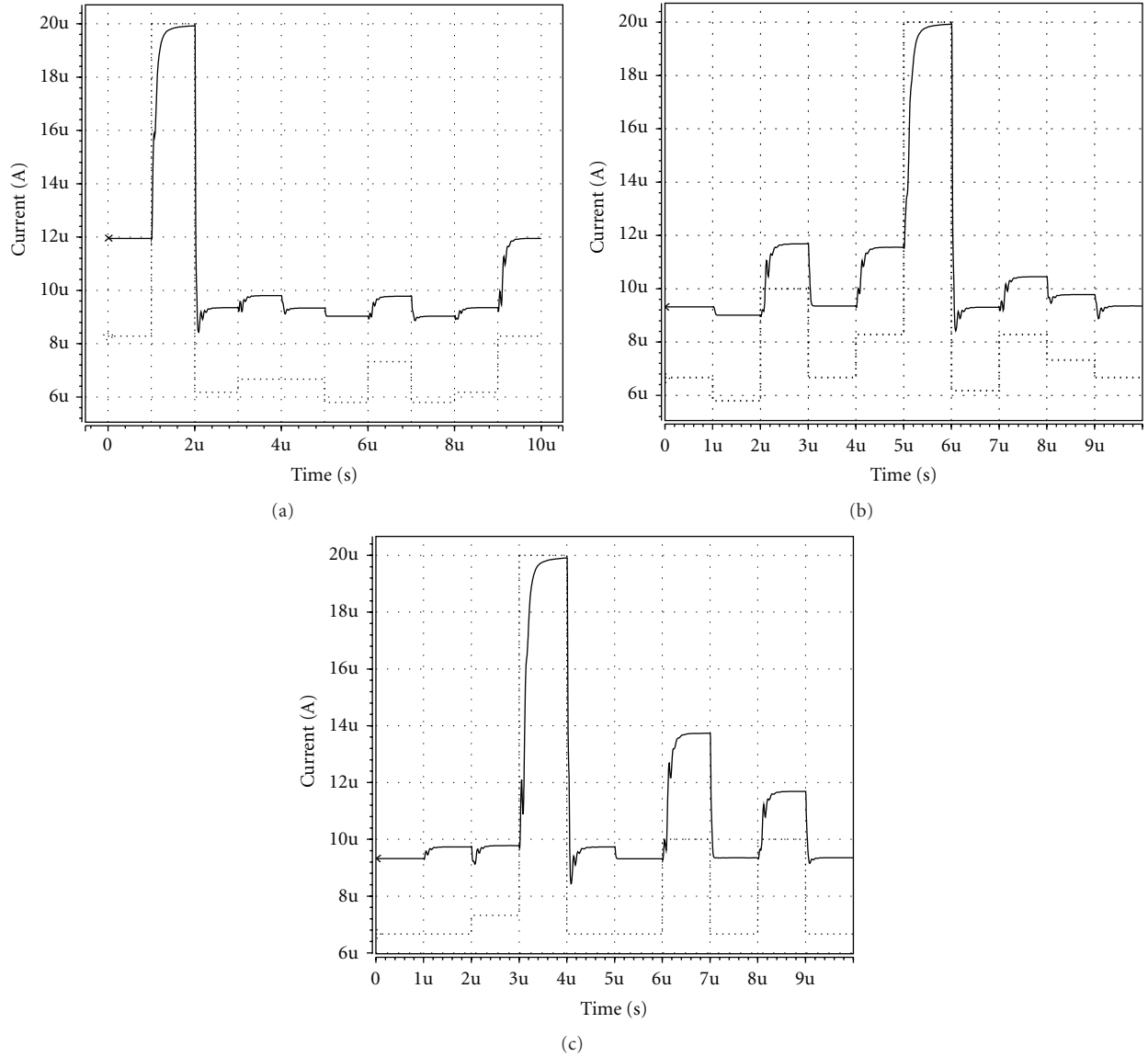


FIGURE 7: Time response of the Euclidean distance calculator circuit for input patterns of (a) U_1 , (b) U_2 and (c) U_3 .

TABLE 2: Comparison with former classifier circuits.

Parameter	Reference [2, 3]	Reference [4]	Reference [5]	Reference [7]	This work
Technology	0.6 μ	0.35 μ	0.5 μ	0.35 μ	0.18 μ
Supply voltage	$2V_{gs} + V_{ds}$ (3.3 V)	$2V_{gs} + V_{ds}$	$2V_{gs} + V_{ds}$ (3.3 V)	± 1.65	$V_{gs} + 2V_{ds}$ (0.9 V)
Power consumption	15 mW	Expected >10 mW	16 mW	0.66 mW	<1 mW
Error	1%	Not Reported	Not Reported	Not Reported	1%
Circuit complexity (transistor count)	>250	>50	>300	>200	144
Body effect	Yes	Yes	Yes	Yes	No
Input current operation area	1 Quad.	1 Quad.	1 Quad.	1 Quad.	2 Quad.

FIGURE 8: Time response of the membership degree calculator circuit for input patterns of (a) U_1 , (b) U_2 , and (c) U_3 .

zero that is for the pattern which is the exact input, and the most distant is 60 μ A for the pattern which all of its pixels has reverse color of the input pixels), but in fuzzy classifier of Figure 8 and to improve interpretability and simplify the decision system, a simple model of the membership

functions of (11) is employed that allows us to normalize Euclidean distance calculator which produces a membership degree with value of a constant normalized current signal $I_N (=20 \mu$ A) when the corresponding distance is zero, and produces zero membership degree when the corresponding

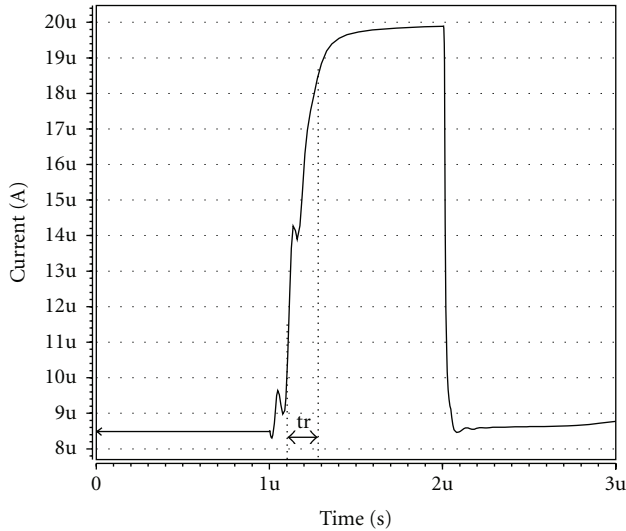


FIGURE 9: Time response for evaluate the rise time of the fuzzy classifier circuit.

distance approaches infinity (in this work and for the most distant of 60 uA will be 5 u). So, from the definition, the values of the functions sum up to $I_N (=20 \text{ uA})$.

The required time for recognizing a pattern in the circuit is defined as identification time and will be evaluated by maximum rise time/fall time of the calculator circuit [3]. Also, the error of the circuit is the relative error of the output current [4] and will be calculated by

$$\text{Relative error} = \frac{I_{\text{out}}(\text{theoretical}) - I_{\text{out}}(\text{simulated})}{I_{\text{out}}(\text{theoretical})} \quad (23)$$

for different input current patterns.

Employing Figure 9 to evaluate the speed of the fuzzy classifier circuit, the identification time has been calculated by estimating rise time for the worst possible case, in which the input pattern that in any slide of the time has the farthest possible from a template pattern and in the next slide time will switch to the closest possible template pattern (and vice versa for fall time estimation), and that shows the identification time of the proposed circuit is less than 250 ns. Also, to evaluate the precision, the relative error of the output current has been calculated by (20) for this worst possible case and also for different input current patterns, and results reveal that errors are less than 1%. In order to determine the temperature effect on the fuzzy classifier, Figure 8(a) is simulated for 7 different temperatures from -25°C to 125°C and for 25°C steps, which is depicted in Figure 10 (up to down with respect to these temperatures). Simulation results show that the maximum power consumption of the Euclidean distance calculator circuit is less than 1 mW. To provide more insight into the technique proposed here, a comparison was made with formerly reported current-mode classifier circuits in Table 2. So, performance of the proposed circuit has increased (a) because of decreasing stacked transistors compared to the preceding proposals [3–5], the minimum supply voltage of the circuit of Figure 4 is one V_{gs} plus two V_{ds} so, it can operates in lower supply

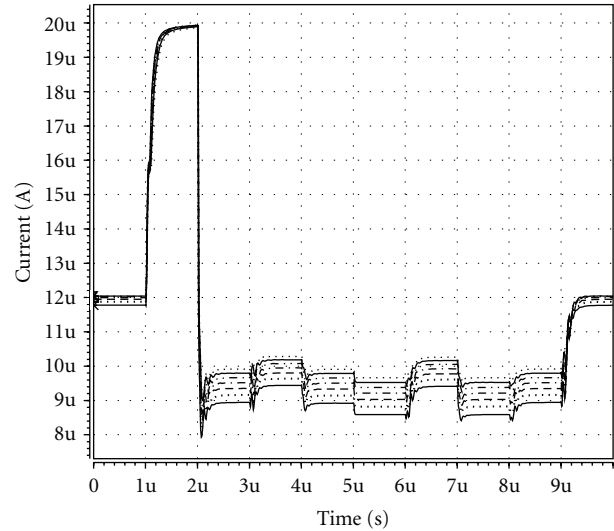


FIGURE 10: Temperature effect on the fuzzy classifier Figure 8(a) for 7 different temperatures from -25°C to 125°C and in 25°C steps (up to down with respect to these temperatures).

voltage, (b) from Figure 4, the sources of translinear MOS transistors of Figure 4 are connected to the substrate, so the circuit is immune from the body effect and (c) the input of the calculator of Figure 1 works in two quadrant, which lead to severely reducing the basic building blocks by eliminating the absolute and subtractor units compared to the other proposals [3–6]) Also, finally, the number of the transistors and power consumption of this circuit is less than the most of those reported before.

5. Conclusion

A new synthesis process for implementation fuzzy classification by using of a well-known Euclidean distance calculator is presented. The circuit was designed using transistors that operate in strong inversion. The application of the proposed method for template matching was described and verified by simulation. Simulation results demonstrate the functionality of the circuit and show the validity and suitability of the circuit for real-world, low-power, and low-supply voltage applications.

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