

Research Article

New Canonic Active RC Sinusoidal Oscillator Circuits Using Second-Generation Current Conveyors with Application as a Wide-Frequency Digitally Controlled Sinusoid Generator

Abhirup Lahiri^{1,2}

¹36-B, J and K Pocket, Dilshad Garden, Delhi, India

²Division of Electronics and Communications, Netaji Subhas Institute of Technology, University of Delhi, Delhi, India

Correspondence should be addressed to Abhirup Lahiri, lahiriabhirup@yahoo.com

Received 17 January 2011; Revised 22 March 2011; Accepted 29 April 2011

Academic Editor: Ali Umit Keskin

Copyright © 2011 Abhirup Lahiri. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

This paper reports two new circuit topologies using second-generation current conveyors (CCIIs) for realizing variable frequency sinusoidal oscillators with minimum passive components. The proposed topologies in this paper provide new realizations of resistance-controlled and capacitor-controlled variable frequency oscillators (VFOs) using only four passive components. The first topology employs three CCIIs, while the second topology employs two CCIIs. The second topology provides an advantageous feature of frequency tuning through two grounded elements. Application of the proposed circuits as a wide-frequency range digitally controlled sinusoid generator is exhibited wherein the digital frequency control has been enabled by replacing both the capacitors by two identical variable binary capacitor banks tunable by means of the same binary code. SPICE simulations of the CMOS implementation of the oscillators using 0.35 μm TSMC CMOS technology parameters and bipolar implementation of the oscillators using process parameters for NR200N-2X (NPN) and PR200N-2X (PNP) of bipolar arrays ALA400-CBIC-R have validated their workability. One of the oscillators (with CMOS implementation) is exemplified as a digitally controlled sinusoid generator with frequency generation from 25 kHz to 6.36 MHz, achieved by switching capacitors and with power consumption of 7 mW in the entire operating frequency range.

1. Introduction

Sinusoidal oscillators are very important analog circuits and find numerous applications in communication, control systems, signal processing, instrumentation, and measurement systems (see [1] and references cited therein). Since the advent of current conveyors, namely, the first-generation current conveyor (CCI) and the second-generation current conveyor (CCII) by Sedra and Smith in [2, 3], considerable attention has been given to the realizations of active RC sinusoidal oscillators using current conveyors (CCs). Several classes of CC-based sinusoidal oscillators have evolved depending on the number of passive components employed and the tuning laws. Oscillators using four passive components (including two resistors and two capacitors) are classified as canonic (or minimum passive component) oscillators and are suitable for realizing variable frequency oscillators

(VFOs) [4]. As pointed in [4], two of the most important tuning laws of the condition of oscillation (CO) and the frequency of oscillation (FO) for realizing canonic variable frequency oscillators (VFOs) are as follows.

Type1:

$$\text{CO: } C_1 = C_2, \quad (1)$$

$$\text{FO: } f_o = \frac{1}{2\pi} \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}. \quad (2)$$

Type2:

$$\text{CO: } R_1 = R_2, \quad (3)$$

$$\text{FO: } f_o = \frac{1}{2\pi} \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}. \quad (4)$$

It is clear from (1)–(4) that Type1 oscillators can provide frequency tuning by means of resistors R_1 and R_2 and Type2 oscillators can provide frequency tuning by means of capacitors C_1 and C_2 . Thus, both types of circuits are suitable to be used as VFOs. Since realizations of both voltage-controlled resistors and capacitors are known, both Type1 and Type2 circuits can be used as voltage-controlled oscillators (VCOs). Detailed references of the known oscillator circuits based on Type1 or Type2 tuning laws are provided in [4]. A very popular circuit for realizing VFO based on Type1 tuning law is reported in [5] (and its equivalent current-feedback op-amp-based version is reported in [6]). A reference apparently skipped in [4], that is [7], also discusses a modified variant of the circuit in [4]. Although not stated in [4], all the circuits in [4–7] (which are based on Type1 tuning law) can be transformed into oscillators with Type2 tuning law by simply using RC-CR transformation, that is, replace each resistor by capacitor and vice versa. The circuits in [8–11] also report minimum passive component CFOA oscillators with tuning laws other than Type1 and Type2 and with nonindependent CO and FO tuning laws. It should be pointed that the circuit in [10] is also minimum in terms of the number of active components. But such tuning laws (as in [8, 10]) are not very desirable as there is no independent term in the FO, and thus independent tuning of FO is impossible without simultaneously readjusting the CO. In a very recent communication [12], Fongsamut et al. proposed both Type1 and Type2 oscillators using two-X two-Z CCII and creating very compact realization of the oscillators.

This paper reports two new topologies for oscillators using two/three CCII, four passive components, and which can realize oscillators with both Type1 and Type2 tuning laws (using RC-CR transformation), thereby adding to the current literature on active RC oscillators. The topologies can also provide quadrature current/voltage outputs because of the use of lossless integrators/differentiators. The resulting circuits are suitable for monolithic integration since both bipolar and CMOS implementations of CCII (both positive and negative) are available. CCII+ is available as a commercial IC (e.g., AD844 [13]), and single current output CCII– can also be created using two CCII+ ICs [14], and this makes bread-board implementation of the circuit solutions using CCII simpler. An important advantage of one of the proposed topologies (and derived circuits) over those in [5, 6, 8, 12] is that both the frequency control elements (either resistors or capacitors) are grounded and which allows very easy electronic tunability (dual-element frequency control) by both analog and digital means. As an example, Type1 oscillators derived from this topology can have voltage-controlled FO by simply implementing resistors through MOSFETs working in triode region. Nonideal analysis of the circuit is briefed and sensitivity analysis is provided. The aim of the paper is also to provide application of the proposed circuits as a digitally controlled wide-frequency sinusoid generator. As an application of the circuit where FO is digitally controlled, the two grounded capacitors (and/or the two resistors) can be replaced by binary weighted programmable element banks controllable by external digital codes and thereby enabling variable frequency generation.

SPICE simulations of the CMOS implementation of the oscillator using $0.35\ \mu\text{m}$ TSMC CMOS technology parameters and bipolar implementation of the oscillators using process parameters for NR200N-2X (NPN) and PR200N-2X (PNP) of bipolar arrays ALA400-CBIC-R [15] have validated their workability. In the example, the circuit can be easily digitally tuned from 25 kHz to 6.36 MHz, a frequency range covering many clock generators (including crystal oscillators).

2. Proposed Circuit Topologies and Derived Oscillators

The first proposed circuit topology is shown in Figure 1(a). CCII is ideally characterized by the following equations:

$$V_y = V_x, \quad I_y = 0, \quad I_{z+} = -I_{z-} = I_x, \quad (5)$$

where the directions of the currents are in accordance with the network convention that all currents are flowing into the terminals. Using (5) and doing routine circuit analysis yields the following characteristic equation (CE) for this autonomous circuit topology:

$$Z_2Z_4 + Z_1Z_3 + Z_2Z_3 = Z_4Z_3. \quad (6)$$

The first oscillator circuit, shown in Figure 1(b), is derived by choosing the impedances as $Z_1 = 1/sC_1$, $Z_2 = R_2$, $Z_3 = 1/sC_3$, and $Z_4 = R_4$. With these impedances, (6) can be rewritten as

$$s^2C_1C_3R_2R_4 + sC_1(R_2 - R_4) + 1 = 0. \quad (7)$$

It is evident from (7) that the CO and the FO are given as

$$\text{CO: } R_2 \leq R_4, \quad (8)$$

$$\text{FO: } f_o = \frac{1}{2\pi} \sqrt{\frac{1}{C_1C_3R_2R_4}}. \quad (9)$$

It is clear from (8) and (9) that the FO can be independently varied (i.e., without disturbing the CO) via capacitors C_1 and C_3 . The second oscillator circuit, shown in Figure 1(c), is derived by simply applying RC-CR transformation on the first circuit, that is, choosing the impedances as $Z_1 = R_1$, $Z_2 = 1/sC_2$, $Z_3 = R_3$, and $Z_4 = 1/sC_4$; (6) can be rewritten as

$$s^2C_2C_4R_1R_3 + sR_3(C_4 - C_2) + 1 = 0. \quad (10)$$

It is evident from (10) that the CO and the FO are given as

$$\text{CO: } C_4 \leq C_2, \quad (11)$$

$$\text{FO: } f_o = \frac{1}{2\pi} \sqrt{\frac{1}{C_2C_4R_1R_3}}. \quad (12)$$

It is clear from (11) and (12) that the FO can be independently varied (i.e., without disturbing the CO) via resistors R_1 and R_3 , leading to resistance-controlled VFO. The circuits in Figures 1(b) and 1(c) are suitable for quadrature current output generation owing to the use of lossless integrators/differentiators. The currents flowing in the x terminals

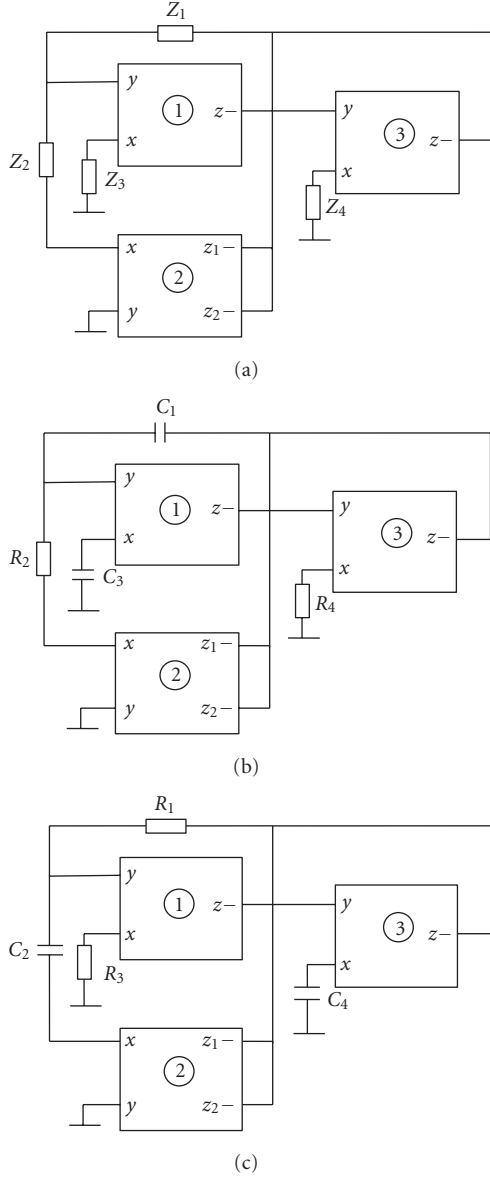


FIGURE 1: (a) First proposed circuit topology, (b) Type2 oscillator, and (c) Type1 oscillator.

of first and second CCII for both the circuits are quadrature in nature. These currents can be sensed out for explicit utilization by means of additional z terminals in the CCII.

The second proposed topology is shown in Figure 2(a) and employs two CCII. Using (5) and doing routine circuit analysis yields the following ideal CE for this autonomous circuit topology:

$$Z_2 Z_4 + Z_1 Z_2 + Z_1 Z_3 = Z_1 Z_4. \quad (13)$$

The first oscillator circuit, shown in Figure 2(b), is derived by choosing the impedances as $Z_1 = 1/sC_1$, $Z_2 = R_2$, $Z_3 = 1/sC_3$, and $Z_4 = R_4$. With these impedances, (13) can be rewritten as

$$s^2 C_1 C_3 R_2 R_4 + s C_3 (R_2 - R_4) + 1 = 0. \quad (14)$$

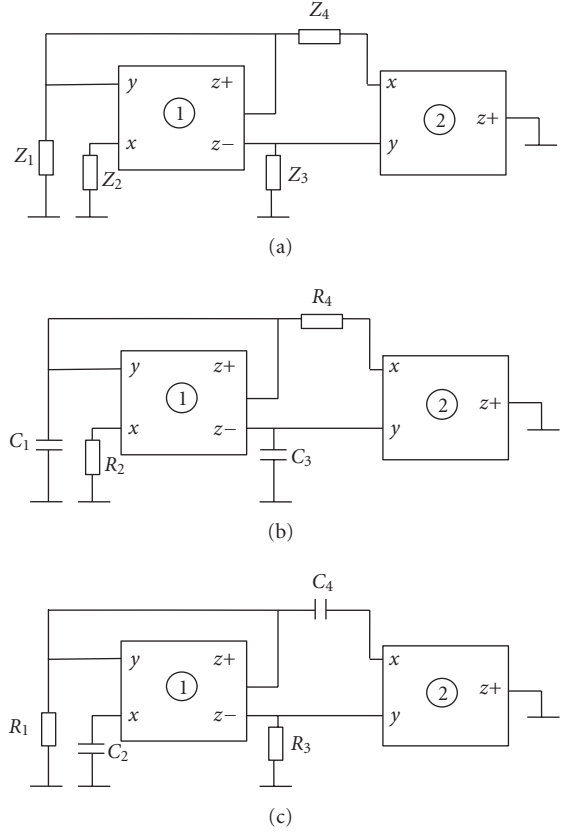


FIGURE 2: (a) Second proposed circuit topology, (b) Type2 oscillator, and (c) Type1 oscillator.

It is evident from (14) that the CO and the FO are given same as in (8) and (9), respectively—which is indicative of Type2 tuning law. The second oscillator circuit, shown in Figure 2(c), is derived by simply applying RC-CR transformation on the circuit in Figure 2(b), that is, choosing the impedances as $Z_1 = R_1$, $Z_2 = 1/sC_2$, $Z_3 = R_3$, and $Z_4 = 1/sC_4$; (13) can be rewritten as

$$s^2 C_2 C_4 R_1 R_3 + s R_1 (C_4 - C_2) + 1 = 0. \quad (15)$$

It is evident from (15) that the CO and the FO are the same as (11) and (12), respectively, which is indicative of Type1 tuning law. The circuits in Figures 2(b) and 2(c) are also suitable for quadrature voltage generation owing to the use of lossless integrators/differentiators. The voltages at x and z terminals of the first CCII for both the circuits are quadrature in nature and given as follows:

For Figure 2(b),

$$V_{z-} = \frac{-1}{j\omega_o C_3 R_2} V_x. \quad (16)$$

for Figure 2(c),

$$V_{z-} = -j\omega_o C_3 R_3 V_x. \quad (17)$$

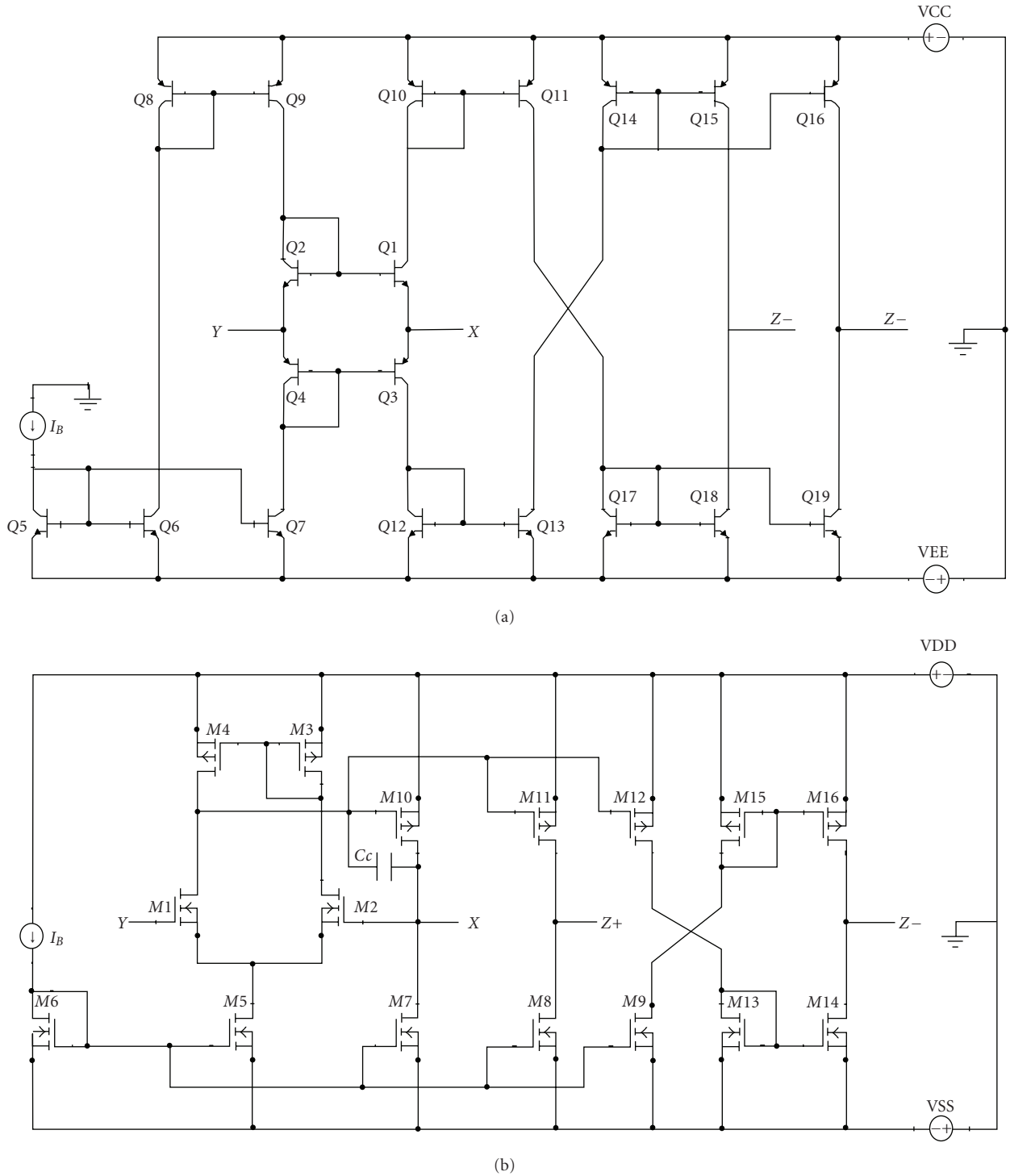


FIGURE 3: Possible (a) bipolar implementation of dual-output CCII- and (b) MOSFET implementation of complimentary output CCII.

3. Nonideal Analysis

Considering the nonidealities that arise from the actual physical implementation of the circuit, the characterizing equation of the CCII in (1) is rewritten as

$$V_y = \alpha V_x, \quad I_y = 0, \quad |I_{z\pm}| = \beta I_x, \quad (18)$$

where α represents the voltage gain from y to x terminal, and β represents the current gain from x to z . According to [16, 17], these gains can be modeled as first-order transfer functions

$$\alpha = \frac{\alpha_0}{1 + s/\omega_\alpha}, \quad \beta = \frac{\beta_0}{1 + s/\omega_\beta}, \quad (19)$$

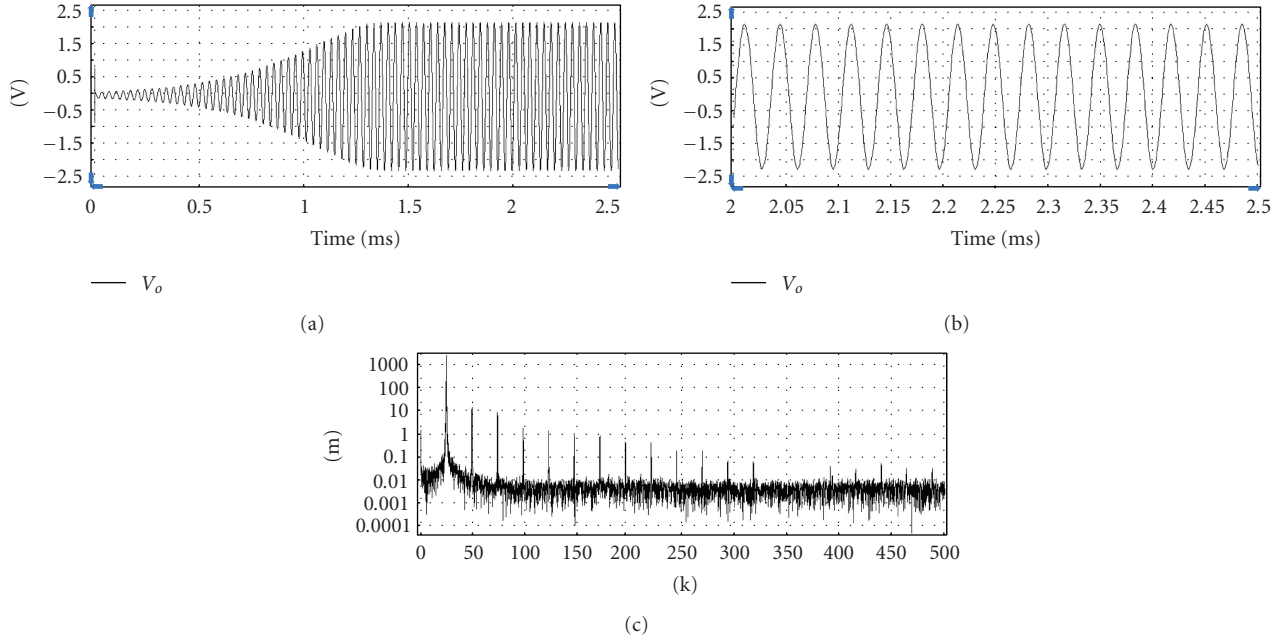


FIGURE 4: Oscillator in Figure 1(b): (a) startup of oscillations, (b) steady-state waveform, and (c) magnitude spectrum.

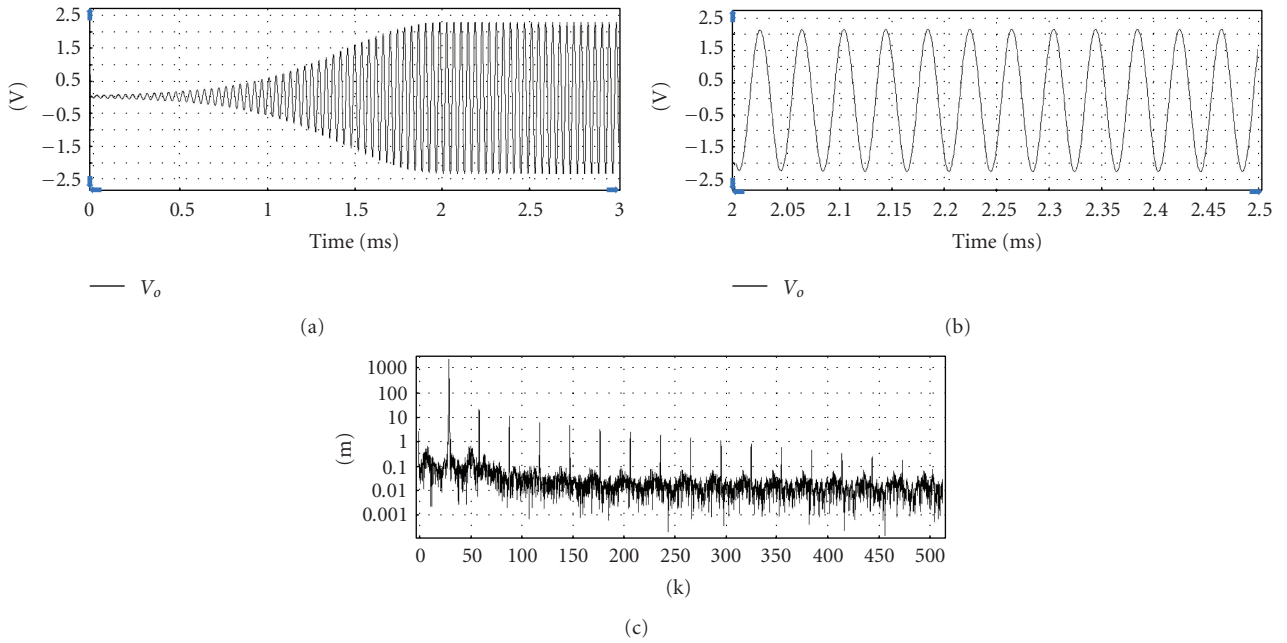


FIGURE 5: Oscillator in Figure 1(c): (a) startup of oscillations, (b) steady-state waveform, and (c) magnitude spectrum.

where α_0 and β_0 represent the DC transfer gains. We consider the operating frequencies much less than those of the angular pole frequencies, ω_α and ω_β , and hence, we can approximate $\alpha \approx \alpha_0$ and $\beta \approx \beta_0$. Apart from this, there exists a nonzero parasitic resistance at terminal x which comes in series with the external impedance at x terminal. We analyze the nonideal behavior of the first topology here, and the nonideal analysis of second topology can also be done similarly (arriving at similar conclusions). For circuit

in Figure 1(b), R_x for the second and third CCII is absorbed into external resistors, R_2 and R_3 , respectively (this requires external resistors to be of much larger value than R_x , so that frequency deviation from the ideal value in (9) and (12) can be minimized). But for the first CCII, R_x comes in series with the external capacitor. To alleviate its affect, the operating angular FO should be chosen such that $\omega_o \ll 1/R_{x1}C_3$. Similarly, for circuit in Figure 1(c), R_x for the first CCII is absorbed into external resistor R_3 , and the operating angular

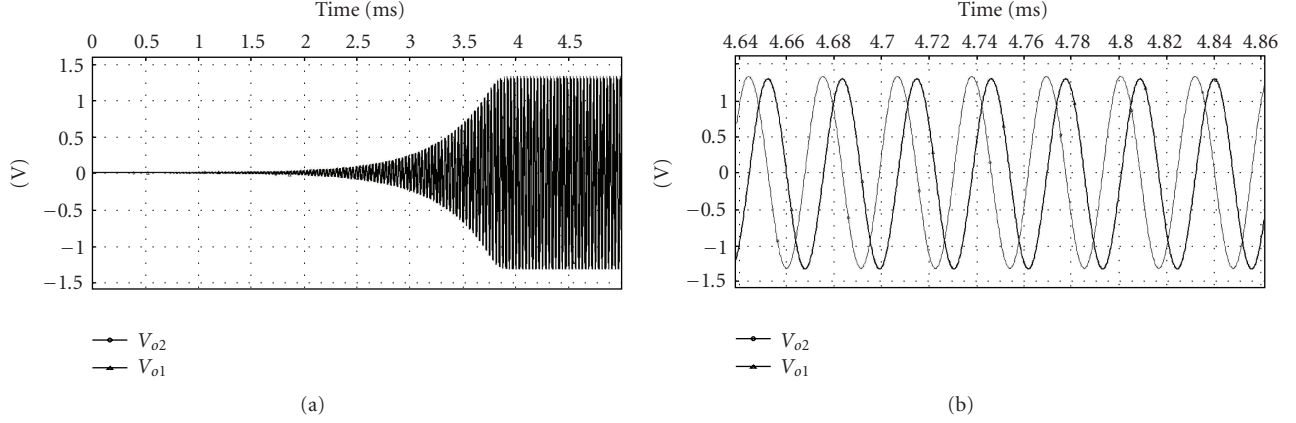


FIGURE 6: Quadrature oscillator in Figure 2(b): (a) startup of oscillations and (b) steady-state waveforms.

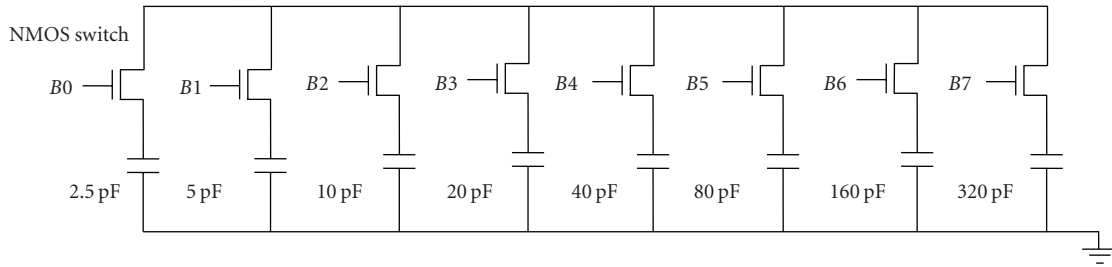


FIGURE 7: Binary-weighted programmable capacitor bank.

FO should be chosen such that $\omega_o \ll \min(1/R_{x2}C_2, 1/R_{x3}C_4)$. Considering the active element nonidealities as indicated in (18), the CE in (6) is modified to

$$\alpha_1\beta_1Z_2Z_4 + \alpha_3\beta_3(Z_1Z_3 + Z_2Z_3) = Z_4Z_3((\beta_{21} + \beta_{22}) - 1). \quad (20)$$

The modified CO and FO for Type2 circuit, shown in Figure 2(b), are given as

$$\text{CO: } \alpha_3\beta_3R_2 \leq R_4((\beta_{21} + \beta_{22}) - 1), \quad (21)$$

$$\text{FO: } f_o = \frac{1}{2\pi} \sqrt{\frac{\alpha_3\beta_3}{\alpha_1\beta_1C_1C_3R_2R_4}}. \quad (22)$$

Equation (21) and (22) provide very useful results. It is clear that even in the nonideal case, the FO can be independently tuned via capacitors C_1 and C_3 . Also, since voltage and current gains appear both in the numerator and denominator in the FO, their effect on FO is minimized (their effect on FO can be nullified if $\alpha_3\beta_3 = \alpha_1\beta_1$). Similarly, the modified CO and FO for Type1 circuit, shown in Figure 2(c), are given as

$$\text{CO: } C_4 \leq C_2((\beta_{21} + \beta_{22}) - 1), \quad (23)$$

$$\text{FO: } f_o = \frac{1}{2\pi} \sqrt{\frac{\alpha_1\beta_1}{\alpha_3\beta_3C_2C_4R_1R_3}}. \quad (24)$$

It is clear from (23) and (24) that even in the nonideal case, the FO can be independently tuned via resistors R_1 and R_3 ,

and the effect of voltage and current gains on the FO can be nullified if $\alpha_3\beta_3 = \alpha_1\beta_1$. The sensitivity analyses from (17) and (19), for both the oscillators, indicate that

$$\left| S_{\alpha_1, \beta_1, \alpha_3, \beta_3, R_i, C_j}^{f_o} \right| = \frac{1}{2} \quad \text{where } i, j = 1, 2. \quad (25)$$

4. Simulation Results

The proposed circuits have been verified using SPICE simulations. Both the CMOS implementation of the oscillator using 0.35 μm TSMC CMOS technology parameters and the bipolar implementation using process parameters for NR200N-2X (NPN) and PR200N-2X (PNP) of bipolar arrays ALA400-CBIC-R from AT & T [15] have been worked. This section provides some design examples that have been implemented. The Type2 oscillator in Figure 1(b) is designed using bipolar implementation of the CCII as shown in Figure 3(a), with $\pm 3\text{ V}$ supply and passive components values: $C_1 = C_3 = 600\text{ pF}$, $R_2 = 10\text{ k}\Omega$, and $R_4 = 11.8\text{ k}\Omega$. The startup of oscillations, the steady-state waveform, and magnitude spectrum of the voltage signal at terminal y of third CCII are shown in Figures 4(a), 4(b), and 4(c), respectively. The total harmonic distortion (THD) of the generated voltage signal is 0.72%, and the simulated FO is 24.578 kHz as compared to the theoretical FO of 24.419 kHz. Similarly, the Type1 oscillator in Figure 1(c) is designed using bipolar implementation and using these passive components values: $R_1 = R_3 = 10\text{ k}\Omega$, $C_4 = 500\text{ pF}$, and $C_2 = 600\text{ pF}$. The startup of oscillations, the steady-state waveform, and magnitude

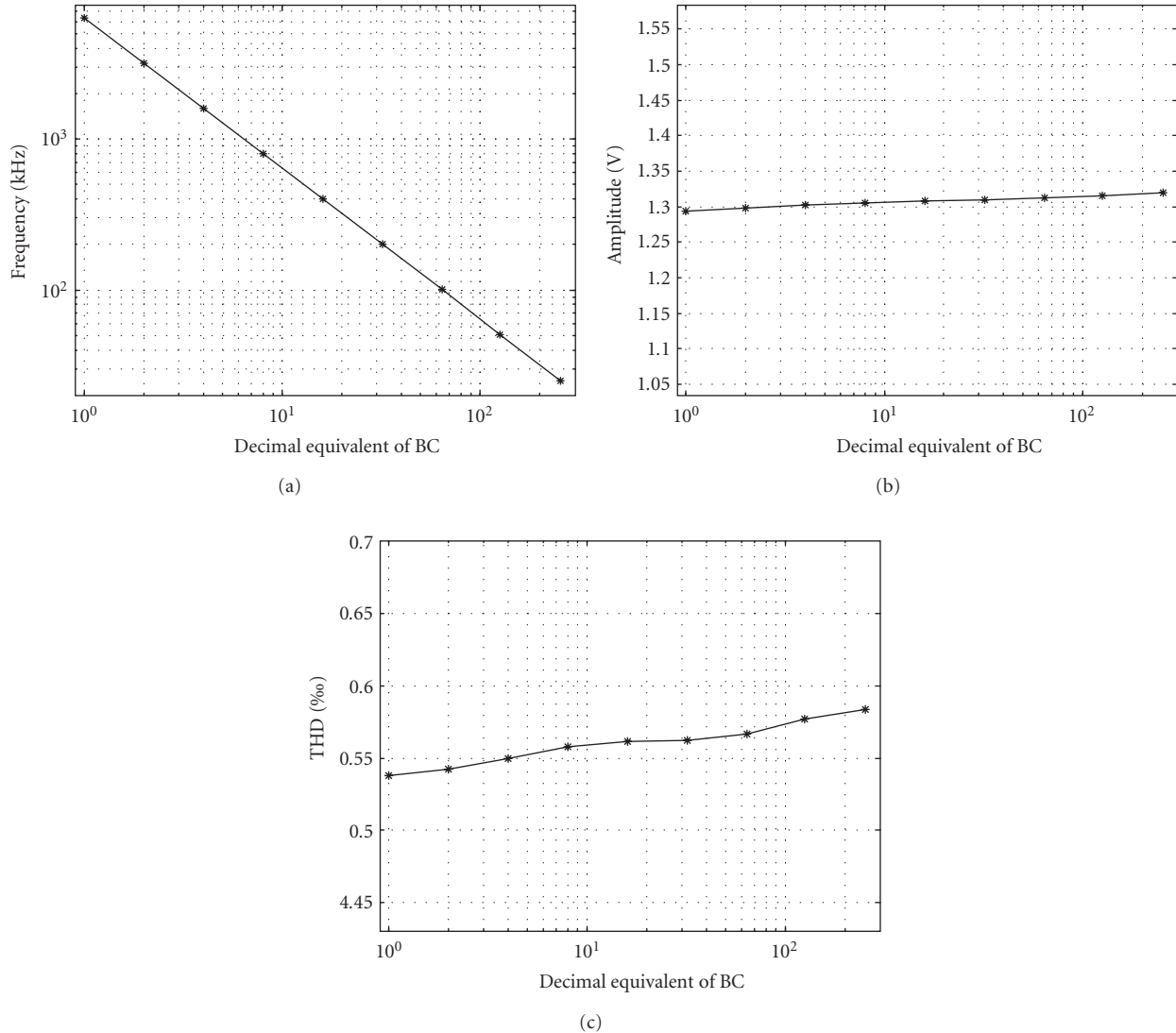


FIGURE 8: (a) FO tuning, (b) amplitude variation, and (c) THD variation, with changing BC.

spectrum of the voltage signal at terminal y of third CCII are shown in Figures 5(a), 5(b), and 5(c), respectively. The total harmonic distortion (THD) of the generated voltage signal is 0.94% and the simulated FO is 29.338 kHz as compared to the theoretical FO of 29.057 kHz. It should be noted that no external auxiliary amplitude control circuitry is used to stabilize the oscillation amplitude, and the amplitude is inherently limited due to the nonlinearity of the active device. Alternatively, automatic amplitude control loops can be employed to achieve tighter THD specification even with larger startup margin. The circuit in Figure 2(b) is designed using a possible MOSFET implementation of CCII, as shown in Figure 3(b), with ± 2.5 V supply. The aspect ratios of the transistors are indicated in Table 1 and the biasing current $I_B = 100$ μ A. With the passive component values chosen as $R_2 = 10$ k Ω , $R_1 = 9.8$ k Ω , and $C_1 = C_2 = 500$ pF, the startup of oscillations and the steady-state waveforms for both the quadrature voltage signals are shown in Figures 6(a) and 6(b), respectively (where V_{o1} and V_{o2} are the voltages

at x and z , terminal of the first CCII). The observed frequency of 149 kHz is in close correspondence with the theoretical value of 159.1 kHz, and the THD at both the outputs is less than 0.6%. For digitally controlled frequency generation, both the capacitors C_1 and C_3 are replaced by binary-weighted programmable capacitors banks (shown in Figure 7) controllable by external digital codes. The capacitor bank consists of eight binary-weighted capacitors with the minimum capacitor value of 2.5 pF (corresponding to LSB), and an eight-bit binary code (BC) [$B_0 B_1 \dots B_7$] is used to control the effective capacitance. The BC can take any value from [10000000] to [11111111], that is, the minimum capacitance of the bank is 2.5 pF, and the maximum capacitance is 637.5 pF. The FO tuning curve with changing BC is shown in Figure 8(a), where the X-axis represents the decimal equivalent of the BC. The FO tuning achieved by this capacitor bank is from 25 kHz to 6.36 MHz, and the power consumption does not exceed 7 mW for the entire frequency range. The variation of the amplitude of oscillation

TABLE 1: Transistors widths for CCII.

MOSFET	W/L ($\mu\text{m}/\mu\text{m}$)
M1-M2	10/0.35
M3-M4-M5-M15-M16	6/1
M7-M8-M9	12/1
M10-M11-M12	12/1
M13-M14	3/1

(at the x terminal of the first CCII) and the THD with changing BC (i.e., changing FO) is shown in Figures 8(b) and 8(c), respectively.

5. Concluding Remarks

This paper reports two new CCII-based oscillator topologies that add to the current catalog of minimum passive component active-RC oscillators. A new topology with grounded frequency tuning elements is presented, and oscillators with frequency control via both resistor and capacitor are realized using the proposed topologies. SPICE simulation results using both the bipolar and CMOS implementation of the circuits have verified their workability. Application of the proposed circuit as a wide-frequency range digitally controlled sinusoid generator is also demonstrated.

Acknowledgments

The author would like to thank the anonymous reviewers for useful suggestions and comments, which helped to improve the paper substantially. The author is also grateful to Dr. Ali Umit Keskin, the associate editor of Active and Passive Electronic Components Journal, for enabling the prompt review of the paper. Part of this work was done while the author was with the Division of Electronics and Communications, Netaji Subhas Institute of Technology, University of Delhi, Delhi, India.

References

- [1] W. Tangsrirat, D. Prasertsom, T. Piyatat, and W. Surakampon-torn, "Single-resistance-controlled quadrature oscillator using current differencing buffered amplifiers," *International Journal of Electronics*, vol. 95, no. 11, pp. 1119–1126, 2008.
- [2] K. C. Smith and A. Sedra, "The current conveyor: a new circuit building block," *IEEE Proceedings*, vol. 56, no. 8, pp. 1368–1369, 1968.
- [3] A. Sedra and K. C. Smith, "A second-generation current conveyor and its application," *IEEE Transactions on Circuit Theory*, vol. 17, no. 1, pp. 133–134, 1970.
- [4] A. Lahiri, "Current-mode variable frequency quadrature sinusoidal oscillators using two CCs and four passive components including grounded capacitors," *Analog Integrated Circuits and Signal Processing*, pp. 1–9, 2010.
- [5] J. W. Horng, "A sinusoidal oscillator using current-controlled current conveyors," *International Journal of Electronics*, vol. 88, no. 6, pp. 659–664, 2001.
- [6] D. R. Bhaskar and R. Senani, "New CFOA-based single-element-controlled sinusoidal oscillators," *IEEE Transactions*

- on Instrumentation and Measurement*, vol. 55, no. 6, pp. 2014–2021, 2006.
- [7] N. Pandey, S. K. Paul, and A. Bhattacharya, "Sinusoidal oscillator a new configuration based on current conveyor," in *Proceedings of the XXVII General Assembly of International Union of Radio Science*, Delhi, India, 2005.
- [8] M. T. Abuelma'atti and S. M. Al-Shahrani, "A minimum component grounded-capacitor CFOA-based RC oscillator," *Active and Passive Electronic Components*, vol. 19, no. 4, pp. 247–251, 1997.
- [9] A. M. Soliman, "Current feedback operational amplifier based oscillators," *Analog Integrated Circuits and Signal Processing*, vol. 23, no. 1, pp. 45–55, 2000.
- [10] M. T. Abuelma'atti, "Two minimum component CCII-based RC oscillators," *IEEE Transactions on Circuits and Systems*, vol. 34, no. 8, pp. 980–981, 1987.
- [11] M. T. Abuelma'ati, "New two CFOA-based sinusoidal RC oscillators with buffered outlet," *Analog Integrated Circuits and Signal Processing*, vol. 66, no. 3, pp. 475–482, 2010.
- [12] C. Fongsamut and W. Surakampon-torn, "Minimal realization for single-element-controlled sinusoidal oscillators using single current conveyor," in *Proceedings of the International Symposium on Communications and Information Technologies (ISCIT '10)*, pp. 196–199, Tokyo, Japan, 2010.
- [13] *Linear Products Data Book*, Analog Devices, Norwood, Mass, USA, 1990.
- [14] A. M. Soliman, "Synthesis of grounded capacitor and grounded resistor oscillators," *Journal of the Franklin Institute*, vol. 336, no. 4, pp. 735–746, 1999.
- [15] D. R. Frey, "Log-domain filtering: an approach to current-mode filtering," *IEE Proceedings—G*, vol. 140, no. 6, pp. 406–416, 1993.
- [16] B. Metin and K. Pal, "Cascadable allpass filter with a single DO-CCII and a grounded capacitor," *Analog Integrated Circuits and Signal Processing*, vol. 61, no. 3, pp. 259–263, 2009.
- [17] A. Fabre, O. Saaid, and H. Barthelemy, "On the frequency limitations of the circuits based on second generation current conveyors," *Analog Integrated Circuits and Signal Processing*, vol. 7, no. 2, pp. 113–129, 1995.



Hindawi

Submit your manuscripts at
<http://www.hindawi.com>

