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*Research Article*

# A Generic Current Mode Design for Multifunction Grounded Capacitor Filters Employing Log-Domain Technique

**N. A. Shah and F. A. Khanday**

*Department of Electronics and Instrumentation Technology, University of Kashmir, Srinagar 190 006, India*

Correspondence should be addressed to F. A. Khanday, farooqsnn20@yahoo.co.in

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A generic design (GD) for realizing an *n*th order log-domain multifunction filter (MFF), which can yield four possible stable filter configurations, each offering simultaneously lowpass (LP), highpass (HP), and bandpass (BP) frequency responses, is presented. The features of these filters are very simple, consisting of merely a few exponential transconductor cells and capacitors; all grounded elements, capable of absorbing the shunt parasitic capacitances, responses are electronically tuneable, and suitable for monolithic integration. Furthermore, being designed using log-domain technique, it offers all its advantages. As an example, 5th-order MFFs are designed in each case and their performances are evaluated through simulation. Lastly, a comparative study of the MFFs is also carried, which helps in selecting better high-order MFF for a given application.

## 1. Introduction

The popularity attributed to the use of continuous-time filters in ever growing wireless industry is their effective handling of high-frequency real-world signals and low-power systems. But the integration of continuous-time filters and digital circuits on the same IC needs reduction in supply voltage which entails increase in the power consumption of conventional analog signal processors for conservation of same dynamic range (DR) and chip area for a given bandwidth [1]. To circumvent this limitation, the use of companding-based signal processors was proposed [2, 3], which comprises compression block, for converting linear input current into compressed voltage; a core processor, for the production of corresponding compressed output voltage and an expansion block, for the conversion of nonlinear output voltage to a linear output current.

The use of logarithmic and exponential functions in the development of log-domain filters permits them to operate on very low supply voltage without sacrificing the dynamic range [4]. These filters also contain low impedance nodes along the signal path, facilitating the achievement of greater bandwidths. Thus, due to these advantages, log-domain filters are receiving interest in literature, and substantial progress has been made in simplifying the processes of analysis and synthesis for such circuits [5–13].

The implementation of filters with multifunction feature finds applications in phase-locked loops, FM stereo demodulator, touch-tone telephone tone decoder, and crossover network used in three-way high-fidelity loudspeakers [14]. Therefore, it is imperative to have such type of filters in log-domain as well. Owing to strenuous efforts, some low-order log-domain MFFs have been reported [15–18], and research in the design of high-order log-domain MFFs continues to be an area of endeavour [19], though conventional integrated high-order filter design with multifunction feature have been reported in [20–22]. The method presented in [20] is based on the cascading of low-order filters with the exchange of input and ground terminals. The cascading result in the use of excessive number of components [21] and the exchange of input and ground terminals is tedious. For high-order design, each time low-order filters are cascaded, the number of components required also increases by the same measure. As a sequel, the design leads to increase in circuit complexity, volume, noise, parasitic effects, and power dissipation, for both IC and discrete designs. In [21], simultaneous outputs

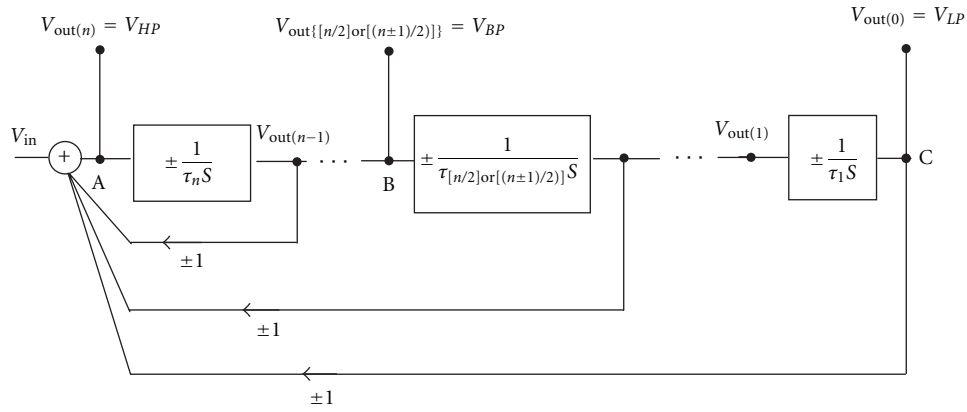



Figure 1: GFBD of the proposed generic $n$th order MFF topology.

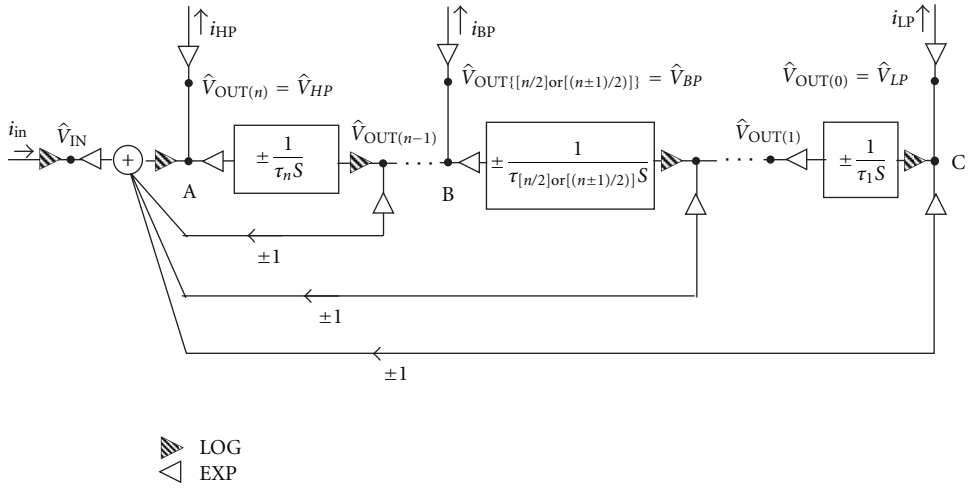



Figure 2: Transposed topology of the filter in Figure 1 into log domain.

are available for different filter functions but for BP filter function only even order can be implemented. Besides, in the general block diagram of the multifunction filter, the order of the feedbacks to be taken for a particular order is not clearly stated. In [22], a general method for simultaneous realization of various filter functions is discussed but involves complex mathematics. Besides, voltage buffers are required at the output to avoid loading effects.

Based on the above facts, a simple generic $n$th order MFF topology is introduced in this manuscript. From this topology, four different stable $n$th order MFF circuits can be constructed which can be implemented using lossless integrators, algebraic summation blocks, and appropriate feedback paths. Each configuration obtained from the generic topology simultaneously offers LP, HP, and BP frequency responses. The proposed generic topology enjoys the following advantages: (i) no restriction on the order of the filter (i.e., $n$ can be even or odd), (ii) modularity of filter structure is ensured being exclusively lossless integrator based, (iii) permit electronic adjustment of frequency characteristics, (iv) suitable for monolithic integration, (v) circuit complexity and noise are reduced [19].

It is worth to point out here that the high-order log-domain MFF of [19] turn out to be one of the configurations of the proposed generic MFF design which, based on the type of integrators, their order of sequence and type of feedback, can yield as many as four different stable filter configurations. Besides, it has been demonstrated that each design has different performances depending on choice of parameters. The comparative study presented in this paper will facilitate the selection of a particular MFF design in accordance with the requirements of a given application.

## 2. Proposed Generic MFF Topology

The general transfer function of $n$th order HP filter function is as follows:

$$\frac{V_{out(n)}(s)}{V_{in}(s)} = \frac{b_n s^n}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + b_0}, \quad (1)$$

where $b_i$ $(i = 0, 1, 2, \ldots, n)$ determine the pole locations.

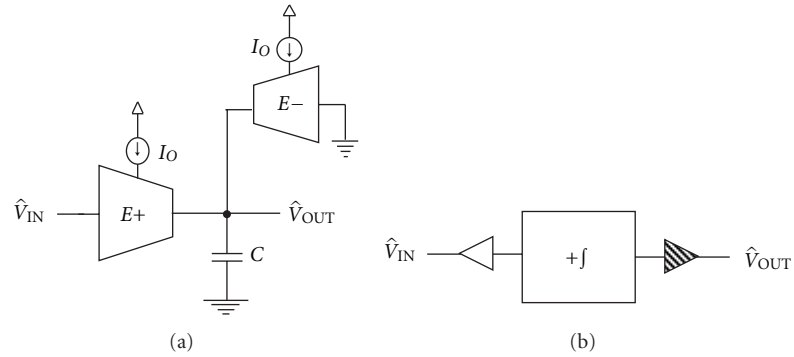



Figure 3: (a) Lossless DC stabilized log-domain noninverting integrator. (b) The employed symbol.

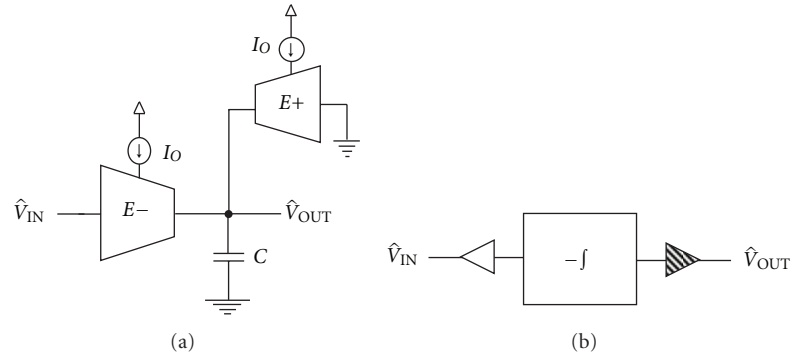



Figure 4: (a) Lossless DC stabilized log-domain inverting integrator. (b) The employed symbol.

Algebraic manipulations yield

$$\frac{V_{\text{out}(n)}(s)}{V_{\text{in}}(s)} = \frac{1}{1 \pm \{1 \pm \{1 \pm \cdots \pm \{1 \pm \{1 \pm 1/(\tau_n s)\} 1/(\tau_{n-1} s)\ \} \cdots \} 1/(\tau_2 s)\} 1/(\tau_1 s)}, \tag{2}$$

where time constant of $j$th integrator is $\tau_j = b_{n-j+1}/b_{n-j}$ ($j = 1, \ldots, n$).

The generic functional block diagram (GFBD) of the $n$th order HP filter topology obtained from (2) is given in Figure 1. An examination of Figure 1 reveals that it consists of lossless integrators, arranged one after the other with feedbacks from their outputs to the summation block. Depending on the type of integrator, their order of sequence and type of feedback, as many as four stable $n$th order MFF filter configurations, can be obtained from GFBD which are discussed hereunder:

$n$th *order filter topology MFF1:* Noninverting lossless integrator followed by inverting lossless integrator with positive and negative feedbacks from their respective outputs.

$n$th *order filter topology MFF2 [19]:* Noninverting lossless integrators are arranged one after the other with negative feedbacks from their outputs.

$n$th *order filter topology MFF3:* Inverting lossless integrator and Noninverting lossless integrator arranged one after the other with positive feedbacks from their outputs.

$n$th *order filter topology MFF4:* Inverting lossless integrators are arranged one after the other with positive and negative feedbacks taken alternately from their outputs.

The filter functions HP, BP, and LP being in conformity with (2) are respectively available at nodes A, B, and C of Figure 1. The former response is obtainable at the output of the summation block while latter responses can be, respectively, obtained by integrating (1) $n/2$ or $(n \pm 1)/2$-times and $n$-times. The derived general transfer function of LP response is as follows:

$$\frac{V_{\text{out}(0)}(s)}{V_{\text{in}}(s)} = \frac{\pm b_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + b_0}. \tag{3}$$

For BP filter function, symmetrical and asymmetrical responses are, respectively, available at the output of $n/2$th integrator and $\{(n+1)/2\}$th or $\{(n-1)/2\}$th integrator corresponding to $n$ either being even or odd. The derived transfer

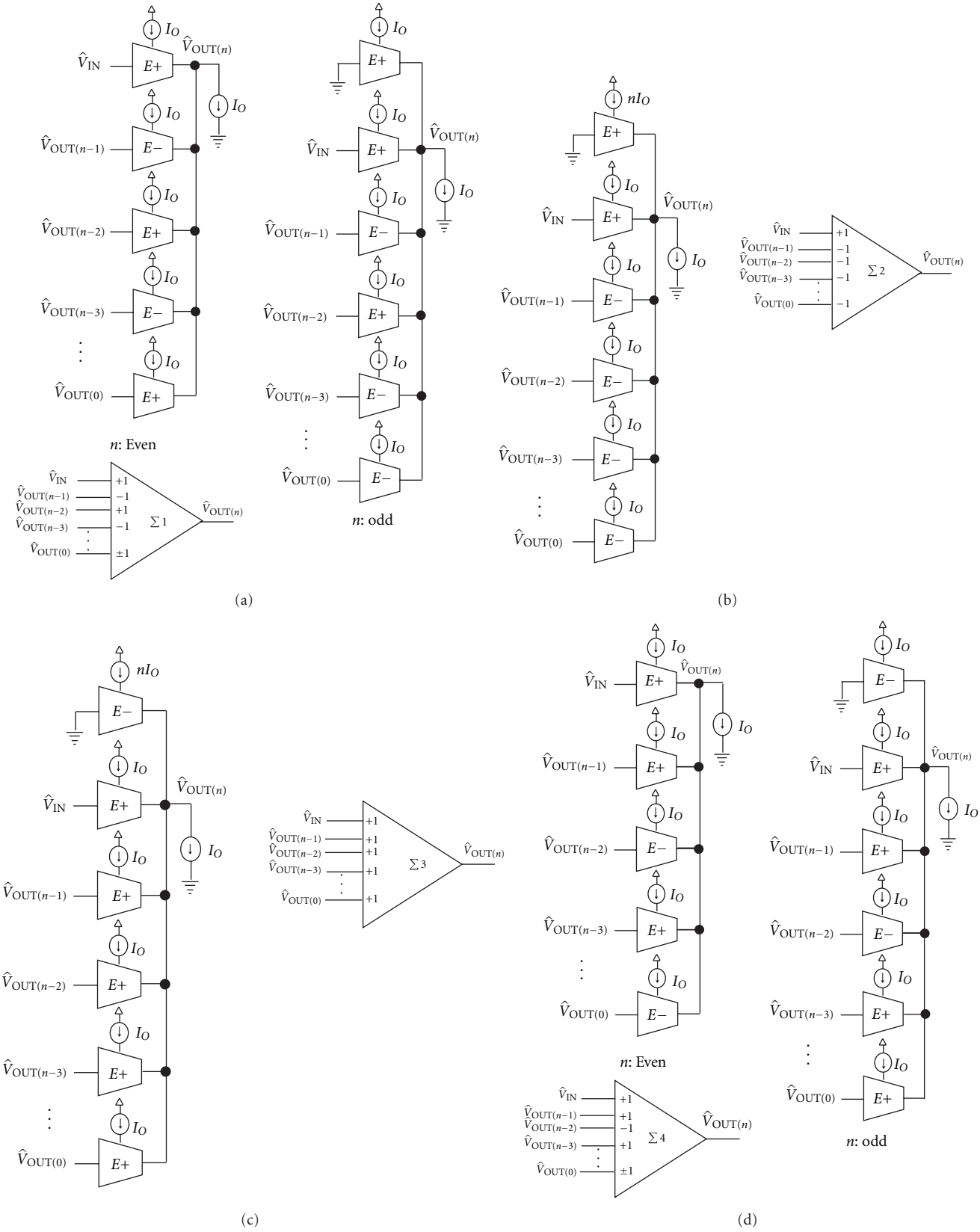



Figure 5: Multipleinput algebraic summation block (for even and odd order) and the employed symbol in all cases. (a) MFF1 (b) MFF2 (c) MFF3 (d) MFF4.

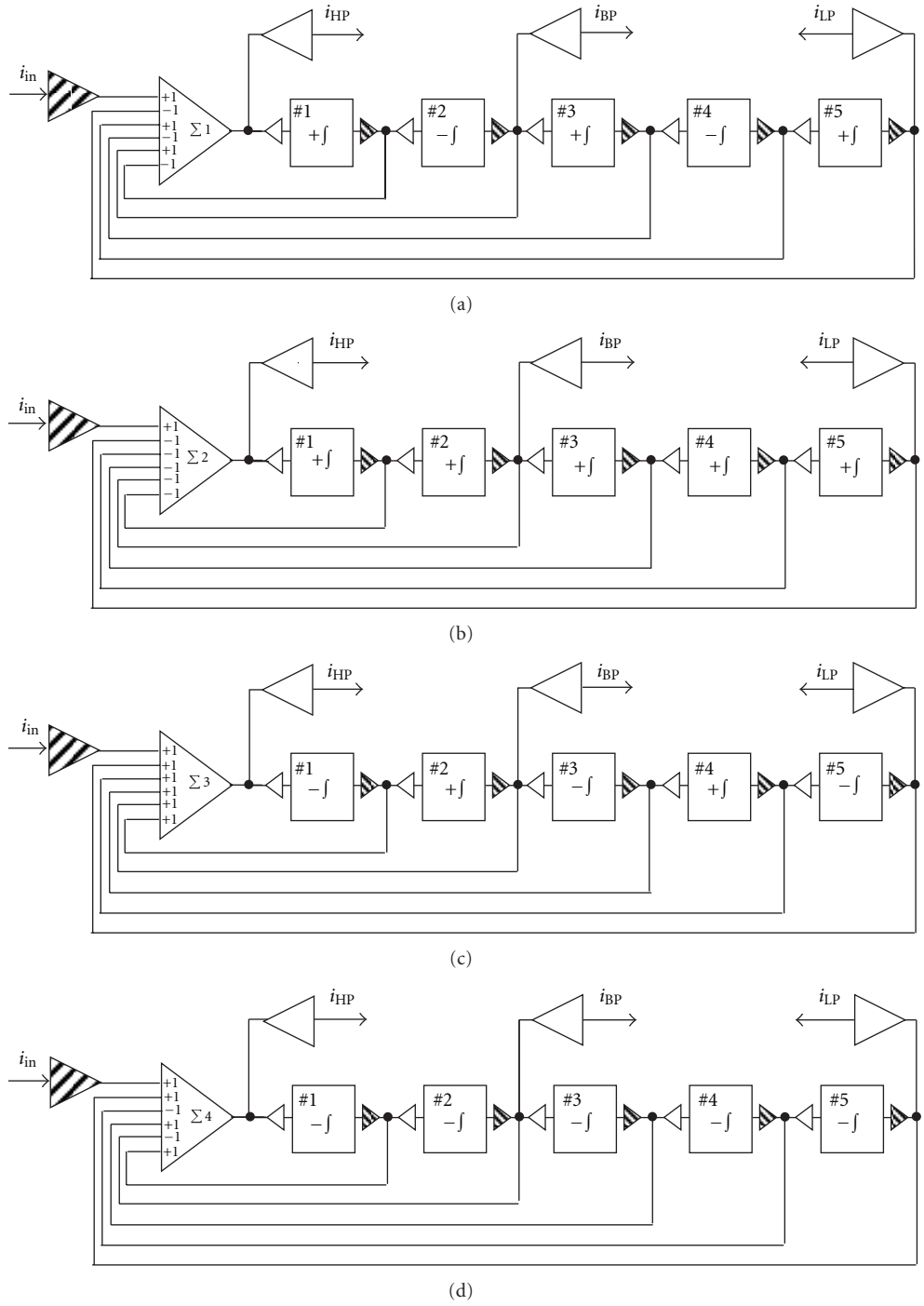



Figure 6: Topologies of the 5th-order generic log-domain MFF of Figure 2. (a) MFF1 (b) MFF2 (c) MFF3 (d) MFF4.

functions of symmetrical and asymmetrical responses for each of the configurations are as follows:

$$\frac{V_{\text{out}(n/2)}(s)}{V_{\text{in}}(s)} = \frac{\pm b_{n/2}s^{n/2}}{b_n s^n + b_{n-1}s^{n-1} + \cdots + b_1 s + b_0}, \quad (4)$$

$$\frac{V_{\text{out}(n\pm1)/2}(s)}{V_{\text{in}}(s)} = \frac{\pm b_{(n\pm1)/2}s^{(n\pm1)/2}}{b_n s^n + b_{n-1}s^{n-1} + \cdots + b_1 s + b_0}. \quad (5)$$

The order of the filter and its configuration determines the noninverting or inverting mode of the transfer function as summarised in Table 1. In addition, the four MFF configurations presented above are the only achievable stable designs from the generic design as is demonstrated for the 2nd order in Table 2.

To transpose GFBD to its log-domain counterpart, an appropriate set of complementary LOG and EXP operators

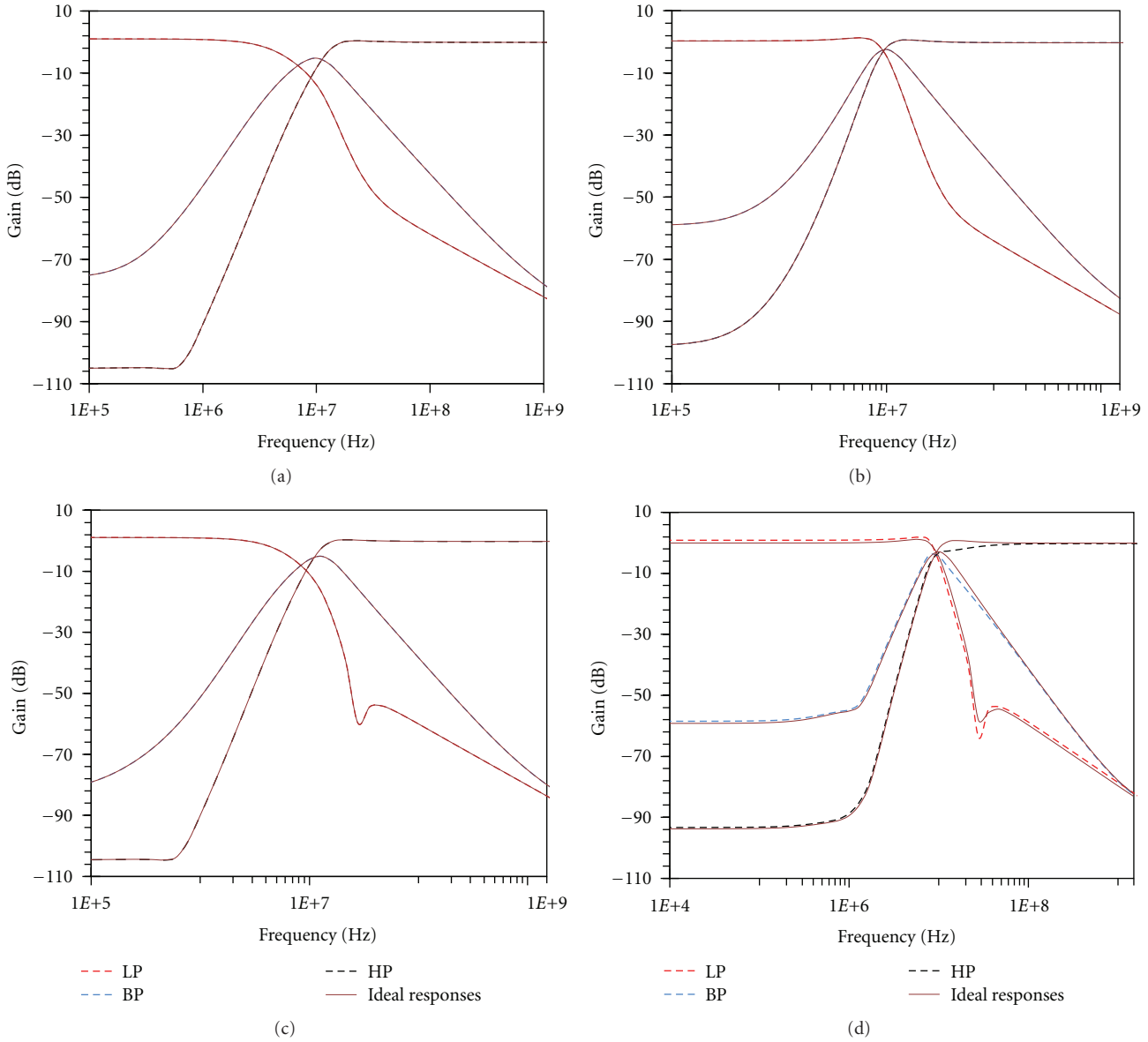



Figure 7: Simulated magnitude responses of standard filter functions of MFFs of Figure 6. (a) MFF1 (b) MFF2 (c) MFF3 (d) MFF4.

are required, which are, respectively, given by [12]

$$\hat{V} = \mathrm{LOG}(i) = V_T ln\left(\frac{i + I_O}{I_O}\right), \tag{6}$$

$$i = \mathrm{EXP}\left(\hat{V}\right) = I_O e^{(\hat{V}/V_T)} - I_O, \tag{7}$$

where $\hat{V}$ and $V_T$, respectively, represent the base-emitter voltage and thermal voltage of BJT, $I_O$ is the bias current, and circumflex ($\hat{}$) denotes the signals in the logdomain.

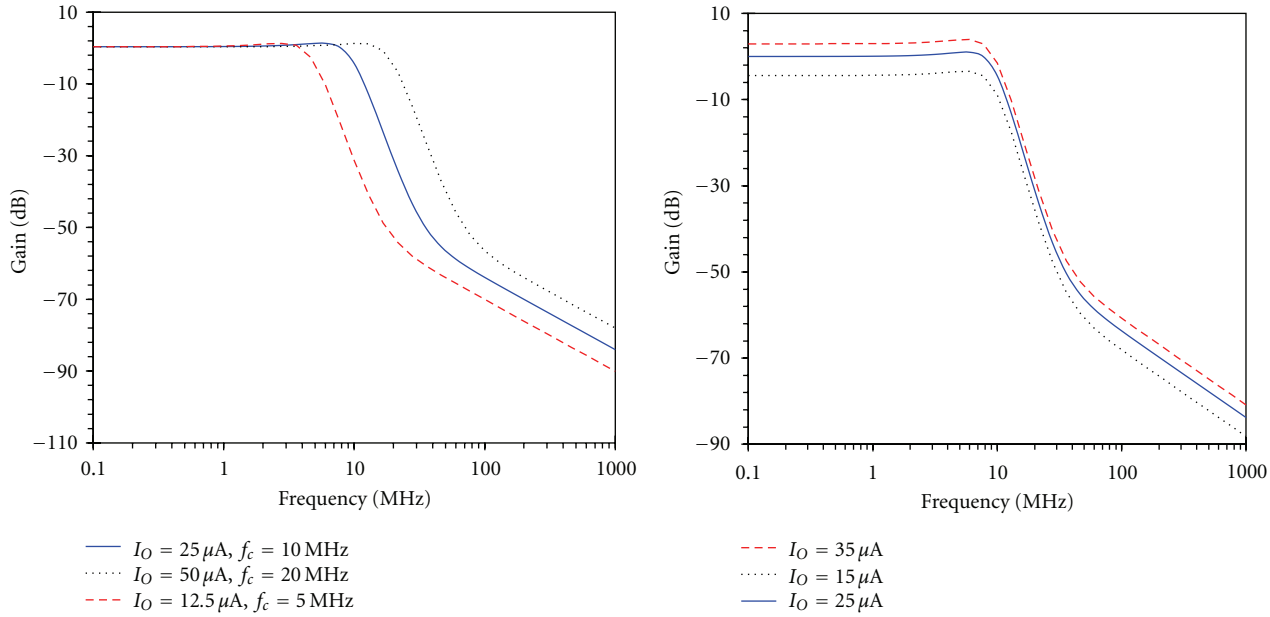
The sequence of steps to be followed in transforming a linear GFBD into log-domain one are given hereunder

(i) Place EXP and LOG blocks in front and behind of each integrator, respectively.

(ii) Place LOG and EXP blocks at the input and output of the filter, respectively.

(iii) dc stabilize the circuit by applying the rules contained in [9] according to which at least one pair of E+ and E− cells must have their outputs connected to each capacitor node and the sum of dc bias currents of E+ cells with their outputs connected at a node should be equal to the corresponding sum of dc bias currents of E− cells with their outputs connected at the same node.

Following the above steps, we obtain the transposed GFBD of the log-domain MFF filter topology depicted in Figure 2. To realize log-domain GFBD of Figure 2,




(a) (b)

Figure 8: Demonstration of electronic tunability of cut-off frequency and gain of MFFs.

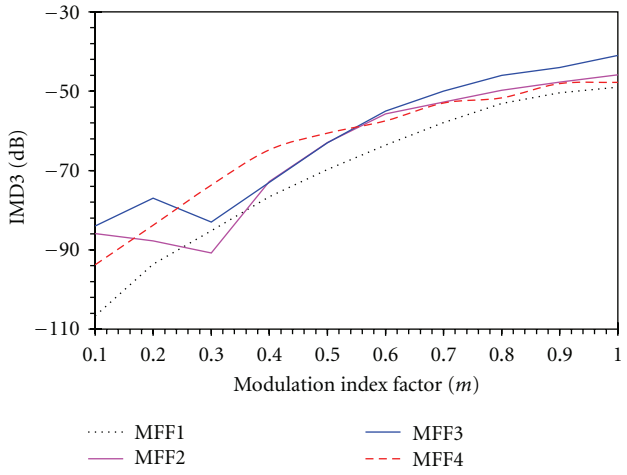



Figure 9: Linear performance of the LP filter functions of 5th order log-domain MFFs of Figure 6.

log-domain lossless integrator and summation blocks are required.

## 3. Log-Domain Building Blocks

The building blocks for implementing log-domain integrator are exponential cells (E cells) which have been reported in [7] for both types of polarity. The reason for using these cells in the circuits is their realization using only NPN transistors, thereby rendering the circuits suitable for IC form. The output current in both the cells is given in terms of terminal voltages as follows:

$$i_{\text{out}} = I_O e^{(\hat{V}_{\text{IN}} - \hat{V}_{\text{OUT}})/V_T}. \tag{8}$$

The possible realizations of LOG and EXP operators from the E cells, used in this paper, are taken from [7].

The log-domain lossless noninverting and inverting integrator configuration is depicted in Figures 3 and 4 respectively, where the input-output relationship is as follows:

$$\text{EXP}\left(\hat{V}_{\text{OUT}}\right) = \pm\frac{I_O}{CV_T}\int \text{EXP}(V_{\text{IN}}) \cdot dt, \tag{9}$$

where $\tau_j = CV_T/I_O$ is the time-constant of log-domain integrator. Thus, an equivalent resistor $\hat{R} = V_T/I_O$ is realized by the log-domain integrator, which is electronically controllable through $I_O$.

The multipleinput algebraic summation blocks required for obtaining HP filter in each configuration are demonstrated in Figures 5(a) and 5(d). The expression for output voltage is obtained as follows:

$$\text{EXP}\left[\hat{V}_{\text{OUT}(n)}\right] = \text{EXP}(V_{\text{IN}}) \pm \text{EXP}\left[V_{\text{OUT}(n-1)}\right] \pm \text{EXP}\left[V_{\text{OUT}(n-2)}\right] \pm \cdots \pm \text{EXP}\left[V_{\text{OUT}(0)}\right]. \tag{10}$$

## 4. Simulation Results

To verify the validity of the proposed design, 5th-order log-domain MFF of each configuration depicted, respectively, in Figures 6(a) and 6(d) were constructed for $V_{CC} = V_{EE} = 1.5$ V,

Table 1: Signs (Noninverting or inverting) of the filter functions (NA: Not Applicable, BP1: $BP_{(n/2)}$, BP2: $BP_{(n+1)/2}$, BP3: $BP_{(n-1)/2}$.

| Order | MFF1 | | | | MFF2 [19] | | | | MFF3 | | | | MFF4 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LP | BP1 | BP2 | BP3 | LP | BP1 | BP2 | BP3 | LP | BP1 | BP2 | BP3 | LP | BP1 | BP2 | BP3 |
| 1 | + | NA | NA | NA | + | NA | NA | NA | − | NA | NA | NA | − | NA | NA | NA |
| 2 | − | + | NA | NA | + | + | NA | NA | − | − | NA | NA | + | − | NA | NA |
| 3 | − | NA | − | + | + | NA | + | + | + | NA | − | − | − | NA | + | − |
| 4 | + | − | NA | NA | + | + | NA | NA | + | − | NA | NA | + | + | NA | NA |
| 5 | + | NA | − | − | + | NA | + | + | − | NA | + | − | − | NA | − | + |
| 6 | − | − | NA | NA | + | + | NA | NA | − | + | NA | NA | + | − | NA | NA |
| 7 | − | NA | + | + | + | NA | + | + | + | NA | + | + | − | NA | + | − |
| 8 | + | + | NA | NA | + | + | NA | NA | + | + | NA | NA | + | + | NA | NA |
| 9 | + | NA | + | − | + | NA | + | + | − | NA | − | + | − | NA | − | + |
| 10 | − | + | NA | NA | + | + | NA | NA | − | − | NA | NA | + | − | NA | NA |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |

Table 2: *Table* demonstrating that the four MFF configurations presented in the paper are the only stable ones.

| Mode of integrators* | | Type of feedback# | | HP transfer function | Stability status~ |
|---|---|---|---|---|---|
| $I_1$ | $I_2$ | $F_1$ | $F_2$ | | |
| NI | NI | + | + | $\frac{s^2}{s^2 - (s/\tau_1) - 1/\tau_1\tau_2}$ | U |
| NI | I | + | − | | |
| I | NI | − | − | | |
| I | I | − | + | | |
| NI | NI | + | − | $\frac{s^2}{s^2 - (s/\tau_1) + 1/\tau_1\tau_2}$ | U |
| NI | I | + | + | | |
| I | NI | − | + | | |
| I | I | − | − | | |
| NI | NI | − | + | $\frac{s^2}{s^2 + (s/\tau_1) - 1/\tau_1\tau_2}$ | U |
| NI | I | − | − | | |
| I | NI | + | − | | |
| I | I | + | + | | |
| NI | NI | − | − | $\frac{s^2}{s^2 + (s/\tau_1) + 1/\tau_1\tau_2}$ | S |
| NI | I | − | + | | |
| I | NI | + | + | | |
| I | I | + | − | | |

*$I_1$: First integrator after summation, $I_1$: Second integrator after summation, NI: Noninverting, I: Inverting.
#$F_1$: Feedback from first integrator, $F_2$: Feedback from second integrator.
~U: Unstable, S: Stable.

Table 3: Comparison of nonlinearity, component count and power dissipation of MFFs of Figure 6.

| MFF/Par. | IMD3. at $m = 100\%$ | rms output $I_{noise}$ (nA) | DR @ 0.3% IMD3 level (dB) | No. of components | | Static power cons. (mW) |
|---|---|---|---|---|---|---|
| | | | | Tr. | $C_S$ | |
| MFF1 | −49 dB | 230 | 36.82 | 66 | 38 | 3.62 |
| MFF2 | −45.9 dB | 240.1 | 35.24 | 72 | 36 | 3.76 |
| MFF3 | −41 dB | 250.3 | 33.75 | 60 | 40 | 3.48 |
| MFF4 | −47.8 dB | 236.4 | 35.82 | 60 | 40 | 3.43 |

Table 4: Statistical simulation results about the frequency behaviour of the LP filter functions of log-domain MFFs of Figure 6.

| MFF | Gain | | Cut-off Frequency | | IMD3 at $m = 100\%$ | |
|---|---|---|---|---|---|---|
| | STD | MV | STD | MV | STD | MV |
| MFF1 | 0.0078 | 0.96 | 0.252 MHz | 9.82 MHz | 1.53 dB | −47.7 dB |
| MFF2 | 0.0087 | 0.95 | 0.284 MHz | 9.8 MHz | 1.65 dB | −44.5 dB |
| MFF3 | 0.0095 | 0.94 | 0.288 MHz | 9.81 MHz | 1.72 dB | −39.4 dB |
| MFF4 | 0.0095 | 0.94 | 0.292 MHz | 9.78 MHz | 1.84 dB | −46.1 dB |

$I_O = 25\,\mu$A, and $C = 15.9$ pF which yield cut-off/centre frequency ($f_C$) = 10 MHz. The NPN transistors in cell implementations are simulated using the parameters of the AT&T CBIC-R NR100N NPN transistor [5]. The frequency behaviour of the filter was evaluated by performing large-signal transient analysis using the PSPICE simulator, with modulation index factor $m = i_{\text{peak}}/I_O = 50\%$. The small deviations, caused by bipolar transistor imperfections, have been compensated by following the procedure suggested in [11, 22]. The values of the compensation factors were $K_{\text{RE}} = 0.999$, $K_{\text{RB}} = 0.996$, $K_\beta = 0.986$, $K_{1\text{VA}} = 1$, $k_{2\text{VA}} = 0.99$, $f_\beta = 0.00019$, and $f_{\text{VA}} = 0.0013$. Also, the DC bias currents for the final stage of the filter are multiplied by a factor 1.0086. The compensated magnitude responses of 5th-order log-domain MFF topologies are given in Figures 7(a) and 7(d). The electronic tunability of cut-off frequency and gain of MFFs has been verified for different values of the bias current as shown in Figure 8.

A comparative study of the proposed circuits was carried out on the basis of usually used parameters of nonlinear behaviour, number of components, sensitivity, and power consumption.

The nonlinear behaviour of each MFF biquad configuration for LP response was carried out employing IMD3 test. For this purpose, two closely spaced tones 3 MHz and 3.2 MHz, which fall in the passband of the LP response, were applied at the input of each of the filters. The simulated values of distortion at $m = 100$ for the biquads are given in Table 3.

Also, the simulated IMD3 responses as a function of the modulation index factor, are given in Figure 9. Further, Table 3 also contains computed data about simulated rms values of the output noise currents integrated over 20 MHz range, dynamic ranges (DR) at 0.3% distortion level, number of devices required, and static power consumption. For obtaining sensitivity graph, Monte Carlo analysis with 100 runs assuming 1% deviation (with Gaussian distribution) was carried out with respect to the variations of the integrating capacitors and bias currents. From this graph, the values of standard deviation (STD) and mean variance (MV) of the maximum gain and cut-off frequency were calculated as given in Table 4. In addition, Monte Carlo analysis with 100 runs assuming 1% deviation (with Gaussian distribution) was carried out with respect to the variations of bias currents. From this graph, the values of standard deviation (STD) and mean variance (MV) of the IMD3 values were calculated as given in Table 4.

The results of Tables 3 and 4 reveal that each design has different performance for different set of parameters, thereby, facilitating application specific selection of MFF design. Further, one can see from the comparative study that MFF1 is better design as most of its performance factors are superior vis-a-vis other designs.

## 5. Conclusion

A novel generic $n$th MFF topology based on log-domain technique, capable of yielding four canonical stable designs, has been presented. The derived MFFs besides realizing simultaneously HP, LP, and BP responses are modular as these can be constructed using only lossless integrators. The circuits use grounded capacitors and permit electronic adjustment of filter parameters. Both these features are suitable for monolithic integration. Further, no restriction is required to be imposed on the order of the filter. The comparative study of MFFs facilitates their application specific design. The PSPICE results confirm the theoretical predictions.

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