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Research Article

Application of Thermal Network Model to Transient Thermal Analysis of Power Electronic Package Substrate

Masaru Ishizuka,[1] Tomoyuki Hatakeyama,[1] Yuichi Funawatashi,[1] and katsuhiro Koizumi[2]

[1] *Department of Mechanics System Engineering, Toyama Prefectural University, Imizu 939-0398, Japan*
[2] *COSEL CO. LTD., 1-6-43 Kamiakae-machi, Toyama 930-0816, Japan*

Correspondence should be addressed to Masaru Ishizuka, ishizuka@pu-toyama.ac.jp

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In recent years, there is a growing demand to have smaller and lighter electronic circuits which have greater complexity, multifunctionality, and reliability. High-density multichip packaging technology has been used in order to meet these requirements. The higher the density scale is, the larger the power dissipation per unit area becomes. Therefore, in the designing process, it has become very important to carry out the thermal analysis. However, the heat transport model in multichip modules is very complex, and its treatment is tedious and time consuming. This paper describes an application of the thermal network method to the transient thermal analysis of multichip modules and proposes a simple model for the thermal analysis of multichip modules as a preliminary thermal design tool. On the basis of the result of transient thermal analysis, the validity of the thermal network method and the simple thermal analysis model is confirmed.

1. Introduction

Laptop personal computers and cellular phones have become smaller and thinner in recent years, while their functions have become more sophisticated. As a result, the heat dissipation density and dissipation power per volume of these devices have significantly increased. Cooling design is the key to the prevention of heat problems. At the same time, there are growing demands for the acceleration of product development and reduction of costs.

Computational fluid dynamics (CFDs) codes [1, 2] have proved their high potential as a tool of thermal design of electronic equipment. However, as the product development cycle is shortened, the CFD-based thermal design needs a new format that allows the packaging designer fast and versatile searches for better design options. The most serious factor that slows the CFD-based design is the geometric complexity created by packing various components in a tight space of the system box.

Recently, in order to reduce the CFD workload, several approaches for the thermal design of electronic equipment have been reported. Nakayama et al. [3–5] proposed a methodology coined build-up approach (BUA) and have applied it to the board- and box-level thermal analyses. Minichiello and Belady [6] proposed a thermal design methodology and applied it to the design of a multi-processor enterprise server, the RP8400. Their methodology combines the well-known analytical and experimental thermal design tools, including heat transfer correlations, flow network modeling, and CFD techniques and experimental measurements.

In a broader perspective, the issue of our interest is concerned with model reduction methodologies, and on this subject, several reports have been presented. Assumption of velocity profiles in computational elements reduces the nonlinear momentum equation to a linear equation, and such linearized models have been proposed by Moosmann et al. [7], D'Amore et al. [8], and Rudnyi et al. [9]. Molina and Clemente [10] reported on an automated technique for reducing actual systems to lumped-parameter thermal models.

Ishizuka and Hayama [11] have also proposed a thermal analysis scheme, in which CFD analysis and thermal network

method are coupled. In this scheme, the essential factors affecting thermal fluid phenomena in electronic equipment are first clarified using CFD analysis, then, using the CFD results obtained under suitable boundary conditions, main heat flow passages are identified. At the end of the model-reduction process, a thermal network model is developed. The thermal network model facilitates the design parameter survey for choosing a set of optimum parameters without resorting to time-consuming CFD analysis. Ishizuka et al. have proposed some simplified models such as heat diffusion model in [12], thermal convection model in [13], phase changing process model in [14, 15], and 3D model in [15] to simulate various thermal behaviors in electronic devices. From those results, it is found that if we would understand the heat phenomenon in a system, some temperature values for the system could be predictable by using a simplified model for a thermal network method.

The present study focuses on the derivation of a simpler network model to predict the transient temperature distribution of the package substrate covered by the cap, where the package consists of high-power transistor chips, other IC chips, resistor chips, and capacitor chips. The analysis was carried out to simulate the results of the transient temperature rise on the surface of a substrate, taking into consideration natural convection and radiation, in the heat transfer mode for a cap-attached circuit substrate in addition to the thermal conduction. The alumina substrate has a circuit composed of various chips centering around four power transistor chips (hereinafter called power transistors). The heat transfer modes for packages are very complicated. The validity of the proposed thermal network model is demonstrated on the basis of a comparison between calculated values and measured values.

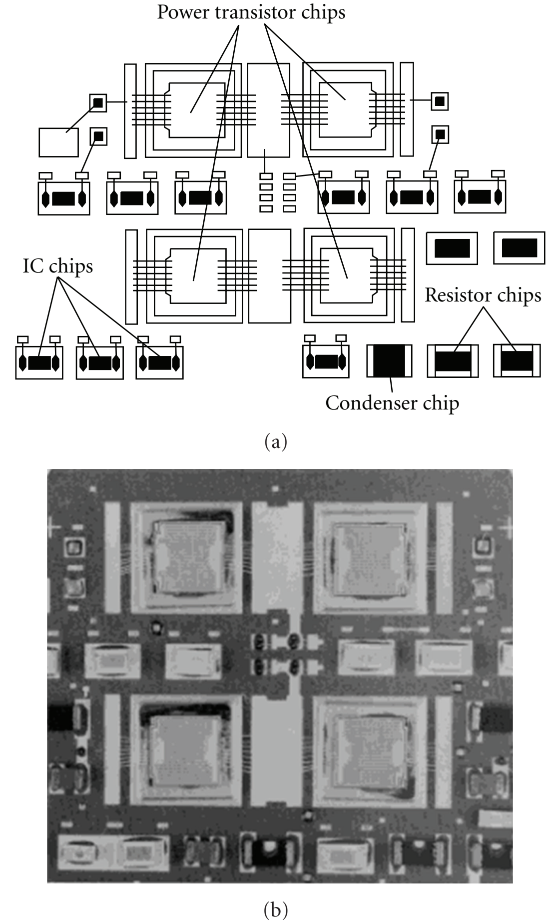

Figure 1: (a) Power-transistor layout. (b) Power transistors (photo).

2. Experiment

2.1. Package Structure. Various kinds of chips such as IC, resistor, and capacitor, centered around four power transistors (square of 4.5 mm in size, 0.3 mm in thickness, each having power dissipation of 8 W), are mounted and wire-bonded to form an electronic circuit on a 1.6 mm-thick and 6 cm-square substrate formed from 92% alumina ceramic. The vicinity of the power transistors is illustrated in Figure 1. The power transistors, a heat source in this circuit, are arranged at 4 mm intervals.

The power dissipation value contributed from other chips may be neglected. Interconnections are provided within the substrate, forming a multilayer printed circuit board. This chip group is covered with a 5 cm-square, 2.8 mm-high and 0.25 mm-thick kovar cap, in which nitrogen gas (N_2 gas) is sealed. Figure 2 shows a cross-sectional view of the substrate. The power transistor chips were mounted on the molybdenum heat sink blocks, which were aligned on the copper heat sink blocks with electroconductive epoxy. The other IC chips, resistor chips and capacitor chips were also mounted on the substrate top conductor metal die pads with electroconductive epoxy. They were then wire-bonded with 30 μm diameter gold wire.

2.2. Temperature Measurement. The module to be measured was held horizontally 10 cm above the surface of a desk and supported at its edges by three thin glass epoxy sticks (3 mm in diameter) in a clean room with free airflow. Temperature was controlled to 298 K. A point equally distant from the four power transistors was considered as the center (radius $r = 0$), and two points were located on the back of the substrate ($r = 0$) and one on the front ($r = 2.55$ mm). A copper-constantan thermocouple (0.1 mm in diameter) for use in making the measurements was bonded by good conductive epoxy material to each of the measuring points. As a measuring procedure, temperature rise values after the application of electric power from a DC power source to the power transistors were recorded by means of an infrared camera. The experiment was stopped when temperature T_0 at measuring point $r = 0$ on the back of the substrate exceeded 410 K.

3. Analysis

3.1. Heat Transfer Model for Multichip Modules. The paths through which package heat transfer takes place was considered as follows. The substrate bottom area and substrate top area, with the exception of the kovar cap area, include

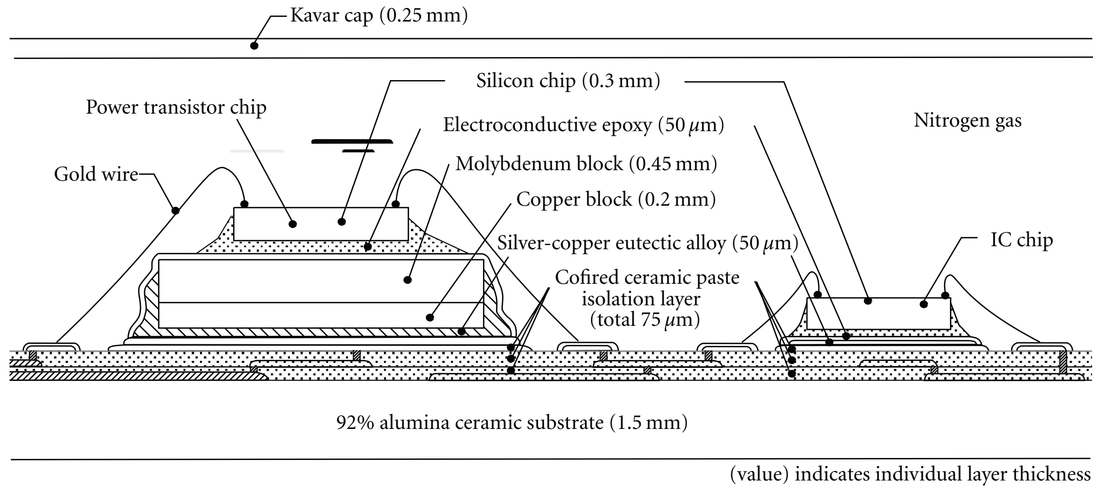

Figure 2: Cross-sectional view of the substrate.

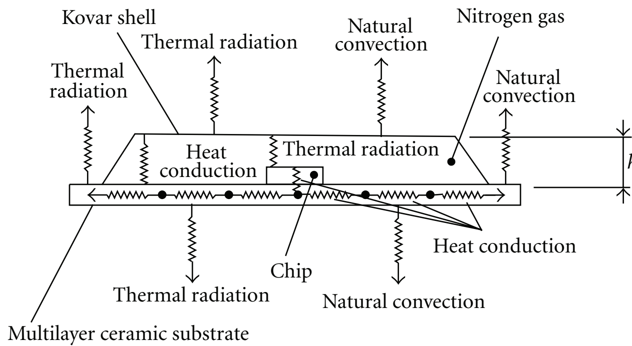

Figure 3: Heat transfer form for package.

heat transport by thermal radiation and natural convection. Inside the kovar cap, heat transport by heat conduction of the nitrogen gas and thermal radiation was considered. At the kovar cap top surface area, heat transport occurs by thermal radiation and natural convection. Furthermore, inside the substrate and the cap, heat transport occurs only by thermal conduction. These aspects are illustrated in Figure 3.

Figure 3 indicates the paths by which heat transfer from the module takes place, where the following major heat transfer factors were considered:

(1) thermal conduction inside the substrate,

(2) natural convection and thermal radiation from the top and bottom surfaces of the substrate to the atmosphere,

(3) thermal conduction through N_2 gas and thermal radiation from the substrate surfaces to the cap,

(4) thermal conduction from the substrate to the cap through the welded area between the substrate and the cap (not shown in Figure 3).

3.2. Thermal Network Model. The existence of the cap is considered to have an influence on the temperature distribution; therefore, the effect of the cap should be taken into consideration. However, since considering the cap results in a complicated three-dimensional analytical model, there is no advantage in adopting the thermal network method. Therefore, the analytical model is formed on the basis of the following assumptions to reduce the model's dimensions from three to one.

(1) The temperature of the center of the cap surface is the same as that of the substrate area where the cap is welded.

(2) The 4 power transistors are regarded as one nodal point.

(3) The heat dissipated by the power transistors flows out in the radial direction.

These assumptions will make the analytical model one dimensional (axial symmetry).

The substrate was divided, as shown in Figure 4, centering on the power transistor ($r = 0$). It is assumed that there is no temperature difference between individual divided partitions and that the partitions are numbered $0, 1, 2, \ldots, n$, respectively, from the center. In this study, n was taken as 6. Representing the heat resistance and the thermal capacitance for each partition by R and C, respectively, the thermal network model for the heat transfer is formed, where heat flux Q_0 is generated by the power transistors, as shown in Figure 5. The total of the heat flux Q_0 was assumed to flow out toward the region 1 in the substrate. Since the area of the region 0 including the power transistor chips were smaller than those of the other regions, the heat transfer for the central region 0 was neglected. In Figure 5, in the case of the first partition where the temperature is represented by T_1, heat flow Q_1 flows out toward external region 2 through heat resistance R_3 due to the thermal conduction. Some of the heat is stored in the thermal capacitance C_1, or dissipated directly or indirectly through cap, out of the substrate by natural convection and thermal radiation through thermal resistance values such as R_2 and R_{16}. It is assumed that

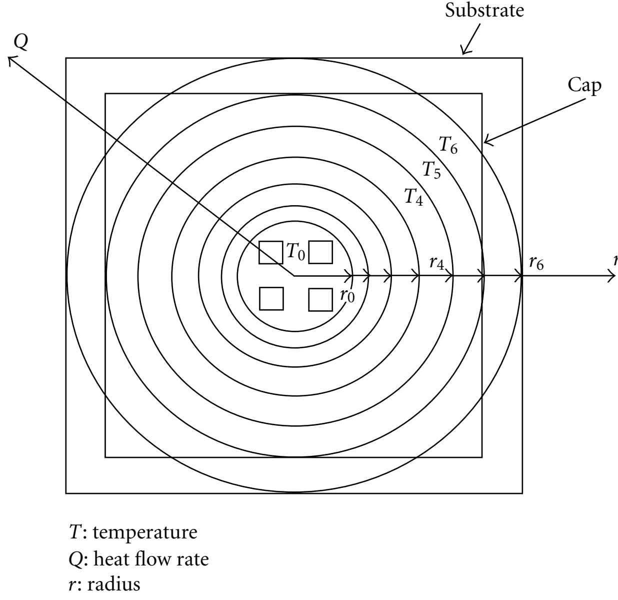

Figure 4: Substrate partition.

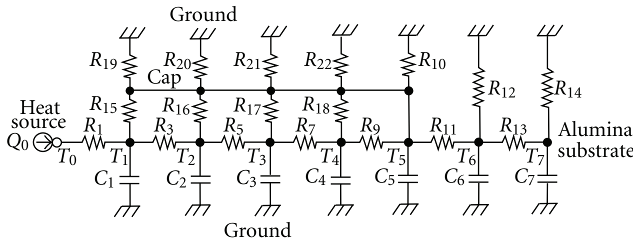

Figure 5: Thermal network model (Model 1).

C_7 value is infinite. Note that although the actual module forms a regular square and the power transistors are arranged quadrilaterally, these may be represented approximately by circles, having diameters equal to the length of one side of the respective rectangle, as shown in Figure 4. On the basis of the previously mentioned assumptions, the center of the cap was linked with the welded portion of the substrate without any thermal resistance.

In addition, the cap thermal capacity was neglected, because it is infinitesimally small compared to that of substrate. In addition, it is assumed, as described previously, that cap temperature is equal to substrate temperature in partition 5.

3.3. Evaluation of Thermal Resistance. The thermal conduction partition model in the substrate is illustrated in Figure 6. It was assumed that a circular heat source, whose radius is r_0 cm, exists at the center of a circular multilayer ceramic substrate, whose thickness is d cm, and the heat diffuses in the radial direction. If the temperature at a point on radius r_1 is T_1 and the temperature at a point of radius r_2 is T_2, the heat flow rate along the radial direction is given by

$$Q_{\text{cd}} = 2\pi d_s \lambda_s \frac{\Delta T}{\ln(r_2/r_1)}, \quad (1)$$

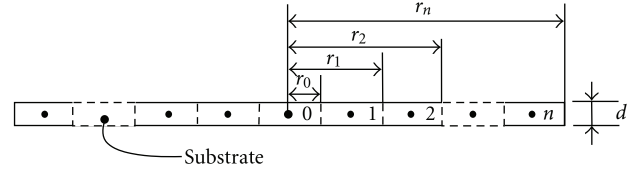

Figure 6: Thermal conduction partition model in the substrate.

where $\Delta T = T_1 - T_2$, λ_s is the thermal conductivity of the substrate.

Therefore, the thermal resistance, R_{cd} in region covered by radius r_1 and radius r_2 is given by

$$R_{\text{cd}} = \frac{\Delta T}{Q_{\text{cd}}} = \frac{\ln(r_2/r_1)}{(2\pi d_s\, \lambda_s)}. \quad (2)$$

The thermal resistance for nitrogen gas inside the kovar cap is given by

$$R_{\text{N}} = \frac{h}{(\lambda_{\text{N}} A)}, \quad (3)$$

where λ_{N} is thermal conductivity, h is the substrate-to-cap distance, and A represents the thermal conduction area.

If there exists a temperature difference (ΔT) between the air and the substrate, the heat flow rate Q_{cv} which passes through the area A of the substrate is given by

$$Q_{\text{cv}} = \alpha_{\text{cv}} A \Delta T. \quad (4)$$

In general, the heat transfer coefficient, α_{cv} is related to the heat transfer phenomenon. If the flow is laminar and the heat transfer occurs through natural convection, the natural convection heat coefficient in the case of two-dimensional flat plate is given considering that Gr·Pr value (Grashof and Prandtl number) in this study was the order of 10^5 as follows

$$\alpha_{\text{cv}} = 2.8D\left(\frac{\Delta T}{L}\right)^{0.25}, \quad (5)$$

where ΔT is the temperature rise with reference to ambient temperature T_a; $T_a = 298\,\text{K}$ is selected as a reference temperature and the value of D is determined by the orientation location of the flat plate, shown in Figure 7. Facing up it is equal to 0.54, while facing down it is 0.27. L is the characteristic length which is determined by the flow path of the cooling air on the hot surface of the material. In this divided doughnut-shaped plate, having inner and outer radius of r_1 and r_2, respectively, the assumed characteristic length L is given by the ratio of area/perimeter of the doughnut-region as follows:

$$L = \frac{\pi(r_2^2 - r_1^2)}{2\pi(r_1 + r_2)} = \frac{(r_2 - r_1)}{2} \quad (6)$$

Then, thermal resistance R_{cv} is expressed as follows, where A represents the thermal radiation area:

$$R_{\text{cv}} = \frac{1}{(\alpha_{\text{cv}} A)}. \quad (7)$$

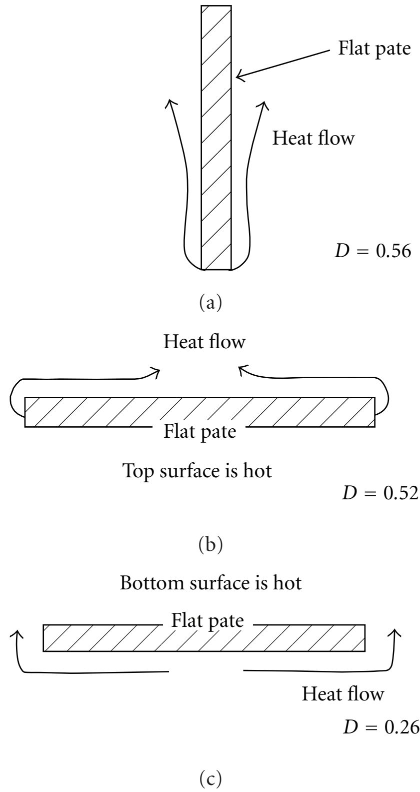

Figure 7: Value D in natural heat transfer equation (5).

In the exchange of thermal radiation energy between two materials which are not black bodies, the general thermal radiation equation is given by

$$Q_{\mathrm{ra}} = \sigma FA\left(T_1^4 - T_2^4\right), \quad (8)$$

where σ is Stefan-Boltzmann's constant which is 5.67×10^{-8} W/m^2 K^4, A is the thermal radiation area, and T_1 and T_2 are absolute temperature, respectively. Furthermore, F is the shape factor which is defined as

$$F = \frac{1}{(1/\varepsilon_1 + (A_1/A_2)(1/\varepsilon_2 - 1))}, \quad (9)$$

where ε_1 and ε_2 are emissivities for the materials. If one side is the atmosphere, A_2 becomes infinity; therefore, F becomes ε_1.

From (8), thermal resistance R_{ra} is expressed as follows:

$$R_{\mathrm{ra}} = \frac{(T_1 - T_2)}{Q_{\mathrm{ra}}} = \frac{1}{\left(\sigma FA\left(T_1^2 + T_2^2\right)(T_1 + T_2)\right)}. \quad (10)$$

3.4. Calculation of Thermal Capacitance. The calculation of thermal capacitance of each partition, for example, C_i is for the ith partition, is expressed as follows, by defining the substrate density as ρ, specific heat at constant pressure as c_p, and substrate thickness as d:

$$C_i = c_p \pi d\left(r_i^2 - r_{i-1}^2\right). \quad (11)$$

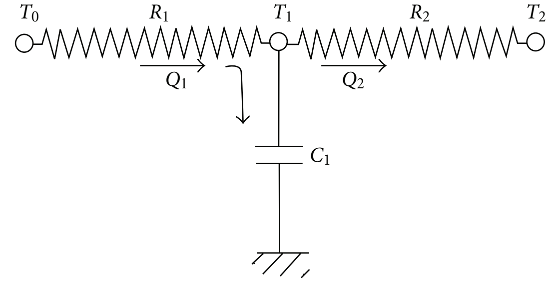

Figure 8: Heat flow at tee section.

3.5. Equation Formulation. The thermal network method is based on the similarity between the diffusion equation for thermal engineering and that for electric engineering, and it is found that the analogous quantities are voltage-temperature and current-heat flow.

Therefore, the transient analog method is formed on the basis of a number of lumped *RC* tee sections, as shown in Figure 8, with subsequent employment of the node analysis method. The following equations, which can be written as examples, are based on heat flow conservation for a nodal point

$$C_1 \frac{dT_1}{dt} = Q_1 - Q_2 \quad \text{at } T_1 \text{ point}, \quad (12)$$

and for heat paths based on thermal resistance definition

$$\begin{aligned} T_0 - T_1 &= Q_1 R_1 \quad \text{for } R_1, \\ T_1 - T_2 &= Q_2 R_2 \quad \text{for } R_2, \end{aligned} \quad (13)$$

where Q represents the heat flow value through thermal resistance and T represents the temperature value.

3.6. Calculation Procedure. The above equations are nonlinear in nature, due to (7) and (10), and iterative calculations are required. However, to simplify the method of calculating parameters, temperature T, required for calculating (7) and (10), is approximated by a value calculated with $\tau = \tau_{i-\Delta\tau}$ instead of $\tau = \tau_i$, assuming that temperature change ΔT is very small during the period $\Delta\tau$ when $\Delta\tau$ is very small; that is, $\Delta\tau \ll R_i C_i$. To solve these equations, the Runge-Kutta secondary approximate method is used. The calculation flow chart is given below.

(1) Set the applied power Q_0.

(2) Give the initial temperature value T_0 for the initial time τ_0.

(3) Calculate the thermal resistance values R_0 from (7) and (10) using the above temperature value T_0 and thermal capacitance C.

(4) Solve the linearized equation system to yield the temperature for the new time level $\tau = \tau_0 + \Delta\tau$ using the Runge-Kutta method.

(5) Advance the time level τ by $\Delta\tau$.

(6) The newly predicted temperatures are assigned to the initial temperature.

(7) The procedure is repeated from step (5) for the subsequent time level until $\tau = \tau_{\max}$.

3.7. Numerical Example. As the calculation condition, the power transistor region, the shapes of the cap, and the substrate are approximated as a circle of diameter 1.5 cm, 5 cm, and 6 cm, respectively, as shown as Figure 4. It is also assumed that the substrate is partitioned into six sections (number of partitions $n = 6$), having radii of $r_0 = 0.75$ cm (central partition), $r_1 = 0.9$ cm, $r_2 = 1.1$ cm, $r_3 = 1.5$ cm, $r_4 = 2.2$ cm, $r_5 = 2.6$ cm, and $r_6 = 3.0$ cm, respectively, where r represents the radius for each circle. Substrate characteristics are as follows. Thickness: $d_s = 1.5$ mm, thermal conductivity: $\lambda_s = 16.7$ W/(mK), density: $\rho = 3.6 \times 10^3$ kg/m^3, and specific heat: $c_p = 879$ J/kg K. Other factors are emissivity: $\varepsilon_N = 0.8$, nitrogen thermal conductivity: $\lambda_N = 0.0286$ W/mK, the cap height: $h = 2.75$ mm, and the cap thermal conductivity: $\lambda_{cap} = 18.6$ W/mK. However, in this study, the property values of the cap were not decided using the assumptions. The calculations were carried out using a time increment $\Delta\tau = 1$ ms, where the conductivity of the substrate was substituted by the conductivity of alumina which was measured by the laser-flash method, because the volume of alumina occupies 98% or more of the total substrate volume.

4. Results

4.1. Comparison of Calculated Values and Measured Values. Figure 9 compares the measured and predicted values for the case of T_0, T_3, T_5, and T_{cap}. T_0 is the temperature of the partition 0 as shown in Figure 4, near the center of the substrate bottom surface, T_3 is the temperature of the partition 3, near the midpoint between the edge of the substrate bottom surface and the center of the substrate bottom surface, T_5 is the temperature of the partition 5, near the edge of the substrate bottom surface, and T_{cap} is the temperature near the center of the kovar cap. For T_3 and T_5, temperatures at two different points in the same region were averaged. Temperature differences between the two temperatures were within 3%. Agreement between measured and predicted values is very satisfactory. In order to prevent the damage of chip, the power supply switch was turned off in the case of temperature T_0 reaching to a value of 410 K.

Figure 9 also shows result using the results of calculated temperature T_0 on the basis of another model in which thermal diffusion is caused only by the substrate thermal conduction (Model 2 as shown in Figure 10). It can be observed here that the temperature T_0 predicted by the model 2 is approximately 10% higher as compared to that obtained using the present model (Model 1). The trends of temperature rise for T_0 is similar to that in the case of the Model 2. The difference in temperatures other than T_0 was within the range of 5% to 8%. Here, since the heat sink effect due to the thermal capacity of the substrate is much large at only initial stage of the temperature rise, the results by model 2 considering only conduction was compared once by model 1. Of course, time passing, the difference becomes much larger. Of course, time passing, the difference between them becomes much larger.

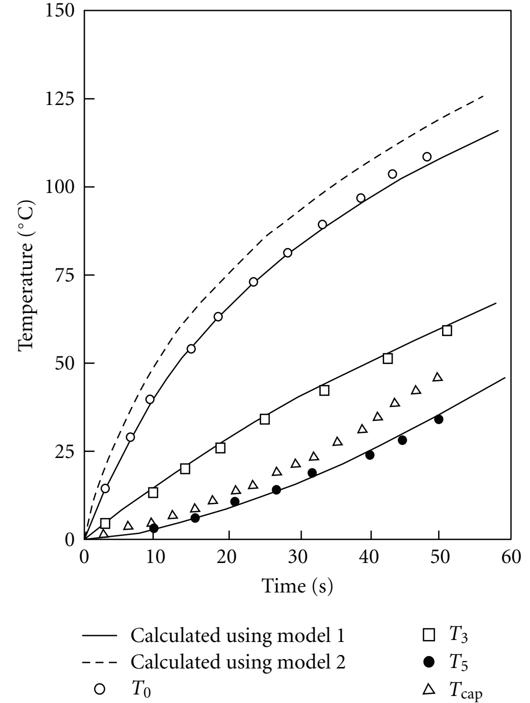

Figure 9: Comparison between calculated values and measured values.

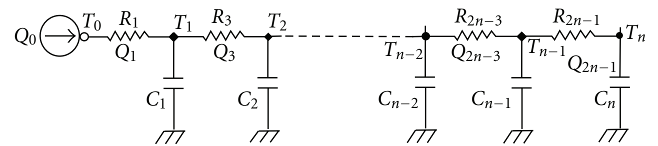

Figure 10: Thermal network model (Model 2).

5. Discussion

In forming the heat transfer model for the present experiment condition, it was assumed that the thermal conduction inside the substrate plays a dominant role in contributing to the heat transfer of the package. The validity of this assumption was verified by comparing the results obtained by considering only thermal conduction and those obtained by considering natural convection and thermal radiation as well as thermal conduction, as shown in Figure 9. The temperature difference between the results obtained by using the heat transfer model and those obtained by using the model which considers only thermal conduction is at the most 10%. That is the reason that in the transient condition, the substrate capacitance works as a main heat sink, and in the steady state condition, the atmosphere does. However, the results obtained by using the proposed heat transfer model coincide closely with the results obtained by using

the model which considers only thermal conduction. On the basis of the recent trends that the power dissipation density values for future electronic elements will become higher or they will be used in a steady-state condition, this 10% difference cannot be neglected. For the current power dissipation density (where power dissipation density value in this substrate is 32 watts for 36 cm^2 area), this proposed model is considered to be useful as a simulation model for thermal design because of its simple and convenient form. It should also be noted that when a forced cooling method is applied instead of natural convection, which was adopted in this experiment, the effect of the proposed model should be higher if (5) were replaced by the forced convection heat transfer coefficient. The difference between results obtained by using the proposed model and by the other model where the natural convection and thermal radiation were neglected would be larger.

6. Conclusion

A thermal network model was applied to simulate a transient temperature rise in small-size multichip modules. The heat transfer process by natural convection and thermal radiation was also adopted in this model in addition to the thermal diffusion by thermal conduction. The calculated results using this model gave a very reasonable estimation of the measured substrate temperature values. Since substrate thermal designing becomes more important and great design accuracy is required, as chip power dissipation density becomes larger, this model is considered sufficiently practical as an engineering model for simulating a transient temperature rise in the substrate, because it is structurally simple and easy to use.

Nomenclature

A: Area, m^2
C: Thermal capacitance, J/K
c_p: Specific heat, J/(kg K)
D: Constant in the natural heat transfer equation
d: Substrate thickness, m
F: Shape factor
h: Cap height, m
L: Reference length, m
Q: Heat flow rate, W
R: Thermal resistance, K/W
T: Temperature, K
ΔT: Temperature rise, K.

Greek Symbols

α: Heat transfer coefficient, W/m^2 K
ε: Emissivity
λ: Thermal conductivity, W/m K
ρ: Density, kg/m^3
σ: Stefan-Boltzmann constant = 5.67×10^{-8}, $W/(m^2 K^4)$
τ: Time, s.

Subscription

a: Atmosphere
cap: Cap
cd: Thermal conduction
cv: Natural convection
ra: Thermal radiation
N: Nitrogen.

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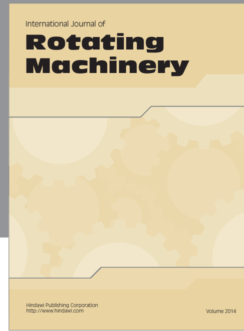
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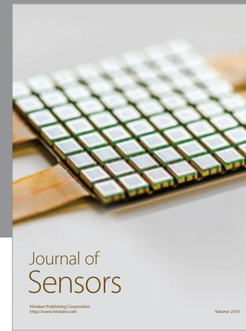
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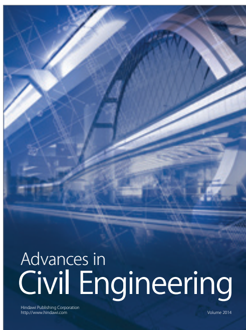
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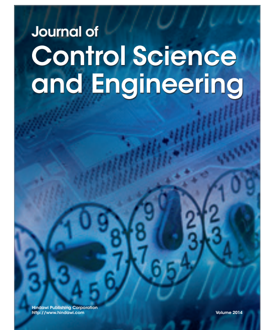
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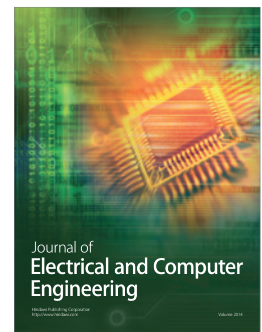
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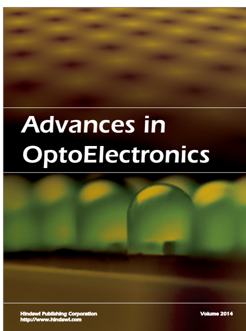
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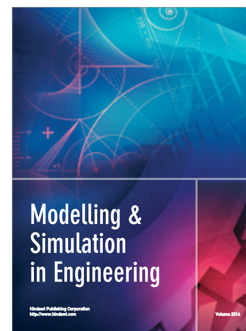
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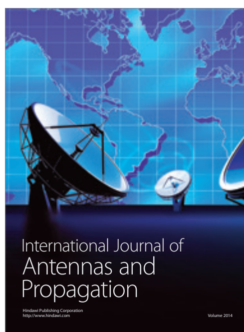
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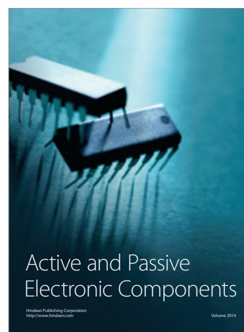
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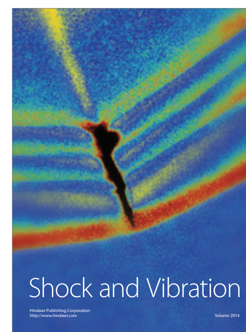
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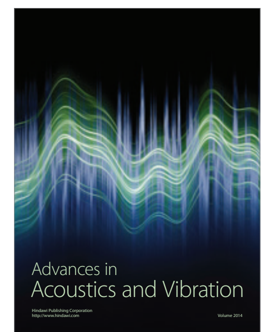
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