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Research Article

Proposal of High-Temperature-Operation Tolerant SOI MOSFET and Preliminary Study on Device Performance Evaluation

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We propose a high-temperature-operation (HTOT) SOI MOSFET and show preliminary simulation results of its characteristics. It is demonstrated that HTOT SOI MOSFET operates safely at 700 K with no thermal instability because of its expanded effective bandgap. It is shown that its threshold voltage is higher than that of the conventional SOI MOSFET because its local thin Si regions offer an expanded effective band gap. It is shown that HTOT SOI MOSFET with 1-nm-thick local-thin Si regions is almost insensitive to temperature for $T < 700$ K (427 C). This confirms that HTOT SOI MOSFET is a promising device for future high-temperature applications.

1. Introduction

The long-term goal in integrated circuits is to lower the dimensionality of MOS transistors in order to increase the function-density and also the speed of extremely large-scale silicon-integrated circuits [1]. The necessity of the silicon-on-insulator (SOI) MOSFET is clear, given its merits of high-speed operation and low-power operation with fewer short-channel effects [2]. However, its off-leakage current is significant, even in thin SOI MOSFETs in the sub-100-nm regime [3]. The author recently proposed the tunneling barrier junction (TBJ) SOI MOSFET that offers suppressed off-leakage current [4, 5]. It has been shown that the TBJ SOI MOSFET suffers from low drive current if used at low temperatures as intended [6].

It has been demonstrated, however, that the thin SOI MOSFET is a promising device for applications that work at 300 C [1]. Its off-leakage current is still a serious problem and prevents its use at higher temperatures. When analyzing high-temperature-operation, it is anticipated that we do not need full quantum-mechanical simulations even for a thin SOI MOSFET because the influence of various carrier scattering events on the transport in the channel region is crucial; so-called *thermalization* is dominant in the Si material.

This paper applies the semiclassical transport model to assess the feasibility of SOI MOSFET in achieving high-temperature operation. This paper introduces the High-Temperature-Operation Tolerant (HTOT) SOI MOSFET and shows preliminary simulation results of its characteristics. A commercial 2D device simulator [7] is used to simulate the drain current characteristics throughout the study.

2. Device Structure and Simulations

A schematic of HTOT SOI MOSFET is shown in Figure 1(a). The device has an n^+-Si gate, a thin n-type body, two thin p-type bodies, and two local-thin Si regions; it is assumed that the top SOI layer surface has (001) orientation. The gate oxide layer is 5-nm thick, buried oxide layer is 100-nm thick, thin n-type Si body and thin p-type Si body are 10-nm thick, and two local-thin Si regions are 1-nm or 2-nm thick; the local-thin Si regions are 2-nm long. n^+-Si source and drain diffusion regions are 10-nm thick and their doping concentrations are 1×10^{20} cm^{-3}; the junction is assumed to be abrupt for simplicity. P-type body has a doping concentration of 3×10^{17} cm^{-3} and n-type body has a doping concentration of 1×10^{15} cm^{-3}. Gate length (L_g) is 100 nm (or 60 nm) and gate width (W) is 1 μm; n-type Si

region is typically 10 nm long and p-type Si region is typically 40 nm long (20 nm long in some cases); this dimension is selected to suppress the short-channel effect. Since the Si layer is very thin in the two local-thin regions, the energy levels in these regions are distinctly quantized. Schematic band structure at $V_d = 0\,\text{V}$ and $V_g = V_{\text{fb}}$ is shown in Figure 1(b), and the effective bandgap energy (E_G^*) of the local-thin Si regions is larger than the nominal bandgap energy of bulk Si (E_G); its theoretical expression is given as [8]

$$E_G^* = E_{n1} - E_{p1}, \tag{1}$$

where E_{n1} is the ground-state level energy of confined electrons in the conduction band and E_{p1} is the ground-state level energy of confined holes in the valence band. In calculating E_G^*, the temperature dependence of intrinsic bandgap energy ($E_G(T)$) of Si is taken into account [9].

When the confinement is along the z-axis (normal to (001) surface), the ground-state energy level of 2-fold X-valleys (E_{n1}) in the local-thin Si body is given by

$$E_{n1} - E_C = \frac{\pi^2 \hbar^2}{2m_{z,\text{2-fold}} t_{\text{S,thin}}^2}, \tag{2}$$

where $m_{z,\text{2-fold}}$ is the effective mass of electrons for the 2-fold X-valley ($= m_l m_0 = 0.92 m_0$) and $t_{\text{S,thin}}$ is the thickness of local-thin Si region (= 2 or 1 nm). $E_{n1} - E_C$ is about 0.1 eV (∼1200 K) when the local-thin Si region is 2-nm thick and about 0.2 eV when the local-thin Si region is 1-nm thick [10]; this suggests that the following consideration based on quantum mechanics is well acceptable because the maximal operation temperature assumed is 700 K.

Since it is assumed that the device works at high temperature, it is expected that semiclassical analysis can be used in the simulations, where we basically assume semiclassical hydrodynamic transport in both thin and thick bodies, and the thermionic emission model [11] is introduced to calculate the transport through the local-thin Si regions using the conventional heterojunction model. This approximation is valid except for the degenerate semiconductor. Therefore, it is expected that, at high temperatures with $V_d = 1\,\text{V}$, the effective energy barrier of the 2-nm-long local-thin Si region enhances thermionic conduction rather than electron tunneling. Accordingly, we apply the thermionic emission model in the present simulations. Mobility models for carrier transport comply with the following physics; Massetit model for doping dependent mobility [12], Lombardi model for mobility degradation at the Si/SiO_2 interface [13] and Canali model for mobility degradation due to velocity saturation [14]. In the present consideration, the subthreshold characteristics are focused on because the increase in the off-current is crucial for such devices at high temperature. The mobility models primarily rule the on-current, not the off-current. Therefore, it is anticipated that the mobility models assumed here do not influence significantly the present consideration.

In addition, since n-type and p-type Si regions are 10-nm thick, discreteness of electronic states is not so crucial for the semiclassical analysis. Thus, to develop an overall consideration of the transport characteristics of the HTOT SOI MOSFET, it can be concluded that the semiclassical analysis is sufficiently verifiable. In the simulation, therefore, we replace the default parameters for the ultrathin Si region with a new set of physical parameters, where the bandgap energy and the effective electron affinity are revised following (1) and (2). When ⟨011⟩ confinement is applied to the HTOT SOI MOSFET, a 3.5-nm-thick local-thin Si region yields a 0.1-eV-high (about) barrier to the conduction electrons; ⟨111⟩ confinement yields an identical result.

Possible fabrication process of the HTOT SOI MOSFET is introduced in Figure 2. The major processing steps are given below.

(a) Shallow and narrow trenches are formed on the n-type SOI layer by the focused ion beam etching technique.

(b) Surface is oxidized in a furnace tube, resulting in separation of the central n-type body.

(c) Surface oxide layer is removed.

(d) A thin crystalline Si layer is deposited epitaxially and surface oxide layer is formed as the gate insulator.

(e) After the n-type body region is covered by resist, p-type body regions are formed by Boron ion implantation and the substrate is annealed.

(f) Gate poly-Si is deposited and the gate electrode pattern is formed. As ion implantation is performed to form n^+ source and drain regions.

The fabrication process mentioned above requests challenging techniques and simulations to predict device characteristics that must also cover atomic-scale physics. The local-thin Si layer has countable atomic layers. Regarding such a thin Si layer, several articles consider the impact of Si-layer thickness on transport properties [15–20]. These articles predict the following

(i) 4 atomic Si layers can roughly hold a bulk band structure [15, 16];

(ii) Effective mass values of conduction band electrons increase as the Si layer is thinned [17–20].

The second point [17–20] suggests that the effective barrier height of the local-thin Si layer may be overestimated. In that case, as suggested later, we should take a longer local-thin Si region to have better characteristics at high temperature.

3. Results and Discussion

3.1. Room Temperature Characteristics. In the HTOT SOI MOSFET, most carriers cannot tunnel through the insulators but can pass through the local-thin Si regions between gate oxide and barrier insulators; the barrier insulator acts as a hard barrier. Since the local-thin Si region is very narrow along the surface channel region, distinct energy quantization should be assumed in the local-thin Si region even at high temperatures because $k_B T < E_{n1} - E_C$. Therefore, the bandgap of the Si region between the gate oxide layer

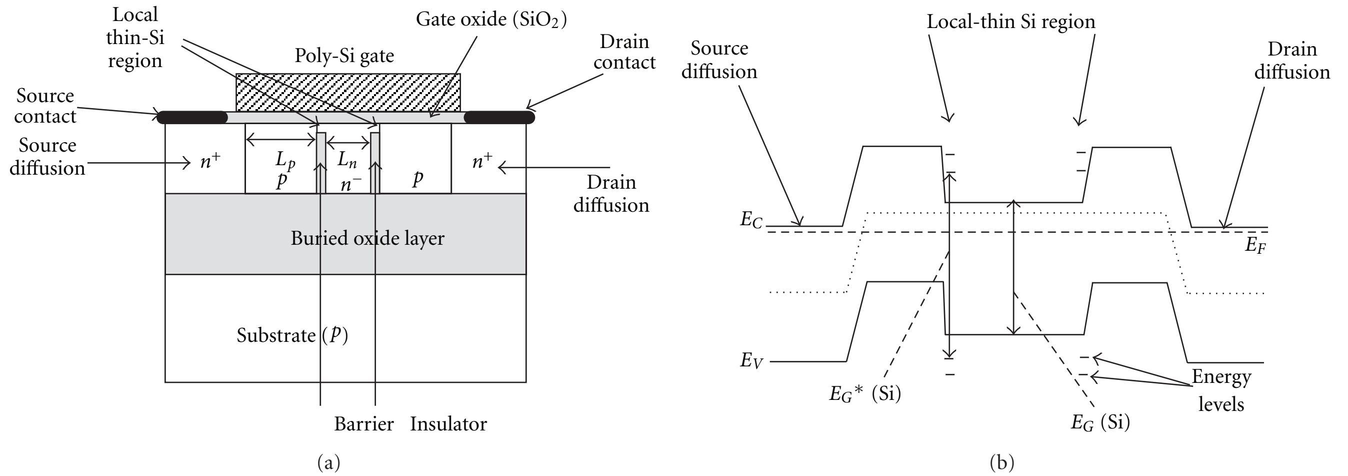

Figure 1: Schematic device structure of HTOT SOI MOSFET. (a) Schematic view of device. (b) Schematic band structure from source to drain at $V_d = 0$ V. E_G^* is the effective bandgap energy of ultrathin Si regions and $E_G^* > E_G$.

Figure 2: Possible fabrication process for HTOT SOI MOSFET.

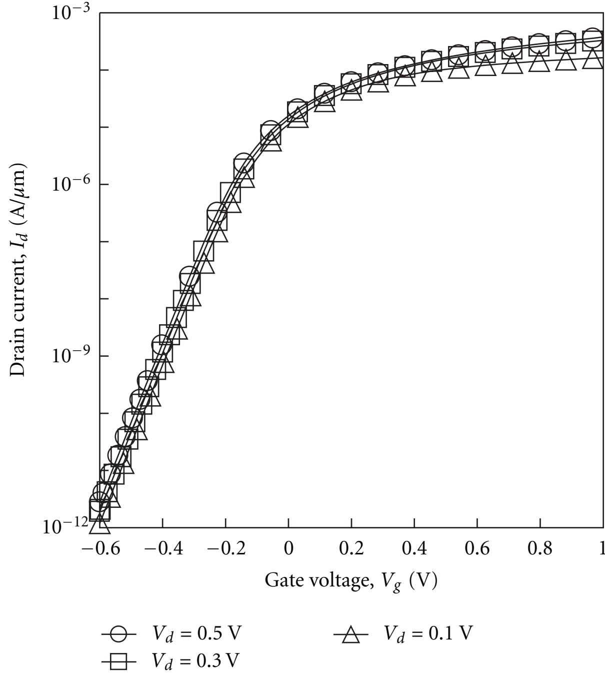

Figure 3: I_d-V_g characteristics of HTOT SOI MOSFET at 300 K for various drain voltage conditions. The device has a 40-nm long p-type region (L_p); $L_g = 100$ nm. The device has 1-nm-thick local-thin Si regions at both sides of n-type Si body.

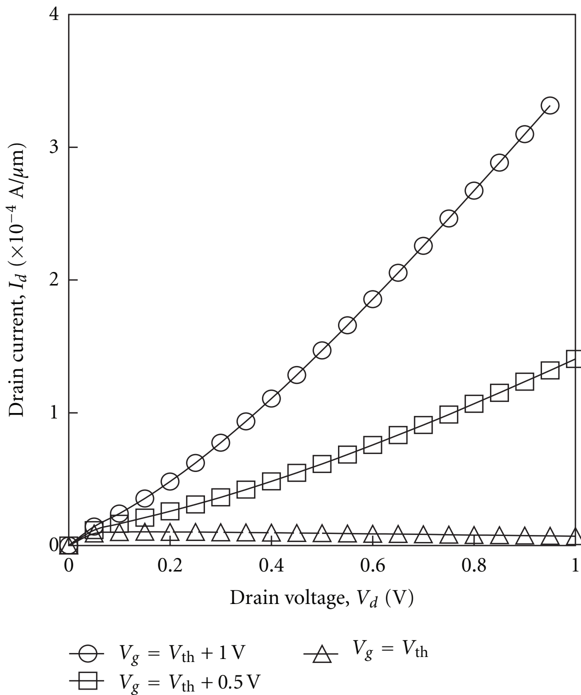

Figure 4: I_d- V_d characteristics of HTOT SOI MOSFET for various gate voltage conditions at 300 K. The device has a 40-nm long p-type region (L_p); $L_g = 100$ nm. The device has 1-nm-thick local-thin Si regions at both sides of n-type Si body.

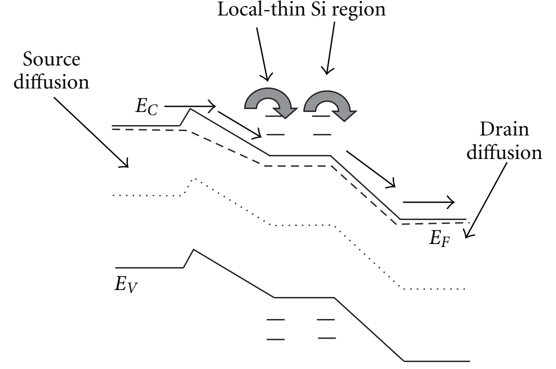

Figure 5: Schematic band diagram of HTOT SOI MOSFET from source to drain at $V_d \gg 0$ V.

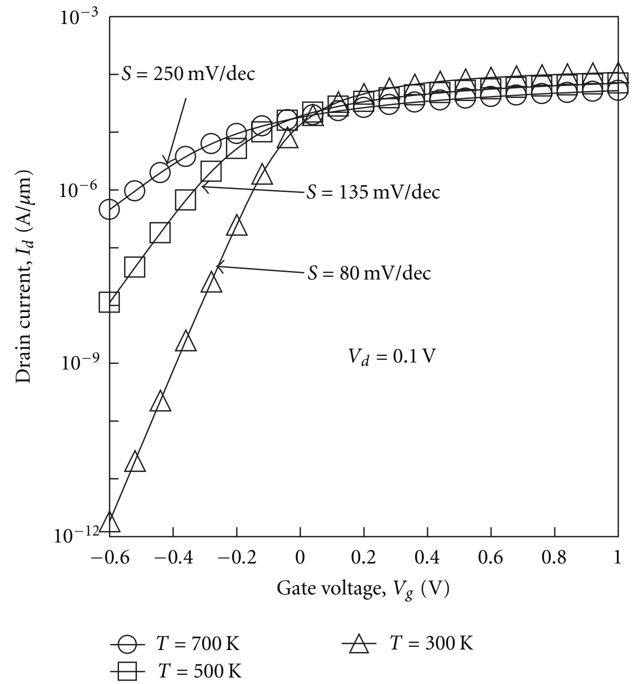

Figure 6: I_d-V_g characteristics of the conventional SOI MOSFET at $V_d = 0.1$ V for various temperature conditions. The device has a 10-nm thick SOI body.

and the barrier insulator is effectively widened which reduces the total drain current. In high-temperature environments the thermal energy of some carriers can exceed the ground-state level ($E_{n1} - E_C$ or $E_V - E_{p1}$) in the channel. Thus, it can be expected that both the drive current and off-current of an HTOT SOI MOSFET operating at high temperatures will be larger than those of a TBJ MOSFET [4, 5], while its subthreshold swing at high temperatures is superior to that of the conventional SOI MOSFET.

Figure 3 shows I_d-V_g characteristics of a HTOT SOI MOSFET with a 40-nm long p-type region (L_p) at 300 K for various V_d values; it is assumed that the HTOT SOI MOSFET has 1-nm-thick local-thin Si regions on both sides of the n-type Si body. It is seen that the HTOT SOI MOSFET has a

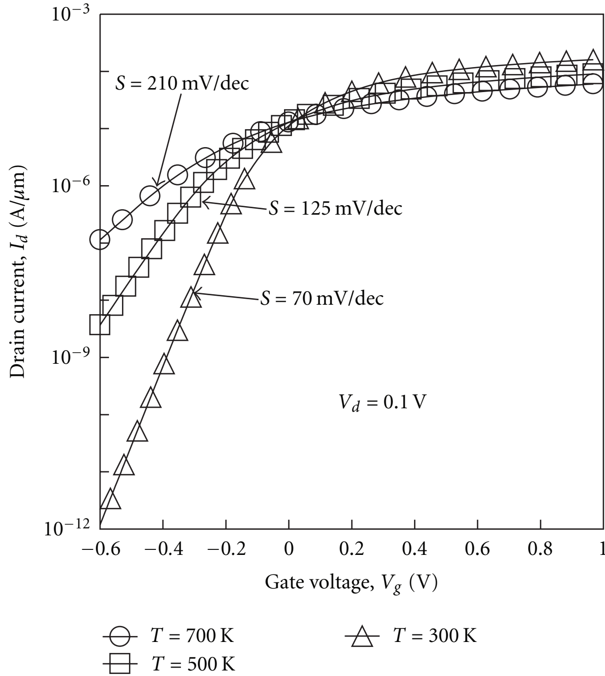

FIGURE 7: I_d-V_d characteristics of HTOT SOI MOSFET at V_d = 0.1 V for various temperature conditions. The device has a 40-nm long p-type region (L_p). The device has 1-nm-thick local-thin Si regions at both sides of n-type Si body.

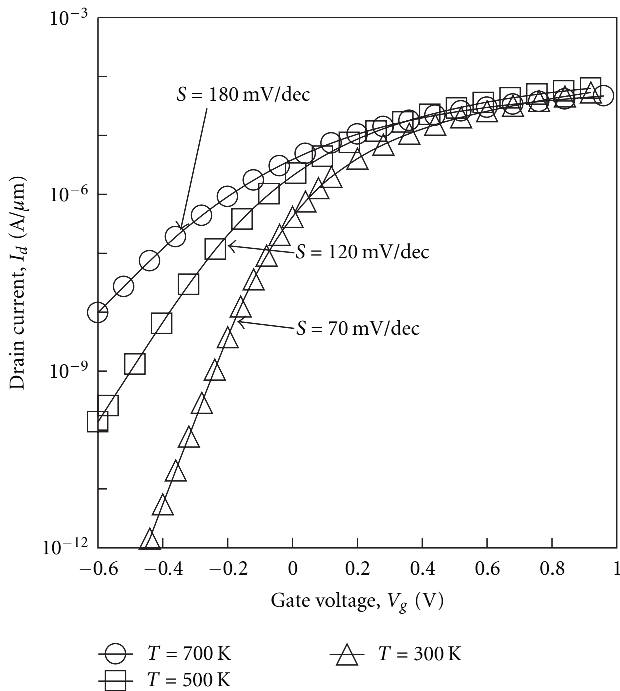

FIGURE 8: I_d-V_g characteristics of HTOT SOI MOSFET with 2-nm-thick and 10-nm-long local-thin Si regions at V_d = 0.1 V for various temperature conditions; L_p = 20 nm and L_g = 60 nm. It is assumed that the ground-state level of the conduction band of the local-thin Si region is higher by 0.1 eV than the conduction band bottom.

subthreshold swing value of ~70 mV/dec. and ON current of about 350 μA/μm at V_g = 1 V.

I_d-V_d characteristics of the HTOT SOI MOSFET at 300 K for various V_g conditions are shown in Figure 4 for L_p = 40 nm. It is also assumed that the HTOT SOI MOSFET has 1-nm-thick local-thin Si regions on both sides of the n-type Si body. In order to consider conduction mechanisms, the schematic band diagram of the HTOT SOI MOSFET is shown in Figure 5 for $V_d \gg 0$ V; arrows indicate carrier-flow paths in the energy space. Two characteristic behaviors are considered; (i) the super-linear increase in the drain current stems from the nonohmic conduction through the local-thin Si regions at the source side, (ii) the negative differential conductance at $V_g = V_{\mathrm{th}}$ stems from the high impedance created by the local-thin Si regions at the drain side.

With regard to the I_d-V_g characteristics of the TBJ MOSFET [4, 5] under the assumption of full tunneling and ballistic transport, the drain current curve shows a kink at around the threshold voltage (V_{th}) and the drain current is almost constant for $V_g > V_{\mathrm{th}}$. In Figure 4, however, the drain current of the HTOT SOI MOSFET smoothly increases around $V_g = V_{\mathrm{th}}$ and it increases monotonously for $V_g > V_{\mathrm{th}}$. This means that the drain current of the HTOT SOI MOSFET is ruled by the semiclassical mechanism.

3.2. High-Temperature Characteristics. This section discusses in detail the I-V characteristics of the HTOT MOSFET at temperatures ranging from 300 K to 700 K. The temperature dependencies of the I_d-V_g characteristics of the conventional SOI MOSFET with a 10-nm-thick p-type body and the HTOT SOI MOSFET with 1-nm-thick local-thin Si regions at the edges of 10-nm-thick n-type body at T = 300, 500, and 700 K are shown in Figures 6 and 7, respectively. Subthreshold swing at each temperature is also indicated in the figures. Little difference in subthreshold swing between the conventional SOI MOSFET and the HTOT SOI MOSFET is seen at T = 300 K in Figures 6 and 7. At 700 K, however, the difference in subthreshold swing is 40 mV/dec; the advantage of subthreshold swing of the HTOT SOI MOSFET is about 5%. The HTOT SOI MOSFET operates safely at 700 K with no thermal instability because of its expanded effective bandgap [8]. Thus the HTOT MOSFET *is somewhat superior* to the conventional SOI MOSFET in high-temperature operation. When the threshold voltage (V_{th}) is set to 0.3 V at the drain voltage (V_d) of 0.1 V at 700 K, the drain current of the HTOT SOI MOSFET has an on/off-dynamic range of about 1.7.

Next, device operations are discussed for the case wherein the energy levels in the 1-nm-thick local-thin Si region are quantized. When energy levels are quantized in the local-thin Si region, the effective conduction band bottom rises to the ground state energy level; consequently, the bandgap is effectively widened. When the local-thin Si region is 1-nm wide, the ground state energy level is higher by 0.26 eV than the conduction band bottom. In the following, I_d-V_g characteristics are simulated for two cases; the ground state energy level is higher by 0.1 or 0.2 eV than the conduction band bottom. In addition, the thickness of the "hard barrier"

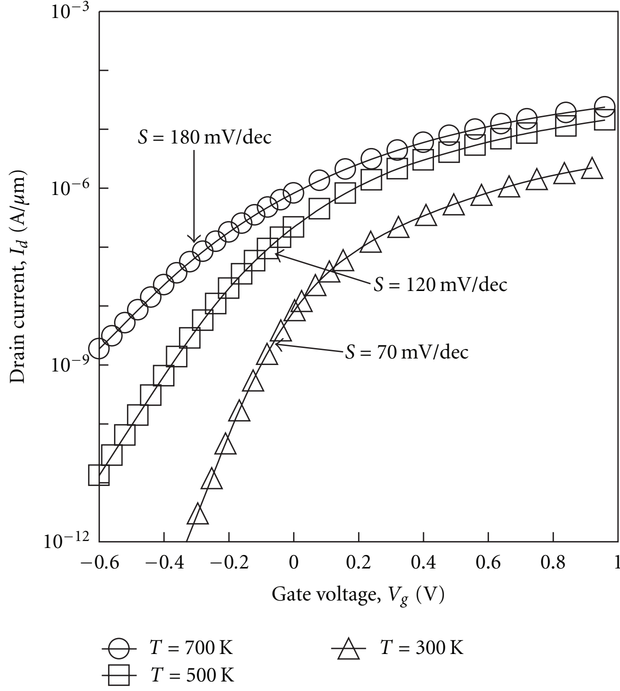

Figure 9: I_d-V_g characteristics of HTOT SOI MOSFET with 1-nm-thick and 10-nm-long local-thin Si regions at $V_d = 0.1$ V for various temperature conditions; $L_p = 20$ nm and $L_g = 60$ nm. It is assumed that the ground-state level of the conduction band of the local-thin Si region is higher by 0.2 eV than the conduction band bottom.

insulator adjacent to the local-thin Si regions is changed to 10 nm in order to clarify the influence of long and narrow conduction paths on overall carrier transport. In this case, $L_n = 10$ nm and $L_p = 20$ nm.

I_d-V_g characteristics depending on temperature (300 K ~ 700 K) for the HTOT SOI MOSFET at $V_d = 0.1$ V are shown in Figures 8 and 9 for $L_p = 20$ nm; in Figure 8, it is assumed that the ground state energy level of the local-thin Si region is higher by 0.1 eV than the conduction band bottom, and in Figure 9, it is assumed to be higher by 0.2 eV. The following points are found in Figures 8 and 9. (i) Subthreshold swing values are insensitive to the width of the local-thin-Si regions because subthreshold conduction is inherently similar to the thermionic process. (ii) Drain current at $V_g = 1$ V is sensitive to the width of the local-thin Si regions as expected because the long and narrow conduction path reduces channel conductivity. When energy levels of the conduction band in the local-thin Si region are discretely quantized, the ground state level in the local-thin Si regions should be higher than the conduction band bottom of the surface-inverted p-type region. (iii) The leakage current at $V_g = -0.6$ V is sensitive to the width of the local-thin Si regions because the electron density in the conduction band strongly depends on the "effective bandgap energy" ($E_G{}^*$).

Since the bandgap energy of the local-thin Si regions is larger than that of bulk Si, the intrinsic carrier density value of the local-thin Si regions (n_i^*) should be lower than that of the bulk Si (n_i) as expected by the following [8]:

$$n_i^*(T) = \left\{ \frac{\left(D_{\text{osn}} D_{\text{osp}}\right)^{1/2} k_B T}{t_S} \right\} \exp\left[-\frac{E_G^*}{2k_B T} \right], \qquad (3)$$

where D_{osn} and D_{osp} are the density of states of two-dimensional conduction-band electrons and the density of states of two-dimensional valence band holes, respectively. The density of states is a function of the effective mass; for simplicity, it is assumed the effective mass is independent of temperature. On the other hand, it is assumed that Debye length (L_D) and the intrinsic bandgap energy (E_G) is a function of temperature [9]. Equation (3) is quite valid for high temperatures because it was derived on the basis of high-temperature approximations. The conduction band of Si presents the electrons with an effective barrier height of $(E_G^* - E_G)/2$ and the thermionic emission current is controlled by the barrier of $(E_G^* - E_G)/2$. This barrier suppresses the subtreshold leakage current at high temperatures. Therefore, the thickness and length of the local-thin Si regions is a design issue and depends on the implementation demands.

Simulated threshold voltage (V_{th}) and subthreshold swing (S) at drain voltage of 0.1 V are summarized in Figure 10. It is assumed that the SOI layer has a (001) Si surface. The HTOT SOI MOSFET is compared to the conventional SOI MOSFET with a 10-nm-thick SOI layer. It is assumed in Figure 10(a) that the local-thin Si regions are 2-nm thick and 2-nm long. At room temperature, both devices show almost identical characteristics; only the threshold voltage is slightly different. However, the HTOT SOI MOSFET exhibits much lower performance degradation than the conventional SOI MOSFET; $\mathrm{d}V_{\text{th}}/\mathrm{d}T = -0.6$ mV/K and $\mathrm{d}S/\mathrm{d}T = 0.3$ mV/dec/K for the HTOT SOI MOSFET. When threshold voltage is set to 0.3 V at 700 K, the present HTOT SOI MOSFET has superior off-leakage, by a factor of 3, to the conventional SOI MOSFET. The threshold voltage of the HTOT SOI MOSFET is higher than that of the SOI MOSFET by about 0.2 V; this is slightly larger than $(E_{n1} - E_C)/q$ be-cause electrons contributing to the threshold current should have the averaged energy slightly larger than $(E_{n1} - E_C)$ at the threshold [21].

In Figure 10(b), simulated threshold voltage (V_{th}) and subthreshold swing (S) are shown at the drain voltage of 0.1 V for 1-nm-thick local-thin Si regions; the HTOT SOI MOSFET is compared to the conventional SOI MOSFET with a 10-nm-thick SOI layer. The results demonstrate that the HTOT SOI MOSFET has outstanding performance: $\mathrm{d}V_{\text{th}}/\mathrm{d}T = 0.0$ mV/K and $\mathrm{d}S/\mathrm{d}T = 0.25$ mV/dec/K. Subthreshold swing of the HTOT SOI MOSFET is about 178 mv/dec at 700 K (427 C). It should be noted that the HTOT SOI MOSFET with 1-nm-thick local-thin Si regions is almost insensitive to temperature for $T < 700$ K (427 C). The mechanism is the same as that described previously.

Finally, I_{ON} versus I_{OFF} characteristics of the HTOT SOI MOSFET are shown in Figure 11 at $V_d = 0.1$ V. Slopes of curves range from −5 to −8. The reduction in on-current values at high temperatures is due to mobility degradation, and the drastic increase in off-current at high temperatures is due to the thermionic emission process. It is seen that the difference

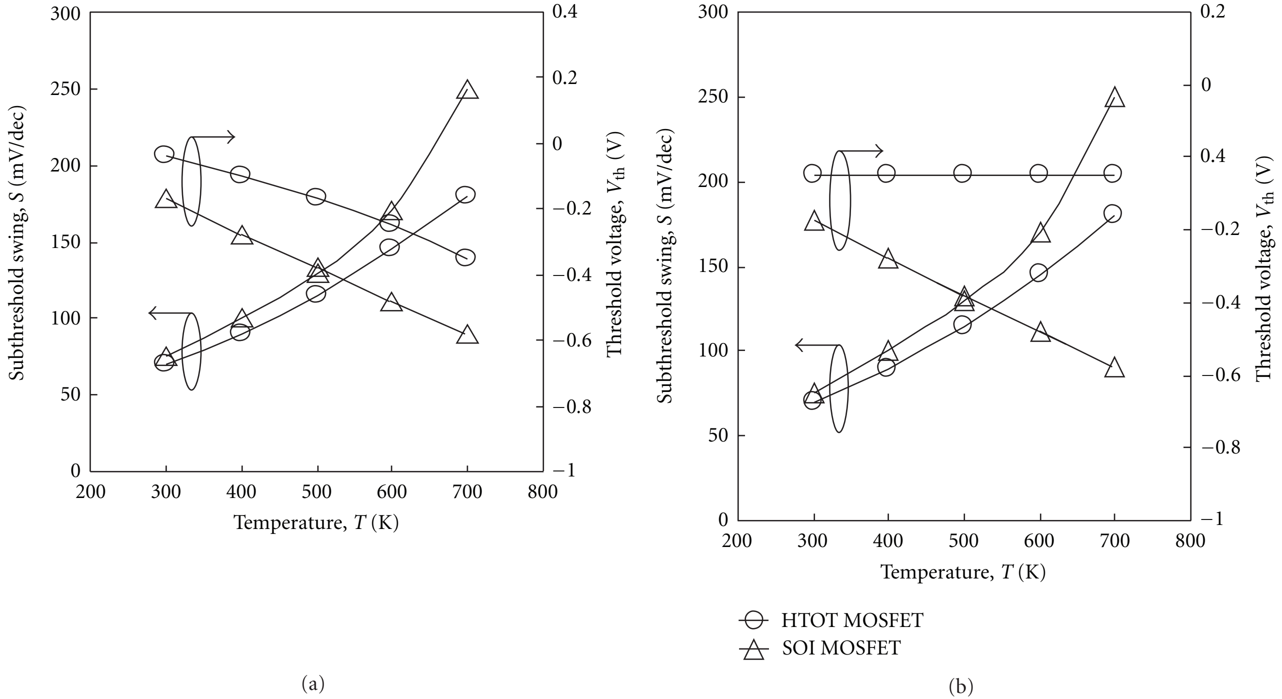

Figure 10: Temperature dependence of subthreshold swing and threshold voltage: HTOT SOI MOSFET compared to conventional SOI MOSFET with a 10-nm-thick SOI layer. (a) Characteristics of HTOT SOI MOSFET with 2-nm-thick local-thin body. (b) Characteristics of HTOT SOI MOSFET with 1-nm-thick local-thin body.

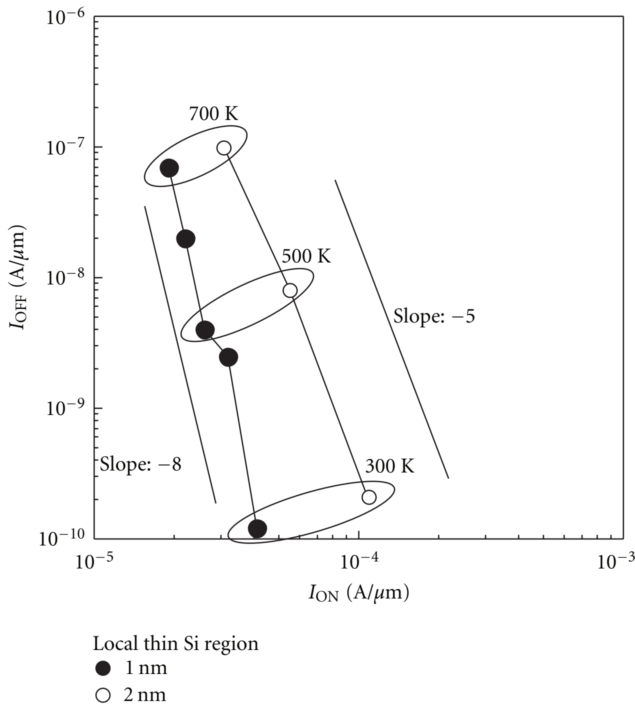

Figure 11: I_{ON} versus I_{OFF} characteristics of HTOT SOI MOSFET at $V_d = 0.1$ V. It is assumed that $V_{th} = 0.3$ V. I_{ON} is defined at $V_g = V_{th} + 0.7$ V, and I_{OFF} is defined at $V_g = V_{th} - 0.3$ V.

in local thin Si region thickness primarily impacts the on-current value (I_{ON}), and that the off-current value (I_{OFF}) is not so sensitive to the local-thin Si region thickness; these are important aspects of the HTOT SOI MOSFET from the view-point of device design.

4. Conclusion

This paper proposed the High-Temperature-Operation Tolerant (HTOT) SOI MOSFET and demonstrated preliminary device simulation results of its characteristics.

The HTOT SOI MOSFET has local-thin Si regions and operates safely at 700 K with no thermal instability because of its expanded effective band gap. A HTOT SOI MOSFET with 2-nm-thick local-thin body regions exhibits much lower performance degradation than the conventional SOI MOSFET; $dV_{th}/dT = -0.6$ mV/K and $dS/dT = 0.3$ mV/dec/K for the HTOT SOI MOSFET. Subthreshold swing of the HTOT SOI MOSFET is about 180 mv/dec at 700 K (427 C). Threshold voltage of the HTOT SOI MOSFET is higher than that of SOI MOSFET by about 0.2 V because the local-thin Si regions offer an expanded effective band gap.

An HTOT SOI MOSFET with 1-nm-thick local-thin Si regions shows outstanding performance: $dV_{th}/dT = 0.0$ mV/K and $dS/dT = 0.25$ mV/dec/K. Subthreshold swing of the HTOT SOI MOSFET is about 178 mv/dec at 700 K (427 C). Therefore, the HTOT SOI MOSFET is a promising device for future high-temperature applications when its device parameters are appropriately optimized.

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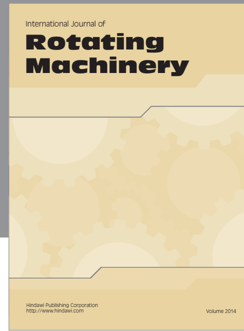
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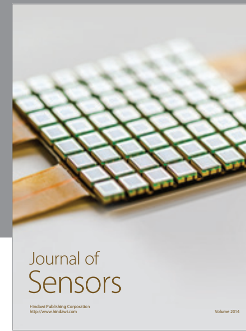
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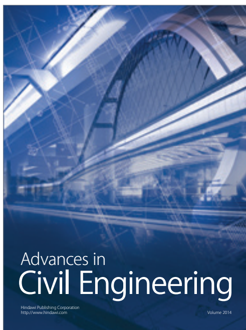
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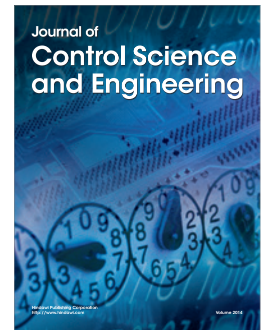
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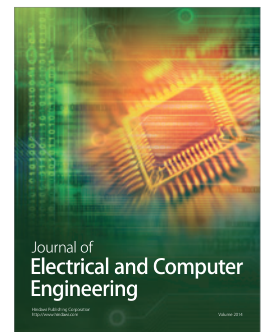
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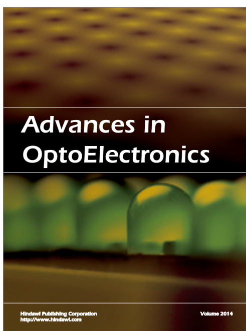
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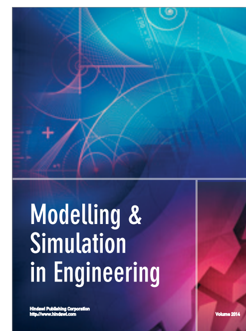
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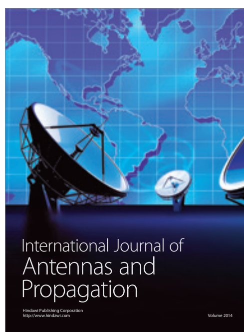
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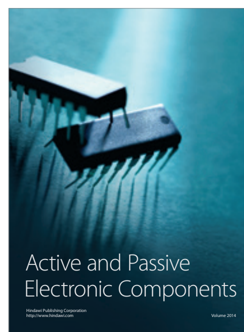
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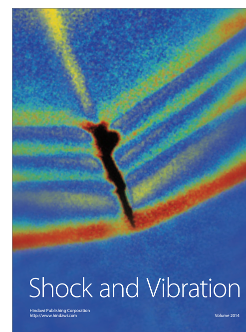
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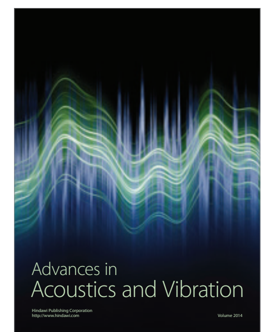
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