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Research Article

Comparative Study of SiO_2, Al_2O_3, and BeO Ultrathin Interfacial Barrier Layers in Si Metal-Oxide-Semiconductor Devices

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In a previous study, we have demonstrated that beryllium oxide (BeO) film grown by atomic layer deposition (ALD) on Si and III-V MOS devices has excellent electrical and physical characteristics. In this paper, we compare the electrical characteristics of inserting an ultrathin interfacial barrier layer such as SiO_2, Al_2O_3, or BeO between the HfO_2 gate dielectric and Si substrate in metal oxide semiconductor capacitors (MOSCAPs) and n-channel inversion type metal oxide semiconductor field effect transistors (MOSFETs). Si MOSCAPs and MOSFETs with a BeO/HfO_2 gate stack exhibited high performance and reliability characteristics, including a 34% improvement in drive current, slightly better reduction in subthreshold swing, 42% increase in effective electron mobility at an electric field of 1 MV/cm, slightly low equivalent oxide thickness, less stress-induced flat-band voltage shift, less stress induced leakage current, and less interface charge.

1. Introduction

The CMOS scaling is bringing the SiO_2 thickness below 1.5 nm. For these very thin oxides, the leakage current becomes unacceptably large. One way to reduce the leakage current is the substitution of the SiO_2 by a material with a higher dielectric constant. The main advantage of high-k dielectrics is the low gale leakage achieved due to its high physical thickness. That also makes it attractive for low power applications. Because of these requirements, over the past 10 years, hafnium oxide (HfO_2) has gained considerable interest as a high dielectric constant material for fabricating complementary metal oxide semiconductor (CMOS) devices. It has several attractive properties such as a high dielectric constant, good thermodynamic stability with Si, and good electrical properties [1]. Unfortunately, some of the other physical properties like mobility reduction, charge trapping, and threshold voltage (V_{th}) instability are a major drawback for the performance of metal oxide semiconductor field effect transistors (MOSFETs) [2]. Especially HfO_2 high-k dielectric stacked MOSFETs were reported with low carrier mobility [3]. The main cause for the low mobility is still unknown, but has been attributed to remote Coulomb scattering caused by charges in the high-k dielectric [4] or optical phonon scattering [5]. Many researchers have believed that it is inevitable for all high-k dielectrics to have low energy bandgap and high scattering, compared to SiO_2. Therefore, if high-k dielectric with high energy bandgap and low scattering can be found, it will be the true solution for the above problems.

An alternative promising high-k gate dielectric material is beryllium oxide (BeO), which has superior interface stability [6–10] and is already known as an excellent gas diffusion barrier. This makes it a potentially suitable diffusion barrier

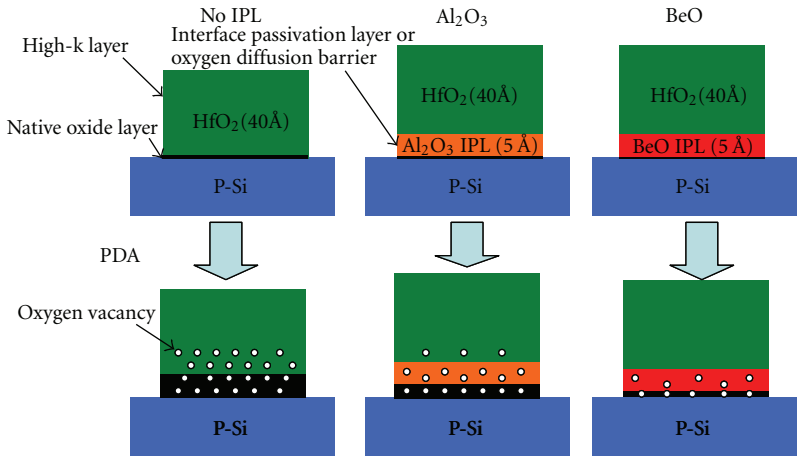

Figure 1: Cross-sectional MOS devices with various IL. The BeO interfacial layer is placed between HfO_2 and p-type Si substrate.

between HfO_2 and Si in CMOS processing. BeO also has metal-like thermal conductivity and a large energy bandgap (10.6 eV). These properties are indicative of low optical phonon and remote Coulomb scattering. Generally, a flow of phonons is responsible for heat conduction in dielectric materials. As the temperature increases, phonon density increases, but above 20 K, the phonon-phonon interaction becomes dominant and reduces the mean free path of the phonon drift, degrading thermal conductivity in the dielectrics [11]. BeO, however, has high thermal conductivity due to low phonon scattering because electrons in BeO are tightly and closely bound, so that the phonons in BeO are coupled to each other and have low energy and long wavelengths (or low phonon frequency). The high energy bandgap and band offset of BeO on Si makes intrinsic charge trapping difficult and results in a low trapped charge in the BeO dielectric (trapped charges in high-k dielectrics are the source of Coulomb scattering) [10]. Our previous studies have showed electrical and physical characteristics that BeO deposited with dimethylberyllium and water improves interface quality on III-V MOS devices by preventing sub-oxidation between high-k and III-V substrate during PDA [6]. In this paper, we compare the effect of interfacial barrier layer by inserting ultrathin SiO_2, Al_2O_3, or BeO barrier layer (IL) between the HfO_2 gate dielectric and Si substrate in metal oxide semiconductor capacitors (MOSCAPs) and NMOSFETs. The aim of using such a barrier layer was to improve the device performance and reliability while maintaining, as much as possible, the overall dielectric constant of the resulting film.

2. Fabrication Procedure

An ALD BeO IL was deposited on HF-last p-type Si substrates using dimethylberyllium precursors and water as an oxygen source. As a reference, ALD Al_2O_3 IL was deposited on the same cleaned substrate using trimethylaluminum and the same oxygen source. Samples with a BeO IL, Al_2O_3 IL, and without an IL were followed by ALD HfO_2. They were annealed for 3 min at 600°C in N_2 at atmospheric pressure. The physical thickness of the BeO and Al_2O_3 IL layers was controlled from the deposition rate which was measured on the bulk oxide using multiple-wavelength (200~900 nm) ellipsometry. The TaN electrode was deposited using reactive dc magnetron sputtering at 2000 Å followed by reactive ion etching (RIE) with Ar + CF_4 after electrode patterning of the gate. The source/drain (S/D) regions of NMOSFETs were implanted with phosphorus at 50 keV and a dose of 5×10^{15} cm^{-2}. High temperature (900°C, 1 min) annealing in N_2 ambient was used for S/D activation. E-beam evaporated Ni/AuGe/Au was used for both S/D and backside metallization. The final sintering was done at 400°C in forming gas for 30 min. For all MOSCAPs samples, PMA (500°C, 2 min) was done.

3. Results and Discussion

Figure 1 shows the cross-sectional MOS structure with various IL (or IPL). It is constructed based on the electrical and physical results in the previous experiments [10]. SiO_2, Al_2O_3, or BeO IL is placed between HfO_2 and the P-Si substrate. Al_2O_3 and BeO IL are intentionally inserted, but SiO_2 IL is thermally grown during post-deposition and S/D activation anneals. In Figure 2, the BeO(IL)/HfO_2 structures show the lowest leakage, comparable to those of SiO_2(IL)/HfO_2 and Al_2O_3(IL)/HfO_2 gate stacks. Insertion of BeO IL (5~10 Å) doesn't increase the EOT significantly after the post-deposition anneal (PDA) due to the efficient suppression of the oxygen diffusion during PDA. The effectiveness of oxygen diffusion barrier for BeO IL is more presented as the annealing temperature increases in Figure 3. BeO IL may have some advantage for EOT scaling and reliability improvement After S/D activation, around 15 Å SiO_2 is grown at the interface between HfO_2 and the Si substrate. The low EOT of BeO IL is an indication of efficient oxygen diffusion barrier. The similar results were presented using X-ray photoelectron spectroscopy (XPS) [10]. Oxygen diffusion through thin films is proportional to the number and size of pinholes in the respective film [12]. In general, smaller pinholes cause more collisions between the diffusing

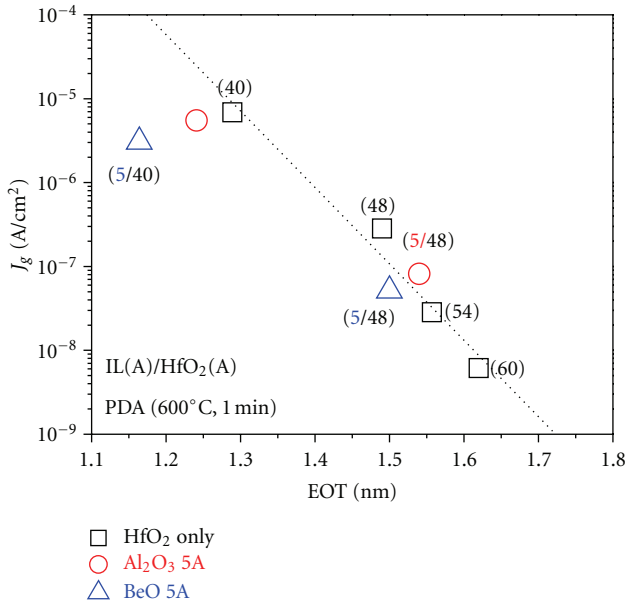

FIGURE 2: Gate leakage current versus EOT for SiO_2/HfO_2, Al_2O_3(IL)/HfO_2, and BeO(IL)/HfO_2 gate stacks.

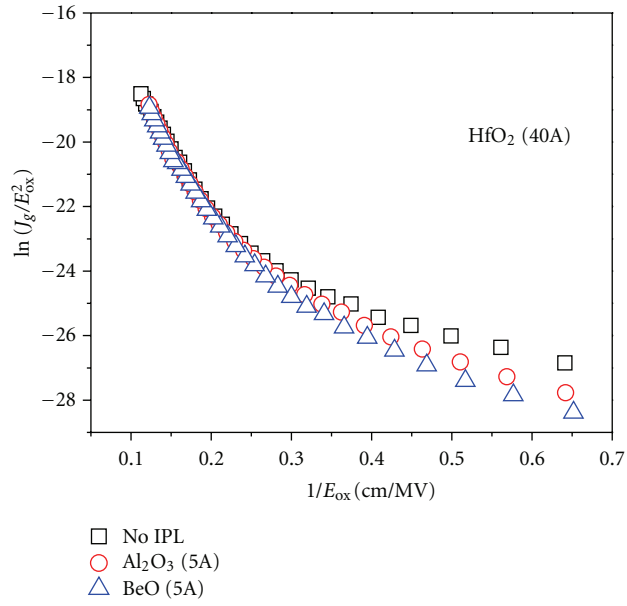

FIGURE 4: F-N plots to compare the effective potential barrier height for three different gate stacks.

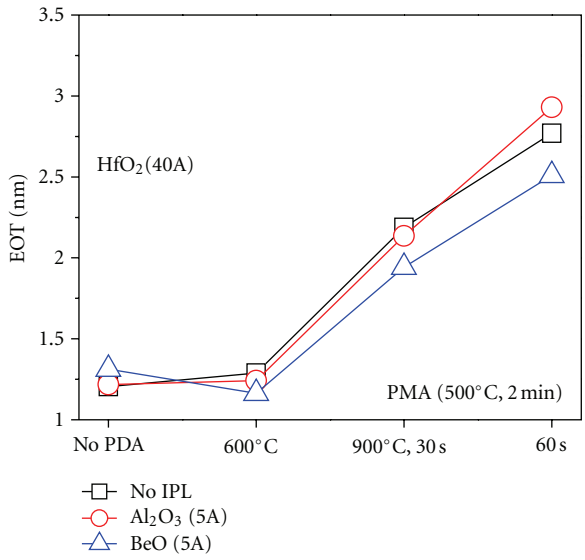

FIGURE 3: The change of EOT with the annealing temperature and duration for three different gate stacks.

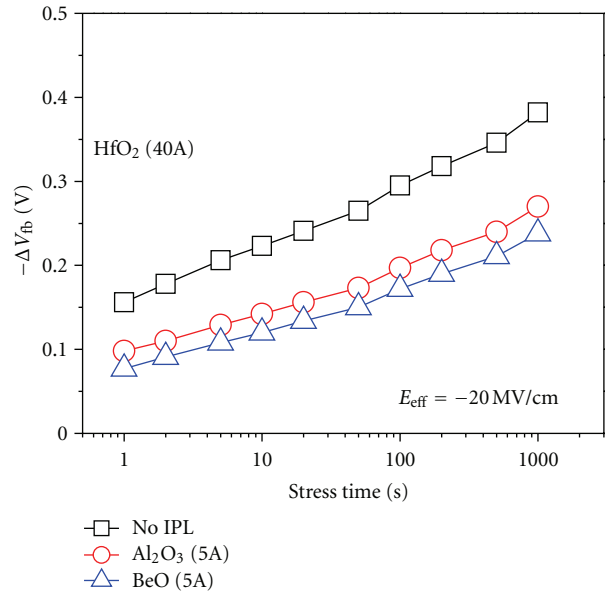

FIGURE 5: Stress-induced V_{fb} shift (ΔV_{fb}) versus stress time for three different gate stacks. $E_{eff} = (V_g - V_{fb})$/EOT.

molecules (e.g., oxygen) and the chemical groups present in the bulk film, reducing the rate of permeation. For reasons that are still under investigation, films of BeO, which have small molecular size, appear to exhibit relatively low oxygen diffusivity and are capable of effectively blocking the diffusion of impurities, such as Hf, thus minimizing defects in the substrate.

In general, the bandgap of the high-k material is inversely proportional to its permittivity, but BeO is an exception, having a very large energy bandgap (10.6 eV) combined with a still high dielectric constant of 6.8. As the bandgap, or correspondingly, band offset increases, a charge trapping in the dielectric decreases. The effective potential barrier heights for SiO_2/HfO_2, Al_2O_3(IL)/HfO_2, and BeO(IL)/HfO_2 gate stacks are compared using the Fowler-Nordheim plot in Figure 4. Due to bilayer gate structure, exact number of the effective barrier height is not extracted. But a higher barrier of the BeO IL stack is observed and it may results in the smaller electron tunneling currents, compared to other different gate stacks. Figures 5 and 6 are the representative results of reliability statistics characteristics. In Figure 5,

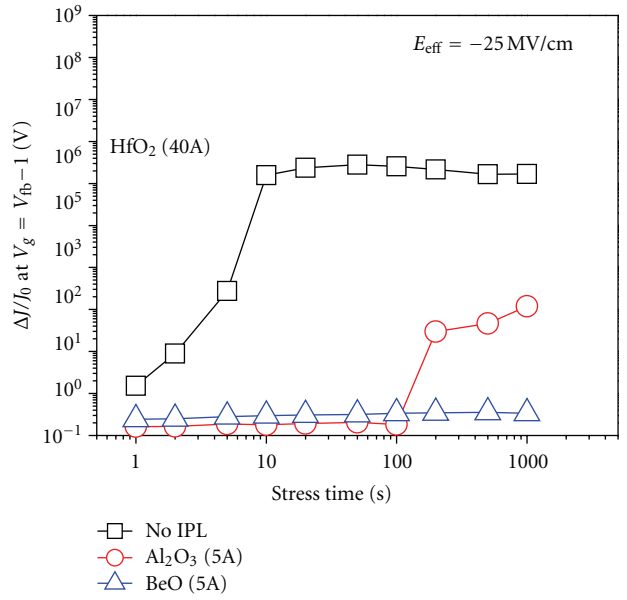

FIGURE 6: Stress-induced leakage current ($\Delta J_g/J_0$) versus stress time. $E_{eff} = (V_g - V_{fb})/EOT$.

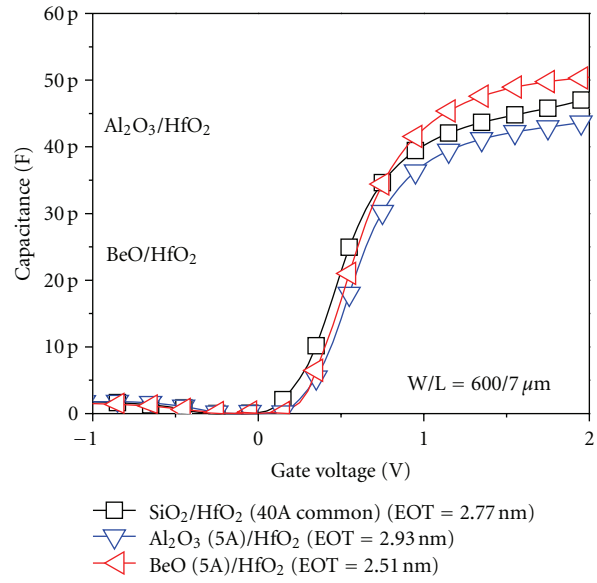

FIGURE 7: NMOSFETs inversion capacitance for three different gate stacks.

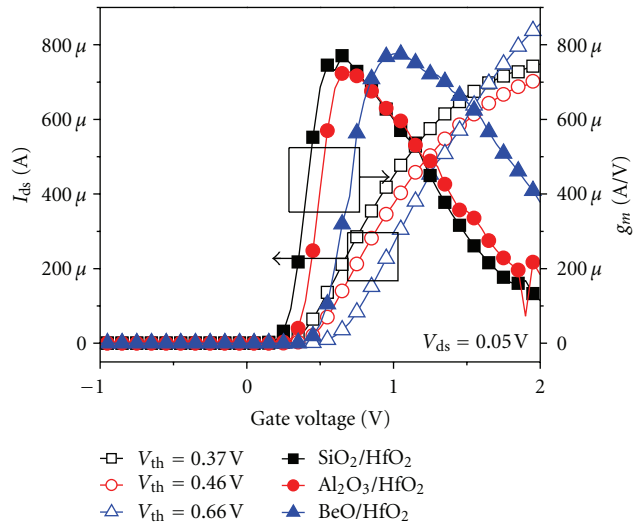

FIGURE 8: NMOSFETs $I_d - V_g$ characteristics of three gate stacks. BeO IL shows slightly higher V_{th}, G_m, and I_d.

the $BeO(IL)/HfO_2$ gate stack shows less initial V_{fb} shift (after 1 sec stress) indicating fewer preexisting traps in the dielectric. A slightly smaller trap generation rate was also observed compared to other two gate stacks. In Figure 6, the $BeO(IPL)/HfO_2$ also shows the reduced stress-induced leakage current (SILC) degradation and no significant breakdown. But SiO_2/HfO_2 and $Al_2O_3(IL)/HfO_2$ show gradual breakdown with stress time. The lower trap generation rate and the reduced tunneling current of the $BeO(IPL)/HfO_2$ gate stack may improve the reliability characteristics and it may be the indication of the high structural stability. In the view point of thermodynamics of materials, the total entropy of a material consists of its thermal entropy, which is related to thermal conductivity, and configurational entropy, which is related to the crystallization (or crystallinity) of the material [13]. With high crystallinity and thermal conductivity, BeO may have high total entropy, and it means that BeO is more structurally stable, compared to other gate dielectrics, even though the direct correlation between thermodynamic stability and device performance is still questionable. For more details of BeO thermal stability, please see the reference [14]

Figure 7 is NMOSFET inversion capacitance for SiO_2/HfO_2 (40 Å), Al_2O_3(5 Å)/HfO_2 (40 Å), and BeO(5 Å)/HfO_2 (40 Å) gate stacks. The BeO/HfO_2 gate stack shows a slightly lower equivalent oxide thickness (EOT) (2.51 nm) than SiO_2/HfO_2 (2.77 nm) and Al_2O_3/HfO_2 (2.93 nm) even though the EOTs for all gate stacks significantly increased after S/D activation annealing (Figure 3). From the XPS analysis, EOT increase is mainly due to the oxygen in HfO_2 dielectric, instead of oxygen residue in anneal tool [10]. For SiO_2/HfO_2, Al_2O_3/HfO_2, and BeO/HfO_2 gate stacks, 1.7 nm, 1.5 nm, and 1.0 nm are expected for native oxide to be grown, respectively, based on Figure 3 results. Figure 8 shows NMOSFET drain current-gate voltage ($I_d - V_g$) characteristics of SiO_2/HfO_2, Al_2O_3/HfO_2, and BeO/HfO_2 gate stacks. With the slightly lower EOT, the BeO/HfO_2 stack exhibits more positive V_{th} (0.66 V), higher drive current at V_g = 2 V, and better subthreshold swing (69 mV/dec), compared to those of the SiO_2/HfO_2 stack (V_{th} = 0.37 V, SS = 77 mV/dec) and Al_2O_3/HfO_2 stack (V_{th} = 0.46 V, SS = 70 mV/dec). The threshold voltage equation obtained from an ideal MOS structure [15] is

$$V_{th} = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F, \quad (1)$$

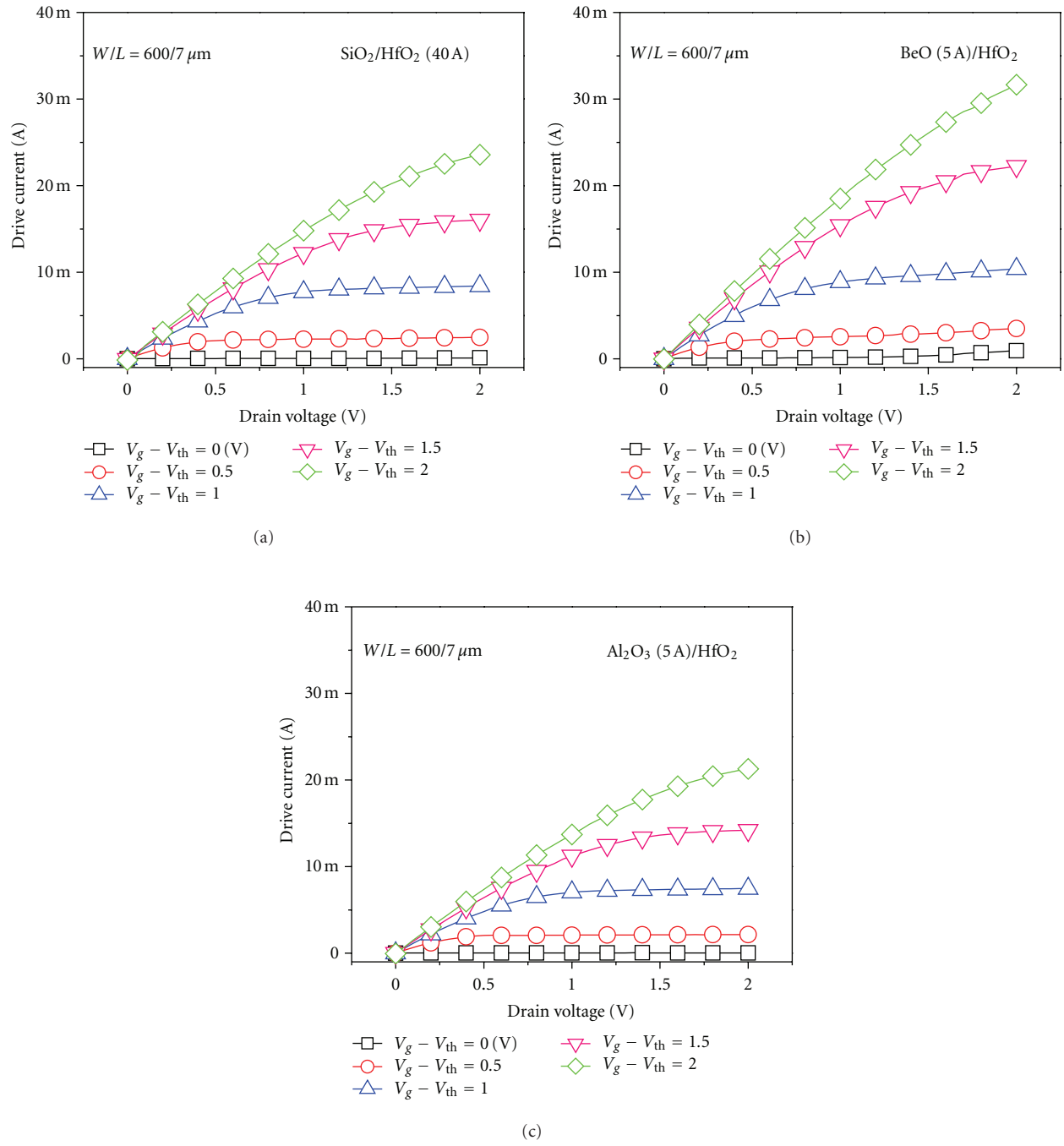

FIGURE 9: $I_d - V_d$ characteristics of three gate stacks. BeO IL shows significant increased drive current compared to SiO_2 and Al_2O_3 IL gate stacks.

where Φ_{ms}, Q_i, Q_d, and ϕ_F are the work function differences between the metal and semiconductor ("−" value), interface charge ("+" value), depletion charge ("−" value) for the n-channel, and energy differences between the intrinsic energy level and Fermi energy level (+) for the n-channel, $\phi_F = (E_i - E_F)/q$. If we assume that Φ_{ms}, Q_d, and ϕ_F are the same for all gate stacks because the only difference is interfacial layer, then the positive shift of V_{th} of the BeO/HfO_2 stack is due to the less positive interface charges between BeO and the Si substrate. The fewer fixed charges in BeO layer may contribute to the fewer interface charges [10].

In Figure 9, the BeO/HfO_2 stack shows around 34% higher drive current (31.67 mA) at $V_d = 2$ V & $V_g - V_{th} = 2$ V than the SiO_2/HfO_2 stack (23.56 mA) and Al_2O_3/HfO_2 stack (21.28 mA). Only 5 Å BeO insertion between high-k and Si channel makes the drive current much improved. There is some reduction of drive current with the IL thickness increase for both the Al_2O_3/HfO_2 and BeO/HfO_2

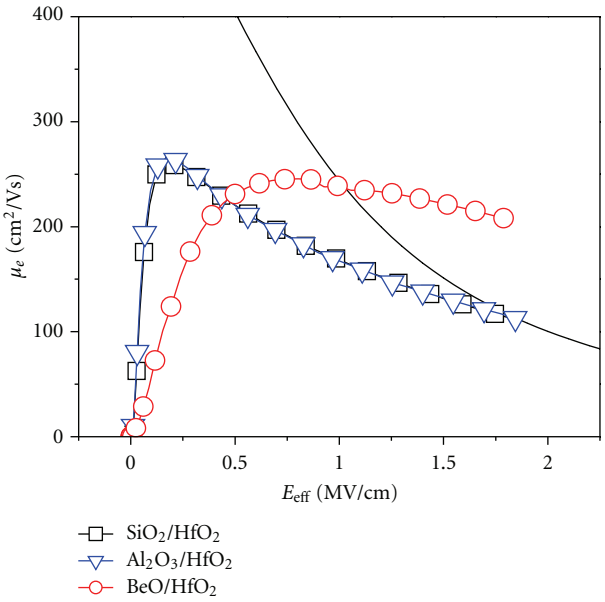

FIGURE 10: Effective channel mobility of NMOSFETs with three gate stacks.

gate stacks, but it is more significant on Al_2O_3/HfO_2 stack. It may be due to the less native interfacial oxide (SiO_2) growth for Al_2O_3/HfO_2, stack. Figure 10 illustrates the effective channel electron mobility using the split capacitance-voltage (C-V) method. The BeO/HfO_2 stack shows a 42% higher effective field (E_{eff}) mobility (238 cm^2/Vs) than SiO_2/HfO_2 (167 cm^2/Vs) and Al_2O_3/HfO_2 (166 cm^2/Vs) at E_{eff} = 1 MV/cm. It may require further investigation to confirm and explain these results. The electron mobility in SiO_2/HfO_2 and Al_2O_3/HfO_2 are fast-saturated to the universal trend, likely due to the thick SiO_2 interfacial layer grown during S/D activation. If the SiO_2 interfacial layer is thinner, the peak electron mobilities of the HfO_2 gate stack will decrease significantly [16]. In atomic configuration, physical roughness difference between amorphous Al_2O_3 and crystalline BeO is similar, but in electronic configuration, the electropotential roughness between them is quite different. In terms of electrostatic potential roughness, the two-dimensional ordered arrays of atoms on a crystalline surface generally give atomic scale surface height fluctuation, which exhibits low electrostatic potential roughness [17]. In a previous study, we demonstrated that ALD BeO on Si grows almost epitaxially [7], thereby may improve surface electro-potential roughness and high field electron mobility.

In this work, a BeO (IL)/HfO_2 gate stack was investigated and systematically compared to a SiO_2/HfO_2 gate stack. Inserting an ALD BeO IL between the Si channel and high-k gate dielectric enhances high field carrier mobility and improves MOSFET parameter and reliability characteristics while maintaining a similar EOT. Excellent BeO properties, such as a high energy bandgap, efficient oxygen diffusion barrier, and high crystallinity, improve the charge trapping, the suppression in EOT increase during S/D activation, and MOSFET performance, thus imparting significant advantages to MOS devices with a BeO IL.

Acknowledgments

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