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Research Article

A 12 GHz 30 mW 130 nm CMOS Rotary Travelling Wave Voltage Controlled Oscillator

G. Jacquemod,[1] F. Ben Abdeljelil,[2] L. Carpineto,[3] W. Tatinian,[2] and M. Borgarino[4]

[1] *University Nice Sophia Antipolis, IM2NP UMR CNRS 7334, 06410 Biot, France*
[2] *University Nice Sophia Antipolis, LEAT UMR CNRS 6071, 06540 Valbonne, France*
[3] *SDRF, Sophia Antipolis, 06410 Biot, France*
[4] *University of Modena and Reggio Emilia, 41100 Modena, Italy*

Correspondence should be addressed to G. Jacquemod, gilles.jacquemod@unice.fr

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This paper reports a 12 GHz rotary travelling wave (RTW) voltage controlled oscillator designed in a 130 nm CMOS technology. The phase noise and power consumption performances were compared with the literature and with telecommunication standards for broadcast satellite applications. The RTW VCO exhibits a −106 dBc/Hz at 1 MHz and a 30 mW power consumption with a sensibility of 400 MHz/V. Finally, requirements are given for a PLL implementation of the RTW VCO and simulated results are presented.

1. Introduction

In a Ku-band satellite receiver, usually the signal picked up by the dish antenna is amplified by a low noise block (LNB) designed with compound semiconductor HEMT (high electron mobility transistor) and the local oscillator is a dielectric resonator oscillator (DRO) [1]. Recently, efforts have been made to design a satellite receiver using CMOS technologies [2, 3]. In [2] the design was focused on the receiver chain only (LNA and mixer) while in [3] the whole LNB was addressed, where the receiver exhibits a traditional superheterodyne and the local oscillator is a traditional differential VCO. Because of the image frequency issue, the RF designer should introduce image rejection filters, facing therefore all the related troubles.

Solutions alternative to the traditional approach (superheterodyne architecture plus image rejection filter) can be envisaged at architectural level in two ways: an image rejection architecture or a direct conversion architecture. In the former solution the architecture is an interferometric structure where the image frequency signal destructively interferes with itself while the desired RF signal constructively interferes with itself. In the latter solution image and RF signal coincide. Both above cited solutions require a demodulator configuration where a couple of mixers are driven by differential in quadrature signals. Their generation is usually obtained using quadrature VCOs, as preferred solution with respect to polyphase filters, ring oscillators, or frequency dividers.

In particular, in the present paper, a rotary travelling wave voltage controlled oscillator (RTW VCO) in a 130 nm CMOS technology is investigated having in mind the idea of improving the Ku-band satellite receiver architecture by replacing the previously sketched out traditional superheterodyne architecture with an image rejection architecture, so that the image frequency rejection filters can be avoided in the receiver design.

In the design of the VCO attention should be paid to the phase noise, which is a very stringent specification for the satellite broadcasting, because of the use of amplitude and phase shift keying (APSK) modulation schemes that make the constellation round and therefore prone to suffer from cycle slips if the phase noise of the local oscillator is too high.

In order to optimize the phase noise performances of the RTW VCO, an impulse sensitivity function (ISF) based model and the design guidelines for required transmission line are proposed.

Table 1: PLL specifications.

Characteristics	Specifications
Frequency band of the input signal	12.2–12.7 GHz
Output frequency (IF)	950–1450 MHz
Local oscillator frequency	11.25 GHz
Local oscillator stability	<1.5 MHZ (30°C–60°C)
Phase noise	< −95 dBc/Hz at 100 kHz
	< −115 dBc/Hz at 1 MHz

The paper is organized as follows. In Section 2, the PLL specifications, its architecture, and its different blocks are presented. Section 3 deals with the RTW oscillator architecture and the corresponding line theory is proposed. Phase noise considerations are presented in Section 4. Section 5 is dedicated to the measurement results and Section 6 is devoted to the design and simulation of the PLL performance, in terms of transient response and phase noise error. Finally, the paper ends with drawing some conclusions in Section 7.

2. PLL Specifications and Design

Figure 1 depicts a Ku-band satellite heterodyne receiver. In this paper, we suggest replacing the DRO of local oscillator (LO), which has a very good stability but a very high cost, with a CMOS PLL. The first generation architecture for satellite receiver was not image rejection mixer. Nevertheless, a QVCO (RTW) is chosen to realize this PLL in order to implement image rejection architecture for the mixer, easing the requirement for the input filter and it is not presented in this paper. The specifications of this PLL are summarized in Table 1. The second oscillator (IF to base band, BB) is a classical PLL, with a tuning range from 1 to 1.5 GHz, without any specific design challenges.

For the band translation switch satellite application, settling time is not a mandatory requirement as in GSM or any standard using hopping (as Bluetooth). Nevertheless, the PLL itself would lock within five times the loop time constant. The loop bandwidth was set for best noise performances to be around 550 to 600 kHz.

The chosen PLL architecture is a classical analog PLL topology, as depicted in Figure 2. The reference frequency is generated by a 50 MHz quartz oscillator. The satellite application forces the output frequency to be around 12 GHz [4].

With the exception of the RTW VCO (described in Section 3), we present in the following paragraphs the various blocks of the PLL.

To divide by N the output frequency, a series of three dividers are used due to the relatively high value of the rand division ($N = 12\,\text{GHz}/50\,\text{MHz}$). Indeed, depending of the working frequency, different divider topologies can be used to get better efficiency [5]. As a consequence, the first divider is a fixed division (by 4 in our case) [6], the second one is a CML [7] divider by 8, and the last one is a CML dual modulus 7/8 frequency divider.

The phase/frequency detector (PFD) is a conventional one. It is based on D-type registers, customized to limit the dead zone. This PFD reduces the nonlinear transfer characteristic. It produces a narrow pulse during the time difference between the rising edge of the reference signal and the signal from the frequency divider in the PLL feedback loop. The use of a charge pump naturally adds a pole at the origin in the loop transfer function of the PLL, since the charge pump current is driven into a filter to generate a voltage. This additional pole integrates the error signal causes the system to track the input with one more order. The charge pump consists of pull-up and pull-down transistors, driving a 1 mA charge pump current.

The third order loop filter has been chosen external (see Figure 3). The resistance and capacitance values are computed according to the following equations developed in [8]:

$$T_1 = \frac{\cos^{-1}(\text{PM}) - \tan(\text{PM})}{\text{BW}}, \tag{1}$$

$$T_2 = \frac{1}{\text{BW}^2 * T_1}, \tag{2}$$

$$C_1 = \frac{T_1 * K_{\text{VCO}} * K_\phi * \sqrt{\left(1 + (\text{BW}*T_2)^2\right)/\left(1 + (\text{BW}*T_1)^2\right)}}{T_2 * \text{BW}^2 * N}, \tag{3}$$

$$C_2 = C_1 \frac{T_2}{T_1 - 1}, \tag{4}$$

$$R_2 = \frac{T_2}{C_2}, \tag{5}$$

$$C_3 = \frac{C_1}{2}, \tag{6}$$

$$R_3 = \frac{R_2}{2}, \tag{7}$$

where PM is the phase margin, BW is the open loop bandwidth, K_ϕ is the charge pump current/PFD gain, K_{VCO} is the VCO gain, and N is the rand division.

3. RTW VCO Architecture and Design

The RTW architecture is a reasonable alternative compared to the LC tank classical topology at frequencies above 10 GHz. Most particularly, it provides a more compact design and a lower phase noise at the cost of a higher consumption [9]. The principle of such a VCO is based on a distributed amplifier, with wave amplification over a transmission line (constructive amplification) where the output (2) is connected to the input (1), as shown in Figure 4. In this way, the oscillating frequency is given by

$$f_{\text{osc}} = \frac{\nu_{\text{phase}}}{2NL} = \frac{1}{\sqrt{L_T C_T}}, \tag{8}$$

where ν_{phase} is the phase velocity, $L = l_g = l_d$ the distance of the transmission line between two amplification stages, and

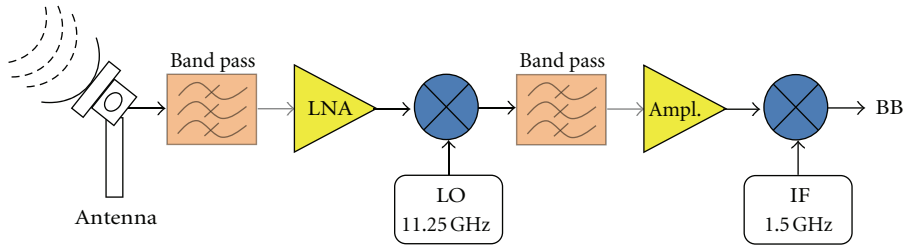


Figure 1: Typical satellite receiver block diagram.

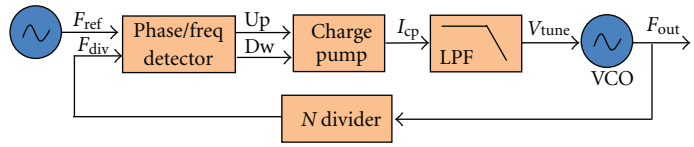


Figure 2: PLL architecture.

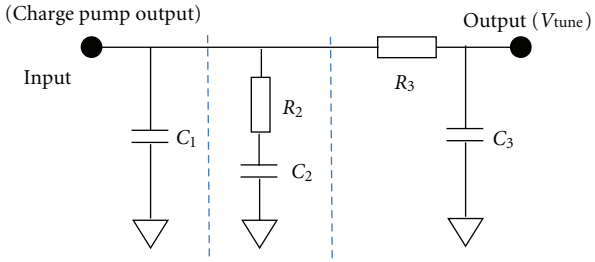


Figure 3: Loop filter schematic.

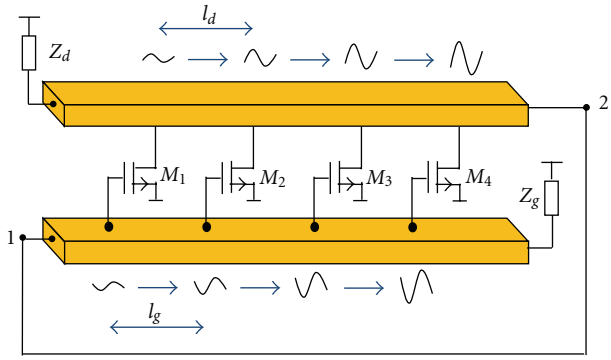


Figure 4: Basic RTW oscillator.

N the number of stages. L_T represents the total inductance of the line, and C_T the capacitance.

In order to avoid the dissipation of half power in terminal Z_g and Z_d, a double crossing line transmission is realized. The corresponding topology is proposed in Figure 10. The amplifiers are realized by CMOS inverters loaded by varactors and switched capacitors in order to reach the desired VCO gain, K_{VCO}. Four amplification stages are used in order to realize a QVCO (Figure 5).

To investigate more in detail the proposed architecture and provide an accurate design method, it is essential to gain a good understanding of the transmission lines theory. As discussed in [9], the oscillating frequency is determined by the odd mode propagation along the line. The characteristic impedance and propagation constant have to be replaced by the ones calculated in differential mode, Z_{0diff} and γ_{diff}, respectively. Neglecting the losses in the metal and dielectric layers, Z_{0diff} can be written as

$$Z_{0diff} = \sqrt{\frac{L_{diff}}{C_{diff}}} = \sqrt{\frac{L-M}{C+2C_f}}, \tag{9}$$

where L_{diff} and C_{diff} are the inductance and capacitance per unit length of the line in differential mode and L, M, C and C_f, are defined as in Figure 6.

In the case of MOS technologies the bottom metal is used to fabricate the ground plane and the top metal or a metal stack is used for the transmission line [10]. This configuration reduces the coupling between lines and ground allowing higher oscillating frequencies, as a consequence. Moreover, as the top metal is usually the thicker one, its use reduces the series resistance providing the advantage of a higher quality factor [11].

In a first approximation, the inductances and capacitances can be computed using Greenhouse [12] and Sakurai and Tamaru [13] formulas. The self- and mutual inductances can be approximated by

$$L = \frac{\mu_0}{2\pi} l\left[\ln\left(\frac{1}{w+t}\right) + 1.193 + \frac{w+t}{3l}\right],$$
$$M = 2l\ln\left(\frac{1}{\mathrm{GMD}} + \sqrt{1+\left(\frac{l}{\mathrm{GMD}}\right)^2}\right) \tag{10}$$
$$-\sqrt{1+\left(\frac{\mathrm{GMD}}{l}\right)^2} + \frac{\mathrm{GMD}}{l},$$

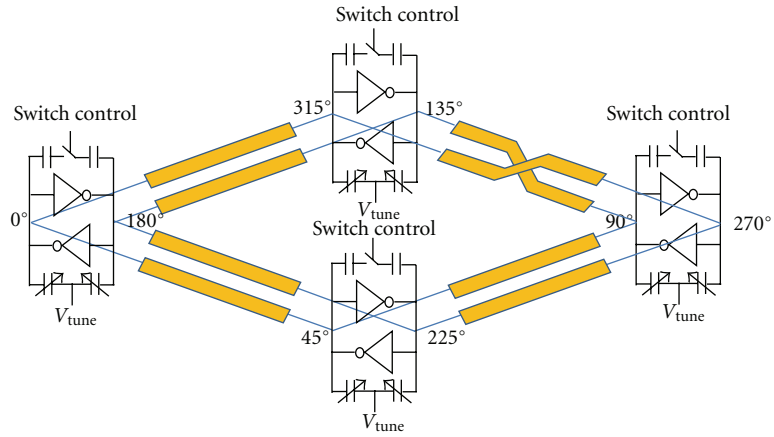


Figure 5: RTW VCO topology.

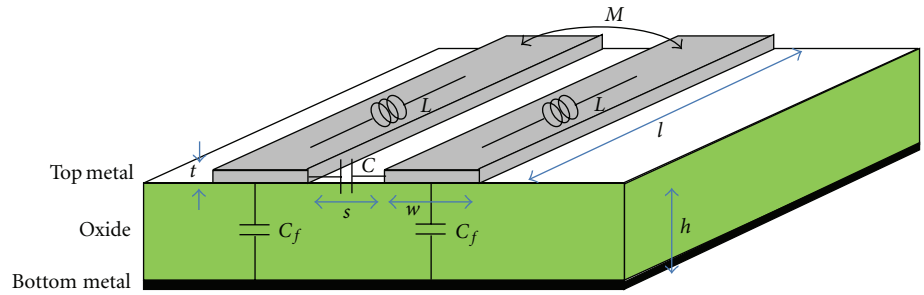


Figure 6: Metal cross-section.

where l, t, and w are the line length, metal thickness, and width, respectively, and GMD is the geometrical mean distance that can be approximated by

$$\mathrm{GMD} = \exp\left[\log(l) - \left[\frac{1}{12}\left(\frac{w}{l}\right)^2 + \frac{1}{60}\left(\frac{w}{l}\right)^4 + \frac{1}{168}\left(\frac{w}{l}\right)^6\right]\right]. \tag{11}$$

The capacitances per unit length are estimated through the following formulas:

$$C = \varepsilon_0\varepsilon_r\left[0.03\left(\frac{w}{h}\right) + 0.83\left(\frac{t}{h}\right) - 0.07\left(\frac{t}{h}\right)^{0.222}\right]\left(\frac{s}{h}\right)^{-1.34},$$

$$C_f = \frac{\varepsilon_0\varepsilon_r}{4} M \sqrt{1 - \left(1 + \frac{2w}{s}\right)^{-2}}, \tag{12}$$

where ε_0, ε_r, s, and h are the vacuum permittivity, the dielectric constant, the spacing between the lines, and the dielectric thickness (see Figure 6), respectively, and M is an elliptic integral of the second kind.

The above equations are guaranteed with an accuracy of about 5 to 10%. If a more accurate calculation is required, one should carry out electromagnetic simulations and then extract an RLGC (or simply LC) compact model compatible with SPICE-like simulators. This entire procedure can become very time consuming.

As the RLC values of the line simultaneously affect the quality factor (Q), which is proportional to the inductance and degraded by the series resistance, and the characteristic impedance, the first step is to choose the line shape that reduces the silicon area and respects symmetry considerations. The second step consists in choosing the spacing, width, and length in order to optimize Q and Z_c.

It has been demonstrated that the characteristics impedance increases as a function of the line spacing and decreases as a function of the width. On the contrary, the quality factor reaches an optimal value for given spacing and width. So, the width has to be optimized to get Q as high as possible; using a 130 nm standard CMOS technology, the optimized width is 5 μm [4]. The drawback is that the characteristic impedance is not very close to the optimal value. This trouble can be fixed by enlarging the spacing to maximize the characteristic impedance almost without impact on Q. As a best trade-off with the line size, we chose a spacing of 14 μm [4].

Finally, the line length was chosen equal to 1500 μm, to get the right amount of total line inductance and capacitance for the desired oscillation frequency.

For simulation purpose, as previously cited, one should extract a RLCG compact model of the line suitable to be adopted in SPICE-like simulator as done by Hsieh et al. [14]. In our case, the line has been optimized to reduce the total space on silicon. The corresponding layout makes it difficult to use theoretical equations accurately.

Practical experience and mismatch between theoretical and simulated scattering parameters clearly suggest the interest of performing electromagnetic simulations (using HFSS) [4].

Once achieved the target oscillation frequency f_{OSC}, varactors, and capacitances can be designed. Moving from the frequency tuning range, the highest allowed K_{VCO}, and the available tuning voltage (1.2 V), the desired frequency tuning range was divided into 500 MHz subbands.

The choice of the switched capacitor value (C_{on}) is carried out according to quality factor Q considerations. For a switch transistor and a capacitor connected in series, Q is equal to $(R_{on}C_{on}\omega)^{-1}$, where R_{on} is the transistor series resistance. C_{on} has therefore to be not too high to have a good quality factor and not too low to limit the effect of the switch parasitic capacitors (C_{off}). In the same way, the switch width has to be chosen to get a good trade-off between R_{on} and parasitic capacitor. In practice, the quality factor of the network should be set to a value higher than the one imposed by the resonator, which is the bottleneck for the quality factor in the RTW oscillator. Eventually, the C_{on}/C_{off} ratio is chosen close to 2. A 100 MHz step between each characteristic leads to 16-switched-capacitor network.

4. Phase Noise Analysis

The phase noise in LC oscillators has been studied for many years [15–17]. However, for the RTW architecture, the theory is slightly different. Legrand de Mercey proposed an approach to compute the phase noise based on the approximation that the output signal is a pure square wave [9]. In our case, the coupled lines act as a band-pass filter and the signal is more sinusoidal. This is mostly the case when the number of inverters becomes low enough and the cut-off frequency of the line decreases.

The theory we propose here is a generalization of Mercey's work to any shape of output signal and is based on the computation of the impulse sensitivity function (ISF) introduced by Hajimiri and Lee as a general theory of phase noise in electrical oscillators [15]. In this kind of approach to the phase noise analysis, the ISF has to be exactly known and thus a transient simulation has to be run prior to the phase noise computation. The ISF, in the following indicated as Γ, describes the phase deviation in the periodic signal due to a current impulse $i_n(t)$. The phase deviation is maximum (minimum) if $i_n(t)$ occurs close to the zero-crossing (peak) instant of the periodic signal. The phase shift φ_{out} due to $i_n(t)$ is described by the following formula:

$$\varphi_{out}(t) = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(2\pi f_0 \tau) \cdot i_n(\tau) d\tau, \tag{13}$$

with q_{max} being the maximal charge stocked by the oscillator. The corresponding phase noise is

$$L(\Delta f) = 10 \log\left(\frac{\Gamma_{RMS}^2 \overline{i_{nw}^2(\Delta f)}}{2q_{max}^2 (2\pi \Delta f)^2} \right), \tag{14}$$

where Δf is the frequency offset, Γ_{RMS} is the root-mean-squared value of the ISF function and i_{nw} is the power spectral density of the current impulses assumed to be white noise current.

Assuming the oscillator as a second order system, the ISF is

$$\Gamma = \frac{g'}{g'^2 + g''^2}, \tag{15}$$

where g' and g'' are the first and second derivatives of the normalized waveform of the signal generated by the oscillator.

Moving from these equations, White and Hajimiri [18] proposed to recompute the characteristic impedance including also the discrete capacitances contributed by the varactors and the switched capacitors. It is here worth noticing that this is valid as long as the distributed condition is respected (e.g., for high number of inverters).

The total capacitance C_T is then given by

$$C_T = C_{diff} + C_{active}, \tag{16}$$

where C_{diff} is the line capacitance in differential mode and C_{active} is the sum of the input and output capacitances of the inverters.

This value of C_T, once inserted into (9) in the place of C_{diff}, leads to a new expression of the adjusted characteristic impedance (Z_{0T}).

In order to compute the total phase noise of the RTW oscillator, q_{max} is expressed as a function of the output signal amplitude (A) and C_T:

$$q_{max} = AC_T. \tag{17}$$

The obtained phase noise expression is given by

$$L(\Delta f) = 10 \log\left(\frac{\Gamma_{RMS}^2 Z_{0T}^2 f_0^2 \overline{i_n^2(\Delta f)}}{2q_{max}^2 (2\pi \Delta f)^2} \right). \tag{18}$$

Finally, the evaluation of the phase noise requires to know the noise spectral density of the noise sources introduced by the active devices while the thermal noise contribution of the line can be calculated using

$$\overline{i_{line}^2(\Delta f)} = \frac{4kT}{\mathrm{Re}(Z_{0T})}. \tag{19}$$

Concerning the contribution of active devices, assuming all the transistors exhibit the same transconductance (g_m), the noise contribution of each transistor is provided by the following expression:

$$\overline{i_{transistor}^2(\Delta f)} = 4kT\gamma g_m. \tag{20}$$

So, the total contribution from the N inverters is given by

$$\overline{i_{active}^2(\Delta f)} = 2N \overline{i_{transistor}^2(\Delta f)}. \tag{21}$$

Adding (19) and (21) one obtains the total white noise power spectral density:

$$\overline{i_{nw}^2(\Delta f)} = 4kT\left(N\gamma g_m + \frac{1}{Z_{0T}} \right). \tag{22}$$

The substitution of this expression into (18) leads to the following expression of the phase noise:

$$L(\Delta f) = 10\log\left(\frac{\Gamma_{\mathrm{RMS}}^2 Z_{0T} f_0^2 4kT(1 + N\gamma g_m Z_{0T})}{2q_{\max}^2 (2\pi\Delta f)^2}\right). \quad (23)$$

In practice, it is worth noticing that a first transient simulation is required to determine the signal amplitude and the RMS value of the impulse sensitivity function while all the other parameters are known prior to the design. We can notice that this formula (23) does not take into account the flicker noise, which is due to the nonlinear capacitors of the circuit. The frequency transition between $1/f^3$ and $1/f^2$ (the flicker knee is mainly fixed by the capacity of the transmission line) is made having relatively low frequency offset below 100 kHz. In fact, the nonlinear capacitors in the circuit are mainly varactors and parasitic capacitors of the transistors (inverters). During the design of the circuit, we have try to reduce at most the varactors (and thus the nonlinear capacitors), for another reason than the flicker noise, to reduce the K_{VCO} with the switched capacitors. By having lowering the flicker noise knee, and by considering the high-pass filtering of the PLL on the VCO noise, the integrated phase noise can be considered as independent from the flicker noise in our case.

In (23), the Γ_{RMS} decreases with the number of invertersis as shown previously, while the term $N \cdot g_m$ represents the total required transconductance and is constant whatever the number of invertersis. As a consequence, the total phase noise will decrease when N increases. This is verified in Figure 7(a) where the ISF function of the output signal for VCOs with 2, 4, 8, or 16 inverters pairs is shown. The corresponding phase noise simulations are given in Figure 7(b).

We can observe that when N increases from 8 to 16 the phase noise variation is lower than expected, which is due to the inverters slew rate that prevents the output signal from being a square wave, so that the Γ_{RMS} tends to reach a minimal value.

5. Implementation and Measured Results

A RTW VCO has been designed and fabricated in a bulk 130 nm CMOS technology using the previously described phase noise modeling and line optimization as a design guideline. The microphotography of the prototype is shown in Figure 8 where V_{tune} is the varactor tuning voltage and V_{comp} is injected in an analog to digital converter to generate the switch word SW. This latter can be checked thank to the SW test outputs. The total size is $300 \times 300\,\mu\mathrm{m}^2$. With all the switches set on, that is, with the digital word controlling the switched capacitor network set to "0000", the RTW VCO exhibited a $f_{\mathrm{OSC}} = 11.24$ GHz and delivered about -30.7 dBm (see Figure 9) to a load of 50 Ω by drawing 25 mA from a 1.2V bias.

The phase noise measurements were carried out with an Agilent E5500 phase noise meter. Under the same switch configuration as before, the measured phase noise is shown in Figure 10. At 1 MHz frequency offset of the central frequency $f_{\mathrm{OSC}} = 11.24$ GHz, the measured phase noise is -105 dBm/Hz instead of the -107 dBm/Hz value from the simulation (-109 dBm/Hz value computed from the theory developed in Section 4). Because of the intrinsic hard nature of both the nonlinear phenomena involved in the generation of the phase noise and of the experimental difficulties affecting the phase noise measurement, it is the authors' opinion that the measured value has to be considered in well agreement with the numerical simulation and especially with the analytical computation. It is worth pointing out that the achieved phase noise value sounds very promising when compared with the phase noise specifications required by satellite applications for the low noise block oscillator. On the basis of the electromagnetic simulations carried out in the present work, it is the authors' opinion that the lacking 10 dB, or at least a large fraction of them, can be achieved by making thicker the top metal layer used to design the line. In particular, it can be estimated that a thickness of $4\,\mu$m would be enough to completely fulfill the phase noise specifications of -115 dBc/Hz at 1 MHz offset from the carrier, leading to a 1.2° RMS integrated phase noise which has been commonly admitted by the design community as a reasonable specification.

Figure 11 depicts the experimental dependence of the output frequency on the tuning voltage measured for all the possible configuration of the switched capacitor network. The lowest (highest) frequency band is obtained by setting the digital word controlling the switched capacitor network equal to "1111" ("0000"). The total frequency coverage is 1.2 GHz divided into 16 parts and the maximal value for the K_{VCO} is 400 MHz/V.

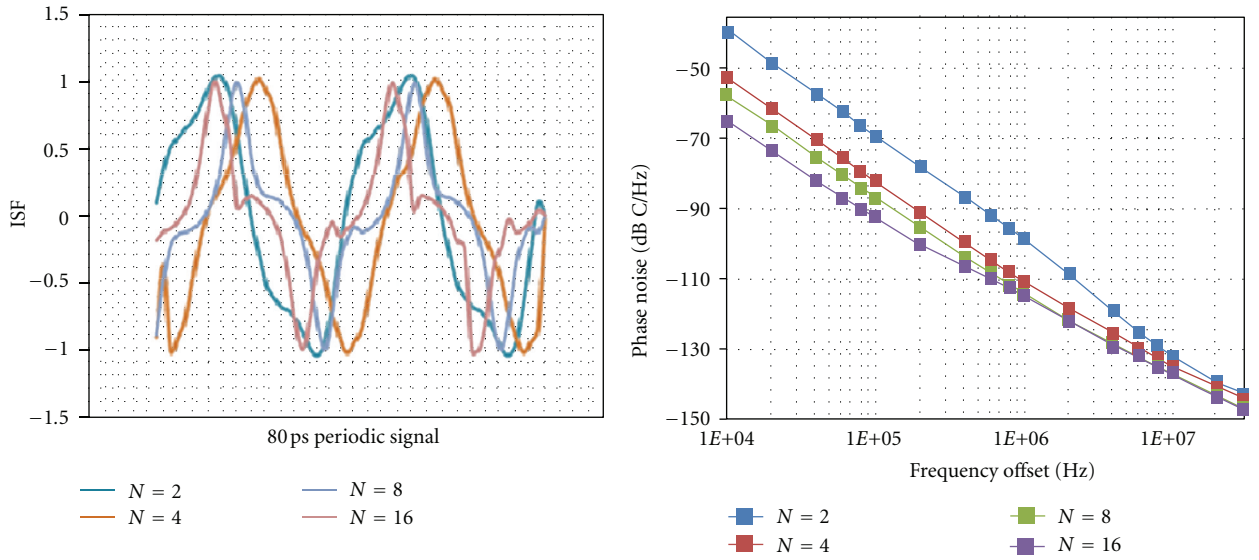
Figure 12 compares through the following Figure Of Merit (FOM) the RTW-VCO reported in the present paper with the state-of-the-art of distributed oscillators [9, 14, 19–23]:

$$\mathrm{FOM} = 10 \cdot \log\left(\left(\frac{f_{\mathrm{osc}}}{f_m}\right)^2 \frac{f_{\mathrm{osc}}}{L(\Delta f) \cdot P_{\mathrm{DC}}}\right) + 10\log(T_{\%}). \quad (24)$$

In the frequency range of interest, the oscillator reported in the present paper well compares with the performances claimed by other authors in the literature. In particular, it is worth pointing out that the FOM achieved in the present paper with a VCO fabricated in $0.13\,\mu$m CMOS technology is fairly close to the FOM achieved by a VCO fabricated in the more expensive 65 nm technology. In addition, in Figure 12, it is also reported an estimation of the FOM achievable if a top metal layer of $4\,\mu$m (RF CMOS process) was used. Measured characteristics of the RTW VCO are listed in Table 2.

6. PLL Implementation

Since the VCO is used in a PLL, the previous measured phase noise spectrum depicted has been adopted in a PLL linear Matlab model [24]. The cut-off frequency of the loop filter has been designed having in mind the minimization of the PLL integrated phase noise. Figure 13 plots the integrated



(a) ISF function

(b) Simulated phase noise

Figure 7: ISF functions and phase noise for $N = 2, 4, 8$, or 16 amplifiers.

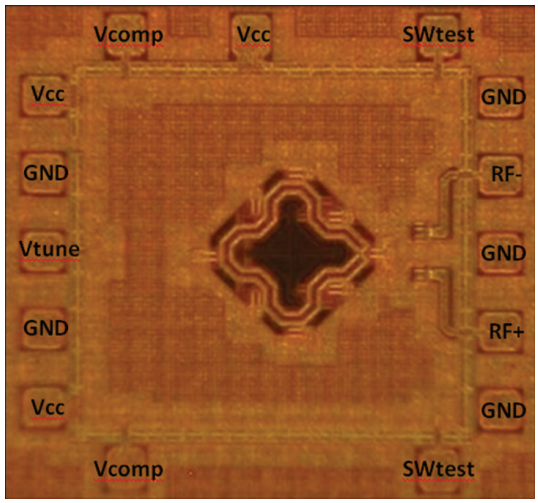


Figure 8: RTW VCO microphotography.

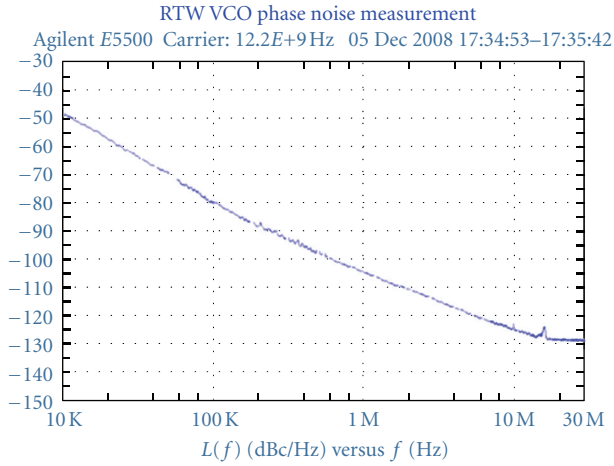


Figure 10: RTW VCO phase noise measurement.

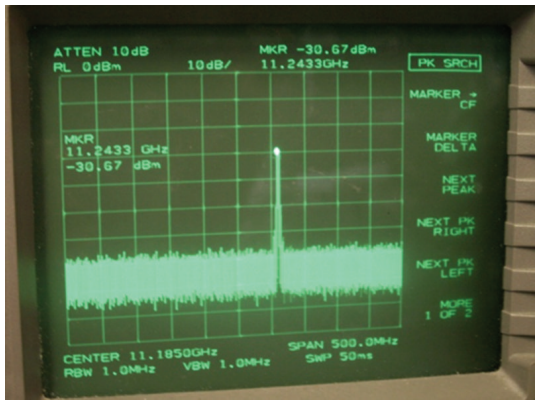


Figure 9: Frequency measurement.

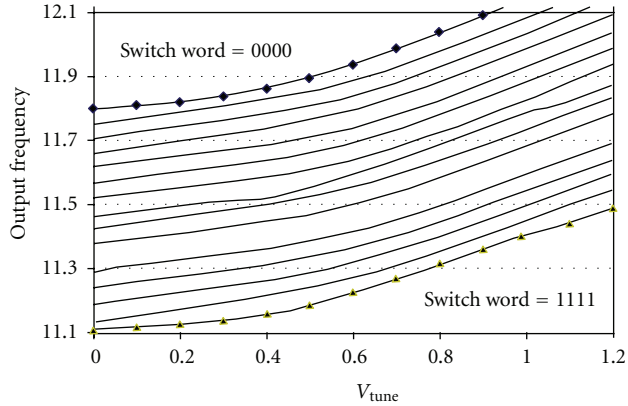


Figure 11: Output frequency versus V_{tune}.

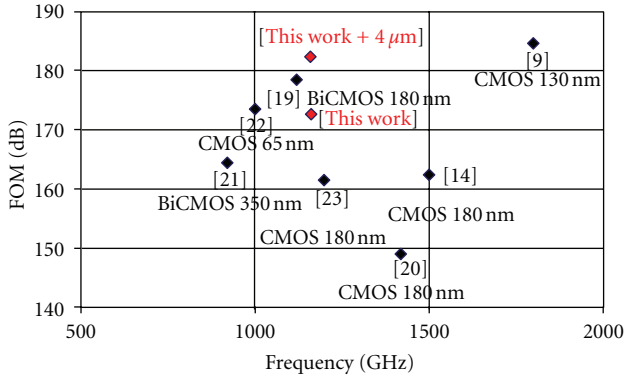


Figure 12: RTW VCO FOM comparison.

Table 2: Measured VCO characteristics comparison.

Central frequency	11.25 GHz
K_{VCO}	400 MHz
Tuning range	1200 MHz
Power consumption	30 mW
Size	0.105 mm^2
PN at 1 MHz	−105 dBc/Hz
FOM	174 dB

Table 3: Simulated PLL characteristics.

Central frequency	11.5 GHz
Power consumption	39 mW
Bandwidth	550 kHz
Size	0.105 mm^2
PN at 1 MHz	−102 dBc/Hz
Settling time	11 μs

phase error versus the open loop bandwidth as computed by the linear model.

The minimum phase error is 1.6° RMS with a 550 kHz optimal bandwidth. From the cut-off frequency of the loop filter, the R and C values of the loop filter were calculated: $C_1 = 15$ pF, $C_2 = 1.9$ nF, $C_3 = 7.5$ pF, $R_2 = 1.7$ kΩ, $R_3 = 1.5$ kΩ. In addition to the previously cited Matlab model, the PLL design has been also addressed through SPICE simulations to gain more details about the noise contribution of each block (PFD/CP, prescaler, divider, and reference), as depicted in Figure 14, and an estimation of the PLL settling time from transient simulation (cf. Figure 15).

The performances of the designed PLL are summarized in Table 3. The phase noise specifications at a 1 MHz offset are not met. Different solutions can be used to solve this problem. For the RTW structure, we can use a thicker and higher quality metal to realize the transmission line [4], further increase the discrete capacitive steps to lower the sensibility (i.e., K_{VCO}), and use an internal regulator to provide a supply that is very clean; the K_{VCO} versus supply is actually one of the biggest problem of this structure.

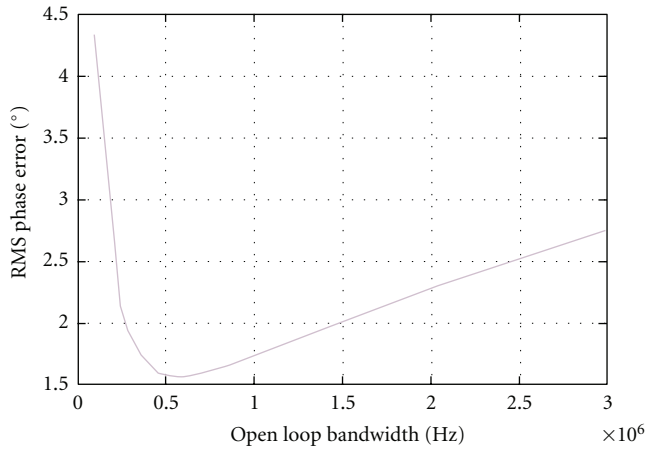


Figure 13: Integrated RMS phase error.

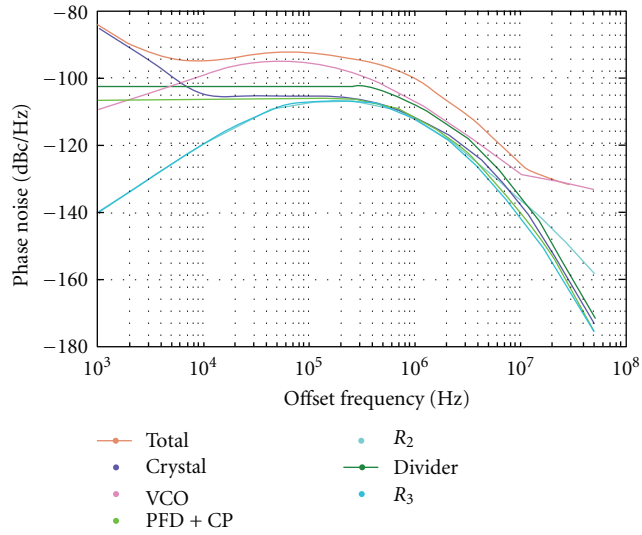


Figure 14: Simulated RTW VCO PLL phase noise.

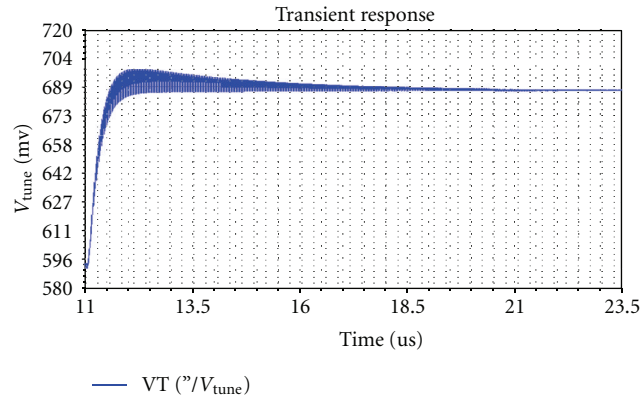


Figure 15: Simulated settling time.

7. Conclusion

In the present paper a RTW VCO designed in a 130 nm CMOS technology has been reported. The VCO was designed featuring two tune modes: a broadband tune mode obtained through switched capacitors and a fine tune mode realized with traditional varactors. This approach allows reducing the VCO gain VCO with improvements for the phase noise and the stability of the PLL. The VCO design was optimized through the use of a phase noise modelling and a line optimization procedure presented in the paper.

In particular the phase noise model was based on the use of the impulse sensitivity function (ISF) which is based on a linear-time-varying (LTV) model of the oscillator. The theory developed in Section 4 estimates a phase noise of −109 dBc/Hz at an offset frequency of 1 MHz, a value that fairly well compares with the measured value of −105 dBc/Hz as well as the simulated value of −107 dBc/Hz. In spite of this fairly well agreement between the proposed analytical model, simulations, and measurements, it is mandatory to pointing out that the theory provides an analytical expression of the phase noise (see (18)) where the impact of the quality factor (Q) on the phase noise is not clear, even if one can attend, as a rule of thumb, that the phase noise decreases with increasing Q. This limitation stems from the fact that an ISF description of the phase noise is based on a linear-time-varying (LTV) model where the computation of the quality factor remains in some way obscure, because of the lack of a unified getting [25–27]. In this perspective, under a conceptual point of view physically based approaches perform better. In [28] the authors report on a physically based theory of the phase noise in a rotary travelling wave oscillator. The theory leads to a fairly well agreement with the measurements for an offset frequency of 1 MHz, as in the case of the present paper. Again, the physically based theory proposed in [28] makes provision for a decrease of the phase noise in the $1/f$ frequency range with increasing the number of amplifiers constituting the oscillator as the ISF theory proposed in the present paper (see Figure 7(b)). Moving closer to the carrier, differences appear between the two approaches. At an offset frequency of 10 kHz the physically based theory fails to predict the phase noise for more than 10 dB while the ISF based model proposed in the present paper matches the experimental value within a 10 dB of tolerance. The authors in [25] state indeed that a physically based modelling of the flicker-noise up-conversion in the rotary travelling wave oscillator is still an open area of investigation. In short, even if the phase noise modelling proposed in the present paper suffers from limited insights into the physical mechanisms responsible for the phase noise, on the other hand, it actually exhibits a prediction capability of the phase noise on a larger offset frequency range.

When compared with other distributed oscillators reported in the literature, the RTW VCO reported in the present work exhibits a figure of merit close to that recently reported for a 65 nm CMOS distributed VCO. On the basis of the experience carried out during this work, the authors believe that the achieved phase noise can be reduced down to −115 dBc/Hz at 1 MHz by using a technology offering a thicker top metal layer.

The obtained results suggest not only that a RTW VCO designed using a CMSO technology can replace the DRO as a local oscillator, with a reduction in size and costs of the satellite receiver, as a consequence, but that it can be also usefully applied for the design of Ku-band satellite receiver with an image frequency rejection or direct conversion architecture, offering the advantage of eliminating the troubles related to the design of the image frequency rejection filters.

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