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Research Article

Gate Stack Engineering and Thermal Treatment on Electrical and Interfacial Properties of Ti/Pt/HfO_2/InAs *p*MOS Capacitors

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Effects of gate stack engineering and thermal treatment on electrical and interfacial properties of Ti/Pt/HfO_2/InAs metal insulator semiconductor (MIS) capacitors were systematically evaluated in terms of transmission electron microscopy, energy dispersive X-ray spectroscopy, current-voltage, and capacitance-voltage characterizations. A 10 nm thick Pt metal effectively suppresses the formation of interfacial oxide, TiO_2, between the Ti gate and HfO_2 gate dielectric layer, enhancing the gate modulation on the surface potential of InAs. An *in situ* HfO_2 deposition onto the *n*-InAs channel with an interfacial layer (IL) of one-monolayer InP followed by a 300°C post-metal-anneal produces a high-quality HfO_2/InAs interface and thus unravels the annoying Fermi-level pinning, which is evidenced by the distinct capacitance dips in the high-/low-frequency *C-V* characteristics. The interface trap states could be further suppressed by replacing the InP IL by an As-rich InAs, which is substantiated by a gate leakage reduction and a steep voltage-dependent depletion capacitance.

1. Introduction

Motivation to study low band-gap InAs and InSb channels for next-generation metal oxide semiconductor (MOS) transistors is strong in light of their superior carrier mobility [1] and established epitaxy techniques [2, 3] among other emerging technologies such as carbon nanotube and graphite. However, the progress of realizing high-performance InAs and InSb MOS transistors has been impeded by the stringent restraint on thermal budget as well as the lack of robust gate dielectrics and suitable surface treatments for unraveling annoying Fermi-level pinning [4] at the oxide/semiconductor interface. Recently encouraging experimental demonstrations of high-*K* gate dielectrics (Gd_2O_3, Al_2O_3, and HfO_2) on GaAs [5–7], InP [8], and InAs [9–11] channels using atomic-layer deposition (ALD) techniques have shed lights and attracted tremendous attentions on this venerable subject. In spite that various chemical and plasma surface treatments [12–14] have been proposed for annihilating surface states of III-V compound semiconductors, it still remains elusive how to produce a clean and well-passivated channel surface for subsequent high-quality gate dielectric growth. The most practical and promising approach for the surface preparation of III-V channels appears to be the *in situ* growth of gate dielectrics on channels.

In this paper, the authors report the interfacial and electrical properties of Ti/Pt/HfO_2/InAs *p*MOS capacitors, in which a high-*K* gate dielectric, HfO_2 was grown on an *n*-InAs epitaxial layer without breaking vacuum by means of the integration of a molecular beam epitaxy system (Riber-32 MBE) with an atomic layer deposition system (Picoson R-100 ALD). In order to prevent thermal evaporation of InAs, all the device fabrication processes were kept below 300°C. Both Ti and Pt metals were evaluated for the gate materials. The interfacial layer effect arising from one-monolayer InP or As-rich InAs between HfO_2 and InAs channel, the deposition conditions of HfO_2, and post-metal-anneal (PMA) processes were systematically studied for improving the interfacial and electrical properties of HfO_2/InAs *p*MOS capacitors.

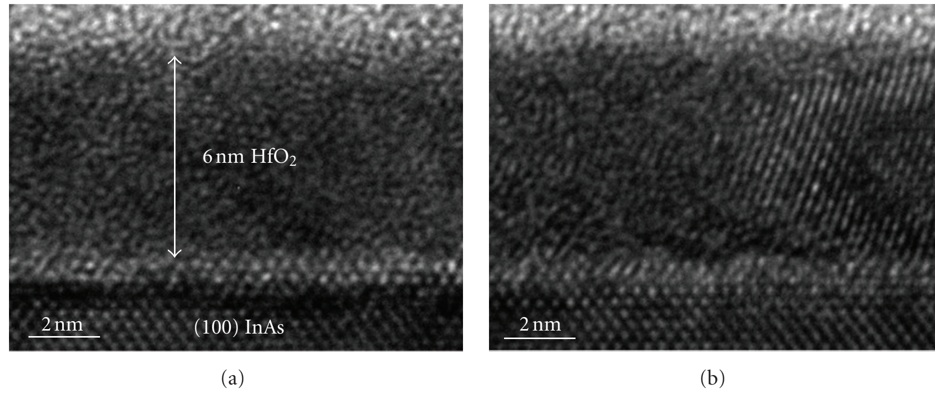

Figure 1: CTEM images of HfO_2 *in situ* deposited on InP/InAs channel at (a) 200°C and (b) 300°C. Abrupt and native oxide free interface provides a promising interface for MOS applications.

Element	Atomic (%)
O(K)	23.8
In(L)	1.7
Ti(K)	74.5
Hf(L)	0
As(K)	0

Element	Atomic (%)
O(K)	43.4
In(L)	4.8
Ti(K)	2.7
Hf(L)	43.6
As(K)	5.5

Element	Atomic (%)
O(K)	54.3
In(L)	0.4
Ti(K)	45.2
Hf(L)	0.1
As(K)	0

Figure 2: Energy dispersive X-ray spectroscopy (EDX) analysis obtained from various locations of Ti/InP/InAs MOS structure. EDX analysis reveals that an interfacial TiO_x ($x \sim 1.2$) and Hf-rich oxide were formed after Ti deposition onto HfO_2/InP/InAs structure.

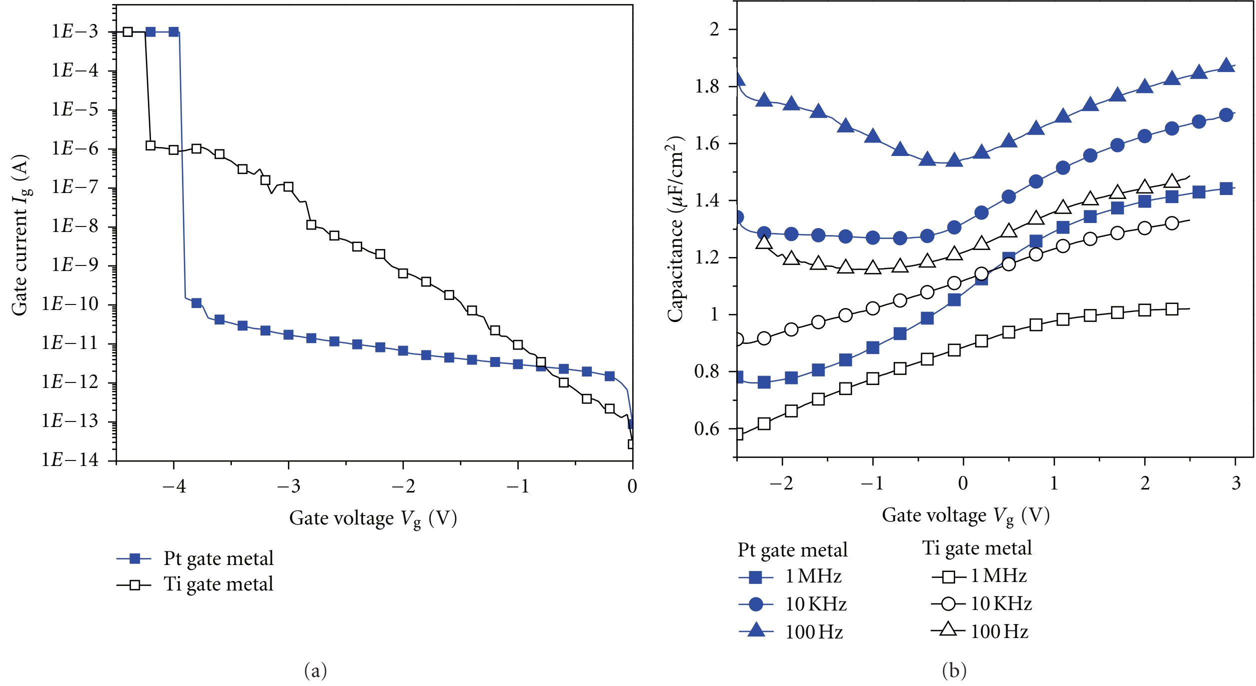

FIGURE 3: (a) I-V and (b) C-V characteristics of HfO_2/InP/InAs MOS capacitors of $100 \times 100\,\mu m^2$ with Ti and Pt gate metal, respectively.

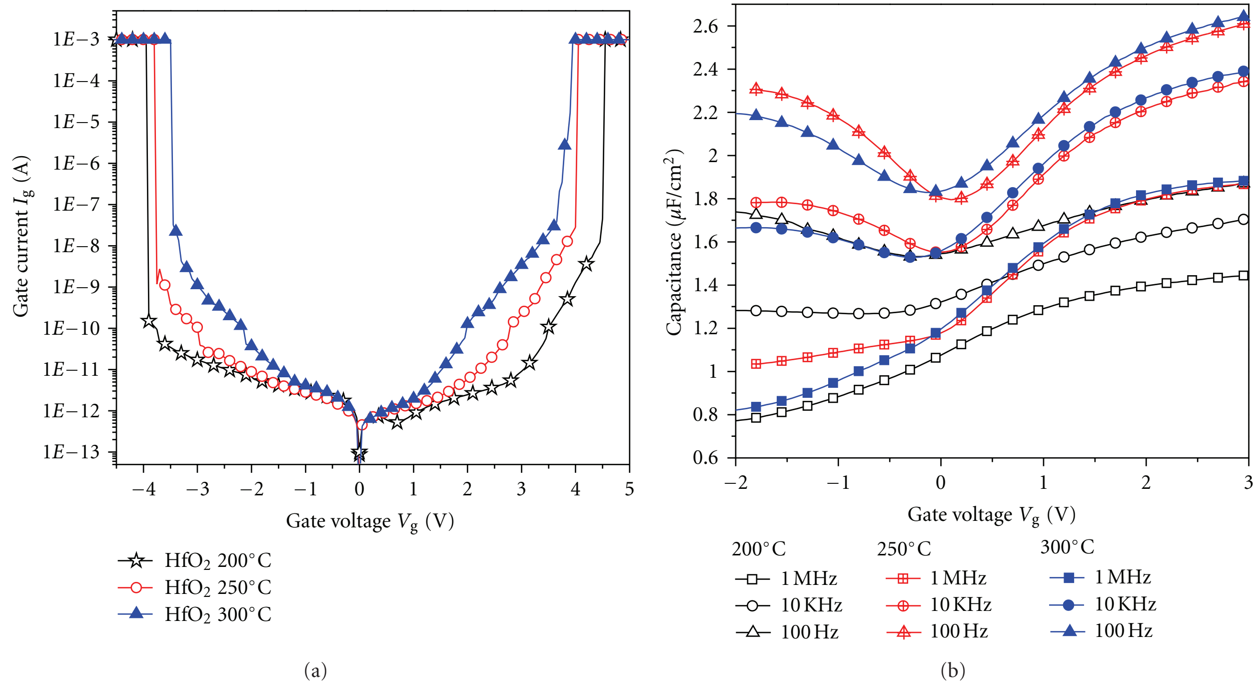

FIGURE 4: (a) I-V and (b) frequency-dependent C-V characteristics of Pt/HfO_2/InP/InAs MOS capacitors in which HfO_2 was deposited at 200, 250, and 300°C, respectively.

2. Experimental

The fabrication of HfO_2/InAs MOS capacitors started with a 2″ (100) n-InAs substrate doped with Si [(2–5) $\times$ $10^{17}\,cm^{-3}$], followed by an epitaxial growth of a 200 nm thick n-InAs channel layer uniformly doped with Si in a concentration of 2 $\times$ $10^{17}\,cm^{-3}$ and an one-monolayer InP or As-rich InAs IL on the top of InAs channel. After transferring the sample from the MBE growth chamber to ALD system through a high-vacuum

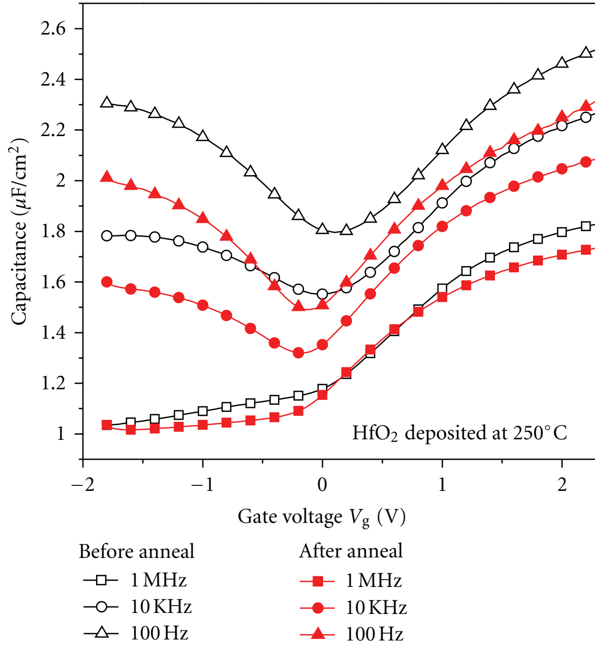

FIGURE 5: Frequency-dependent C-V characteristics of Pt/HfO_2/InP/InAs MOS capacitors in which HfO_2 was deposited at 250°C before and after a subsequent 300°C forming gas PMA.

chamber with a base pressure of 6×10^{-8} Torr, a 6 nm thick HfO_2 layer was deposited at 200-300°C using water vapor and tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf[N(C_2H_5)(CH_3)]_4$] precursors. A 300 nm thick Ti or a 50 nm thick Pt was evaporated as gate materials followed by the gate definition either using photolithography and HF/H_2O_2 chemical etching or through a shadow mask. Finally, the fabrication of MOS capacitors was completed by the evaporation of a 100 nm thick Al onto the substrate as the back-gate electrode and a 300°C PMA for 30 min. The interfacial and structural properties of the Ti/Pt/HfO_2/InAs system were examined using high-resolution transmission electron microscopy (HRTEM) and energy dispersive X-ray spectroscopy (EDX). The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the HfO_2/InAs MOS capacitors were characterized using Keithley-4200 and HP4284 semiconductor analyzers.

3. Results and Discussion

Figure 1 shows the cross-sectional TEM (CTEM) images of the gate stack of Ti/HfO_2/InP/InAs structure. The *in situ* growth of HfO_2 on an InP/InAs channel produces a native-oxide free and abrupt HfO_2/InP/InAs interface, indicating dangling bonds or surface states of InP/InAs are suppressed and providing a good interface for charge inversion under gate modulation. Additionally, there appears to be a 10–12 nm thick interfacial layer between a 6 nm thick HfO_2 layer and Ti-gate, and EDX analysis reveals that the chemical composition of the interfacial layer is TiO_x ($x \sim 1.2$) and the underlay hafnium oxide becomes a Hf-rich oxide (Figure 2), suggesting Ti catalytically releases oxygen from the stoichiometric HfO_2, forming a Hf-rich oxide, and the subsequent reaction of Ti and released oxygen generates TiO_x. The undesired interfacial TiO_x and Hf-rich oxide layers not only deteriorate the oxide integrity but also thicken the gate dielectrics thickness, which are evidenced by a high-gate leakage, a poor gate modulation on the surface potential of InAs channel but a slightly higher breakdown voltage as illustrated in the I-V and C-V characteristics (Figure 3).

An interesting finding that we have made through TEM observation is that a thin Pt barrier metal before Ti deposition effectively suppresses the formation of an interfacial oxide layer and retains the stoichiometry and high quality of HfO_2. The dielectric thickness of the Pt-gated MIS capacitor is 6 nm thick HfO_2, whereas the Ti-gated MIS capacitors have a gate oxide of 16–18 nm (10–12 nm TiO_x and 6 nm Hf-rich oxide). Although the thinner gate dielectric in the Pt-gated MIS capacitors sustains a smaller breakdown voltage than Ti-gated devices do, the reduction of gate leakage is more than 4 orders in magnitude as compared with the Ti-gated MIS capacitors. As a consequence, there appear a significant increase in the accumulation capacitance for a Pt-gated MIS diode and an enhanced gate modulation from C-V characteristics in Figure 3(b).

The gate-oxide integrity appears to be strongly dependent on the HfO_2 deposition temperature and the thermal treatment after metal patterning. Increasing the deposition temperature from 200 to 250°C not only enhances the accumulation capacitance because of an increase in the dielectric constant of HfO_2 from 11 to 15, but also improves the inversion capacitance as a consequence of a better HfO_2/InP/InAs interface. This is evidenced by a steep C-V transition in the depletion regime and a distinct capacitance dip when gate voltage modulates the surface potential of the InAs channel from depletion to inversion regimes (Figure 4). However, a higher HfO_2 deposition temperature at 300°C degrades the gate leakage and breakdown E-field accordingly, possibly originating from the crystallinity of HfO_2 transitioning from amorphous to polycrystalline phases from 200 to 300°C (Figure 1(b)). An additional 300°C PMA in H_2/N_2 ambient for 30 min further appears to reduce the dangling-bonds and annihilates the surface states at the HfO_2/InP/InAs interface, but also improves the frequency-dependence of the accumulation capacitance as a result of the dielectric constant dispersion (Figure 5). The above mentioned experimental results also suggests that the InAs epitaxial layer is of high quality and does not degrade after a long duration (45 min) of 300°C ALD and PMA process.

The interfacial properties and electrical characteristics of InAs MOS capacitors could be further improved by replacing the unrelaxed InP IL with a latticed match As-rich InAs IL, in spite that the bandgap of InAs (0.345 eV) is smaller than InP (1.344 eV). This is evidenced by a reduction of the gate leakage by one order in magnitude as shown in Figure 6(a). This is also substantiated by a steeper slope in the depletion region of the C-V characteristics in Figure 6(b). Suppressed surface states by As-rich IL and a high-thermal generation rate in narrow band-gap InAs [15] make the C-V curves

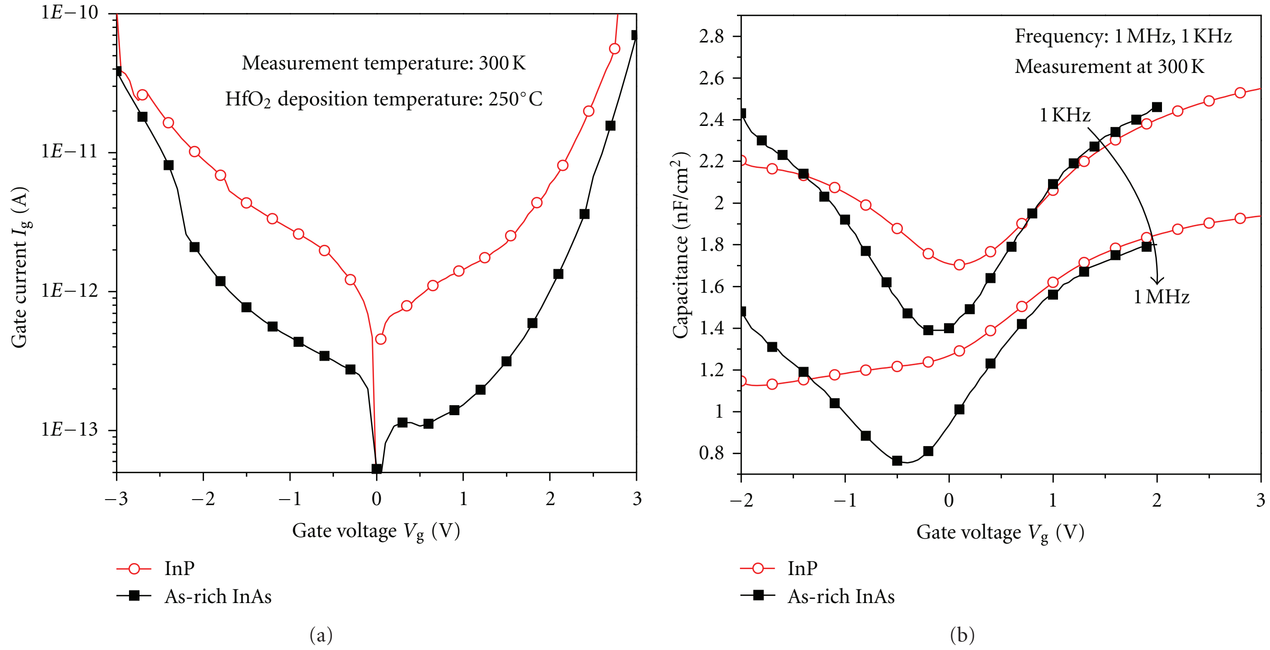

Figure 6: (a) I-V and (b) C-V characteristics of Pt/HfO_2/InAs MOS capacitors with respective InP or As-rich InAs interfacial layers.

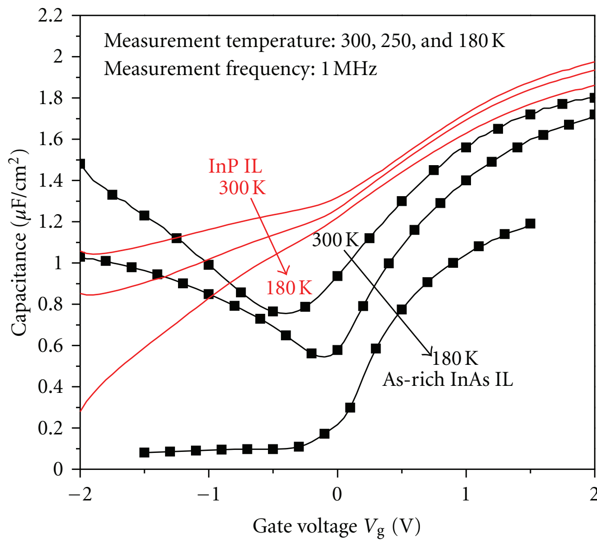

Figure 7: 1 MHz temperature-dependent C-V characteristics of InAs MOS capacitor with respective InP or As-rich interfacial layers.

measured at 1 MHz deviate from the conventional high-frequency C-V characteristics, in particular, at the inversion regime (Figure 7). For example, the inversion capacitances at 300 and 250 K are voltage dependent and getting close to the value of the gate oxide capacitance, instead of the effective capacitance of gate oxide capacitance in series with the depletion capacitance. Decreasing measurement temperature from 300 to 180 K decreases the thermal-generated carrier population and makes the inversion capacitance value restoring back to the one of typical high-frequency C-V characteristics. The extracted interface trap density (D_{it}) using a conductance method from the Pt/HfO_2/InAs MOS capacitors with InP and As-rich interfacial layer is 1.59×10^{13} and 7×10^{12} cm^{-2} eV^{-1}, respectively, which are comparable with reported data [9–11].

4. Conclusion

The *in situ* growth of HfO_2 on InAs channel produces an abrupt and oxide-free interface, which is an important prerequisite for high-performance InAs MOS devices. The interfacial and electrical properties of HfO_2/InAs MOS capacitors are strongly influenced by the gate metal, HfO_2 deposition temperature, the post-metal anneal, and interfacial control layer between HfO_2 and InAs channel. A Pt barrier metal effectively suppresses the formation of interfacial TiO_x oxide and thus significantly improves the gate leakage and insulating quality of the gate stack. The gate oxide integrity and the gate dielectric constant of HfO_2 could be further improved by a 250°C ALD deposition and a 300°C PMA treatment. An As-rich InAs IL further suppress surface states, evidenced by the reduction of gate leakage, and depletion/inversion capacitances.

Acknowledgments

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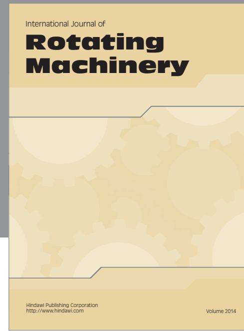
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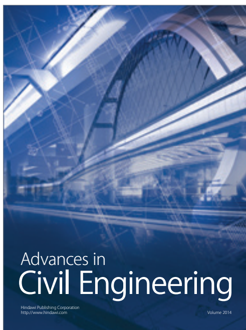
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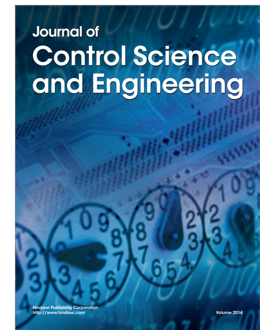
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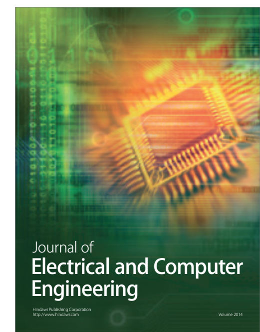
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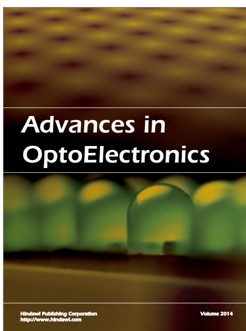
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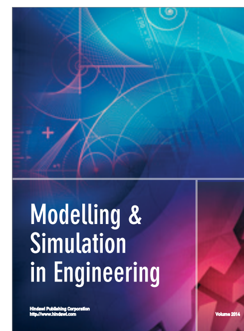
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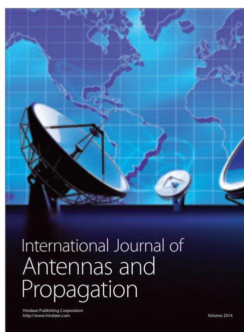
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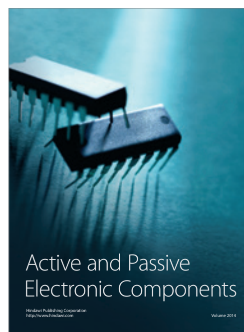
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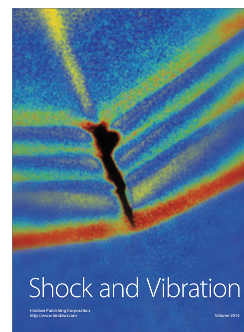
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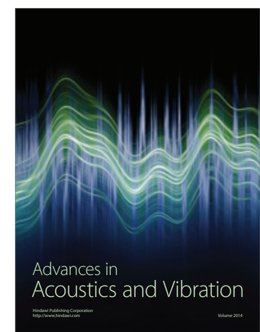
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