

Research Article

The Improvement of Reliability of High-k/Metal Gate pMOSFET Device with Various PMA Conditions

Yi-Lin Yang,¹ Wenqi Zhang,² Chi-Yun Cheng,² and Wen-kuan Yeh²

¹ Department of Electronic Engineering, National Kaohsiung Normal University,
Kaohsiung 824, Taiwan

² Department of Electrical Engineering, National University of Kaohsiung,
Kaohsiung 824, Taiwan

Correspondence should be addressed to Yi-Lin Yang, t3550@ncku.edu.tw

Received 9 March 2012; Revised 23 April 2012; Accepted 26 April 2012

Academic Editor: Kuan-Wei Lee

Copyright © 2012 Yi-Lin Yang et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

The oxygen and nitrogen were shown to diffuse through the TiN layer in the high-k/metal gate devices during PMA. Both the oxygen and nitrogen annealing will reduce the gate leakage current without increasing oxide thickness. The threshold voltages of the devices changed with various PMA conditions. The reliability of the devices, especially for the oxygen annealed devices, was improved after PMA treatments.

1. Introduction

High-k/metal gates are needed to continuous device scaling-down. However, threshold voltage instability and performance degradation are important problems for high-k devices [1]. The defect density in the interface of gate stack is the major cause for negative bias temperature instability (NBTI) as well as mobility degradation [1]. Oxygen vacancy is known to play an important role in threshold voltage variations [2] and is a significant defect in the HfO₂/Si system [3]. The influence of charge oxygen vacancies introduces a dipole offset between the gate metal and the substrate [4].

Post metallization annealing (PMA) is used to reduce the defects at the interface, such as fixed oxide charges, oxide trapped charges, and interface charges [5]. Previous work has demonstrated that oxygen vacancies can be passivated for device with noble metal gate by oxygen diffusion through the gate metal [6]. However, these suffer from high equivalent oxide thickness. In this work, we show that both oxygen and nitrogen can be diffused through thin TiN layer and passivate the oxygen vacancies without increasing the oxide thickness by using PMA with various temperatures. Negative bias instability for pFET is improved, especially for the oxygen annealed one.

2. Experimental

28 nm FET high-k/metal gate was formed on bulk Si. After interfacial SiO₂ layer/high-k and TiN deposition, TiN layer was then deposited with the thickness of 100~200 Å. The fabrication process of the high-k metal gate last device was sketched in Figure 1. Some of the samples were annealed at 400°C and 450°C in oxygen or nitrogen ambient for several minutes, respectively.

The capacitance-voltage (*C-V*) curves were measured with an HP4280 precision LCR meter and the current-voltage (*I-V*) curves with an HP-4156B. After the basic electric measurements, the samples were then stressed by using a constant voltage of $V_{\text{stress}} = V_t - 1$. After stressing, the samples were measured again to find out the performance of reliability.

3. Results and Discussions

Figure 2 shows the *C-V* curves of the samples measured with 1 MHz. The extracted EOT for all samples is about 13 Å. The merged *C-V* curves at low voltage for all samples indicate that there is no extra growth in oxide thickness even after 450°C PMA in O₂ ambient. Figure 3 shows the *I_G-V_G* curves for all samples. It could be found that the sample without

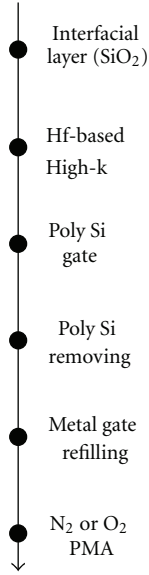


FIGURE 1: The fabrication process of the high-k metal gate last device.

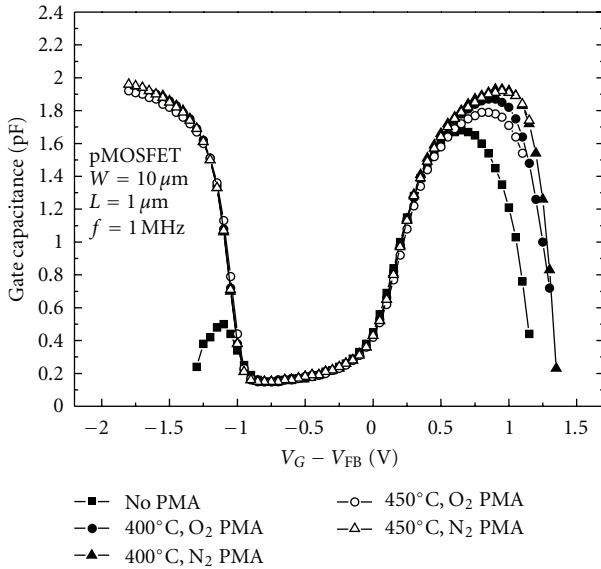


FIGURE 2: The $C-V$ curves with V_{FB} normalization.

PMA shows an obviously huge gate leakage current than other samples. On the other hand, the gate leakage current reduced after PMA in all conditions. The reduction of gate leakage current is because of the defects passivation in high-k/Si interface [7].

Figure 4 shows the I_G-V_G curves for samples with various PMA treatments. It could be observed that the device without annealing shows the most negative threshold voltage due to the existence of charged oxygen vacancy, and the threshold voltage shifts positiveward after PMA treatment. Both the threshold voltages are similar with various annealing temperatures for the nitrogen-annealed devices. On the other hand, the amount of threshold voltage

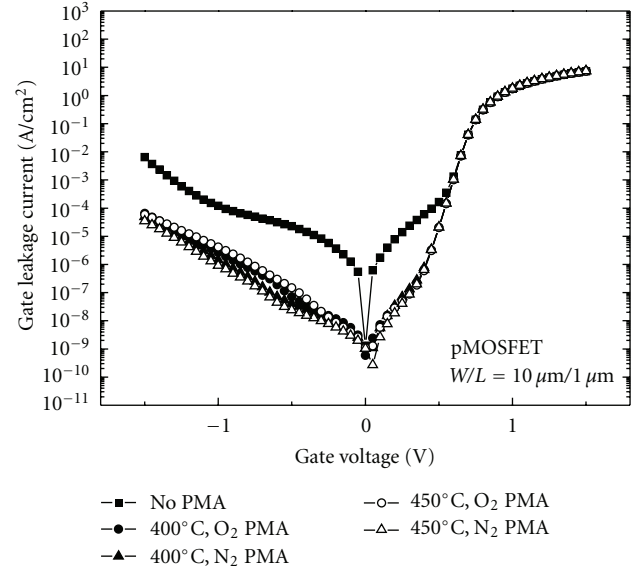


FIGURE 3: The I_G-V_G curves for samples with various PMA treatments.

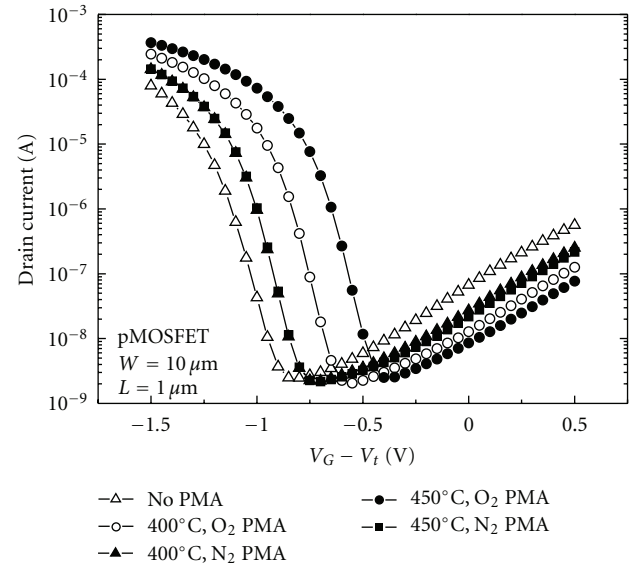
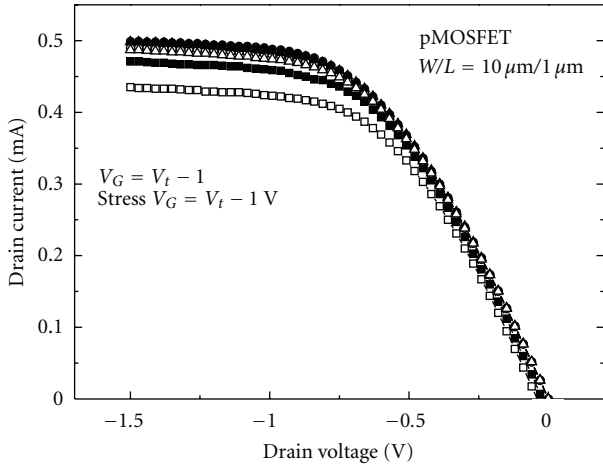


FIGURE 4: The I_D-V_G curves for samples with various PMA treatments.

shift of oxygen-annealed device is strongly dependent on the annealing temperature. The positive shift of threshold voltage might be due to the passivation of oxygen vacancies in the interfacial layer (IL) region [6]. Both the oxygen and nitrogen could be permeated through the TiN region and reach the IL region although TiN is commonly used as diffusion barrier. The phenomenon is suggested to reduce the threshold voltage of pMOSFET for the high-performance application.

Figure 5 shows the I_D-V_D curves with various PMA conditions before and after constant voltage stress, and the amount of degradation of I_D was extracted and shown in



Square: W/G PMA
 Circle: 400°C, O₂ PMA
 Triangle: 400°C, N₂ PMA
 Solid: before CVS
 Open: after CVS

FIGURE 5: I_D - V_D curve of pMOSFET with various PMA conditions before and after constant voltage stress.

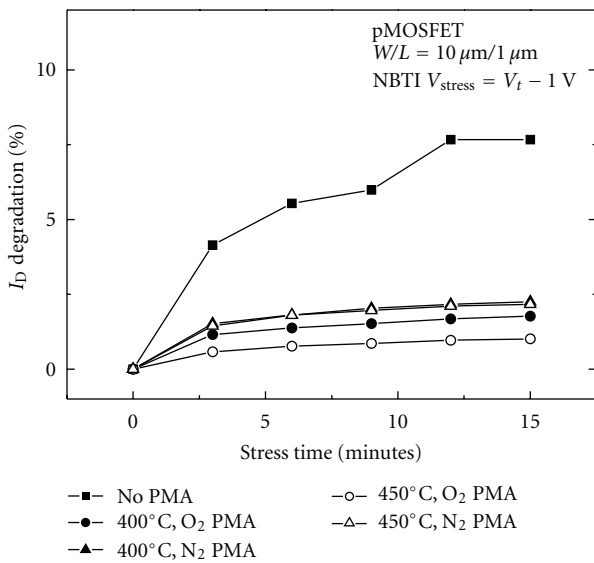
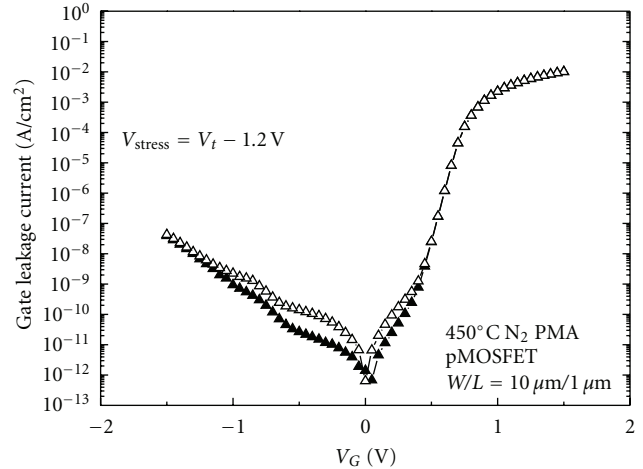


FIGURE 6: The extracted I_D degradation after constant voltage stress.

Figure 6. It could be observed that the device without PMA shows the worst device performance. On the other hand, the reliability is improved for devices with PMA treatment. As compared to the various PMA conditions, the oxygen devices with oxygen annealing show the better reliability than the device with oxygen annealing. The I_D degradation is suggested due to the breaking of passivated oxygen vacancies during stress. Compared to nitrogen, oxygen is believed to cause stronger bonding when passivating the dangling bonds of oxygen vacancies. As a result, the device with oxygen annealing shows the lowest I_D degradation.



▲ Fresh
 △ After 15-minute stress

FIGURE 7: The I_G - V_G curves of 450°C, N₂ annealed sample before and after stress.

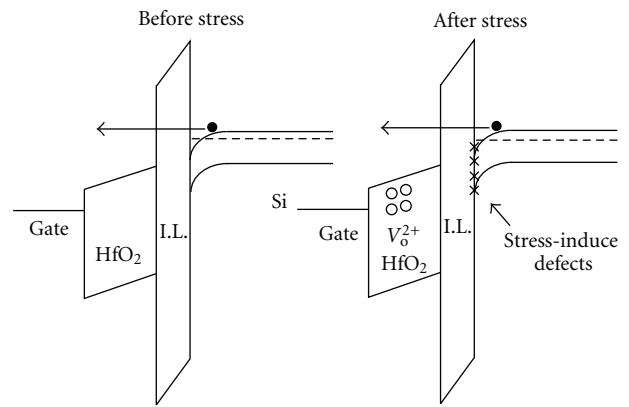


FIGURE 8: Band diagram of I_G - V_G curve in accumulation region.

In order to realize the mechanism of I_D degradation, the variation of gate leakage current before and after stress was investigated in this work. Figure 7 shows the I_G - V_G curves of samples annealed in N₂ ambient at 450°C before and after constant voltage stress. It could be found that the two curves overlap in the region of accumulation and strong inversion, and it divides in the region of depletion and weak inversion. The results could be explained using the following models as shown from Figure 8 to Figure 10. After applying a constant voltage stress, it is believed that some traps would be generated in both interface and high- k dielectric layer. When the device is biased to accumulation (see Figure 8), enough electrons would be injected from the substrate into the gate electrode by tunneling; as a result, the gate leakage current is independent of the generated traps. When the device is biased to depletion and weak inversion (see Figure 9), the gate leakage current includes two components: the generation holes and the gate-injected electrons. The stress-induced traps in the high- k dielectric layer would result in trap assistant tunneling from the gate

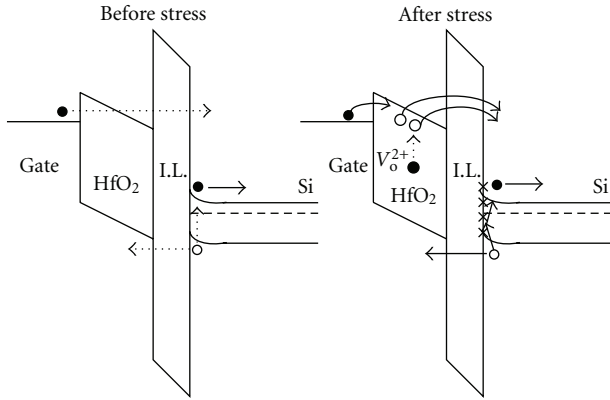


FIGURE 9: Band diagram of I_G - V_G curve in depletion and weak inversion region.

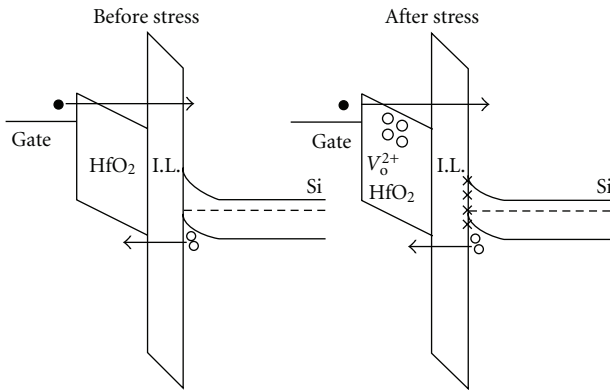


FIGURE 10: Band diagram of I_G - V_G curve in strong inversion region.

electrode, and the traps in the high- k /Si interface would enhance the generation holes. Both traps would increase the gate leakage current. In other words, more traps generated in both the gate dielectric layer and the interface would induce larger gate leakage current. As the electric field is large enough (see Figure 10), the electrons and holes would, respectively, pass through conduction band and valance band of the high- k layer. Therefore, the gate leakage current is independent of the stress-induced traps. From the above model, the gate leakage current variation is mainly attributed to both trap assistant tunneling and holes generation in depletion and weak inversion region. As shown in Figure 7, the devices with oxygen annealing have less variation of gate leakage current than those with nitrogen annealing. This could be explained that oxygen annealing has stronger bonding to passivate the dangling bonds of oxygen vacancies, which results in fewer traps generated during stress.

4. Conclusions

Postmetallization annealing was used in this work to improve the performance and reliability of the high- k /metal gate pMOSFET devices. The models show that the increase of gate leakage current after stress must be due to the traps generation in both high- k gate dielectric layer and high- k /Si

interface. It is believed that oxygen would cause the stronger bonding than nitrogen as passivating the dangling bonds of oxygen vacancies. As the results show, the devices with oxygen annealing show the least I_D degradation and gate leakage current variation than the others.

Acknowledgments

This work was supported by the National Science Council under Contract NSC 100-2221-E-390-004, NSC 100-2221-E-017-002, and the authors would like to thank UMC staff for their helpful supporting.

References

- [1] H. H. Tseng, P. J. Tobin, S. Kalpat et al., "Defect passivation with fluorine and interface engineering for Hf-based high- κ /metal gate stack device reliability and performance enhancement," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3267–3275, 2007.
- [2] S. Zafar, H. Jagannathan, L. F. Edge, and D. Gupta, "Oxygen vacancy mobility and diffusion coefficient determined from current measurements in SiO₂/HfO₂/TiN stacks," in *Proceedings of the International Conference on Solid State Devices and Materials*, p. 669, 2010.
- [3] S. Guha and V. Narayanan, "Oxygen vacancies in high dielectric constant oxide-semiconductor films," *Physical Review Letters*, vol. 98, no. 19, Article ID 196101, 2007.
- [4] K. Shiraishi, K. Yamada, K. Torii et al., "Oxygen vacancy induced substantial threshold voltage shifts in the Hf-based high- K MISFET with p+poly-Si gates -A theoretical approach," *Japanese Journal of Applied Physics, Part 2*, vol. 43, no. 11 A, pp. L1413–L1415, 2004.
- [5] M.-J. Jeng, H.-S. Lin, and J.-G. Hwu, "Rapid thermal post-metallization annealing effect on thin gate oxides," *Applied Surface Science*, vol. 92, pp. 208–211, 1996.
- [6] E. Cartier, M. Hopstaken, and M. Copel, "Oxygen passivation of vacancy defects in metal-nitride gated HfO₂/SiO₂/Si devices," *Applied Physics Letters*, vol. 95, no. 4, Article ID 042901, 2009.
- [7] C. C. Hong and J. G. Hwu, "Degradation in metal-oxide-semiconductor structure with ultrathin gate oxide due to external compressive stress," *Applied Physics Letters*, vol. 79, no. 23, pp. 3797–3799, 2001.



Hindawi

Submit your manuscripts at
<http://www.hindawi.com>

