Hindawi Publishing Corporation
Active and Passive Electronic Components
Volume 2013, Article ID 525017, 7 pages
http://dx.doi.org/10.1155/2013/525017

Research Article

Logic Gates and Ring Oscillators Based on Ambipolar Nanocrystalline-Silicon TFTs

Anand Subramaniam,[1] Kurtis D. Cantley,[2] and Eric M. Vogel[2,3]

[1] *Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX 75080, USA*
[2] *Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, TX 75080, USA*
[3] *School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA*

Correspondence should be addressed to Anand Subramaniam; asubram3@utdallas.edu

Received 2 August 2012; Revised 12 March 2013; Accepted 4 April 2013

Academic Editor: Olga Korostynsk

Nanocrystalline silicon (nc-Si) thin film transistors (TFTs) are well suited for circuit applications that require moderate device performance and low-temperature CMOS-compatible processing below 250°C. Basic logic gate circuits fabricated using ambipolar nc-Si TFTs alone are presented and shown to operate with correct outputs at frequencies of up to 100 kHz. Ring oscillators consisting of nc-Si TFT-based inverters are also shown to operate at above 20 kHz with a supply voltage of 5 V, corresponding to a propagation delay of <10 μs/stage. These are the fastest circuits formed out of nanocrystalline silicon TFTs to date. The effect of bias stress degradation of TFTs on oscillation frequency is also explored, and relatively stable operation is shown with supply voltages >5 V for several hours.

1. Introduction

Nanocrystalline silicon (nc-Si) has attracted much interest for use in circuit applications that require low temperature, large-area fabrication, and alternative substrates. Examples of these applications may include neuromorphic architectures for vision sensing [1, 2], flexible and flat-panel displays [3–5], radio frequency identification (RFID) tags [6], solar cells [7], and many more. Many of these applications do not require high performance devices, but rather the viability of a simple and inexpensive fabrication process. Neuromorphic circuits are also defect tolerant to a certain extent, allowing low-yield devices to be employed. Nc-Si thin film transistors (TFTs) can be fabricated using a CMOS-compatible fabrication process [8, 9], which also facilitates three-dimensional integration with high-performance CMOS structures [5, 10, 11]. In such a case, TFT circuitry such as biosensor arrays or neural networks could be fabricated around a CMOS core to improve the overall functionality.

The limited use of noncrystalline silicon devices in circuits was historically due to low carrier mobility [12], device degradation under bias stress [13, 14], and the lack of p-channel operation [15]. Use of nc-Si instead of amorphous silicon (a-Si) improves the electron mobility and device degradation to a certain extent. The above drawbacks have been further addressed in the recent years by high purity nc-Si deposition which reduces the incorporation of impurity oxygen in the channel layer and ensures ambipolar operation of the devices [8, 15]. In this context, the term "ambipolar" refers to either n- or p-channel operation depending on the bias conditions. The maximum mobility observed in nc-Si TFTs is 150 $cm^2/V{\cdot}s$ for electrons and 25 $cm^2/V{\cdot}s$ in case of holes [15]. The performance of these devices has also been considerably improved by utilizing thin high-κ gate dielectrics that reduce the subthreshold swing and threshold voltages (V_T) of these devices [16]. For instance, the switching power consumption of an ambipolar nc-Si TFT-based inverter operating at 100 Hz reduced from 5 pJ per switch to 350 fJ per switch when the gate dielectric was changed from 200 nm SiO_2 to 20 nm HfO_2. Fabrication of nanoscale TFTs has been demonstrated using electron beam lithography (EBL) [9]. Submicron device dimensions

are essential for use in high-density architectures such as neuromorphic systems [17]. In addition, nc-Si TFTs can be fabricated at temperatures of 250°C and below, allowing the incorporation of alternative substrates including polyimide [18] and steel foil [19]. The feasibility of fabricating circuits on such flexible substrates provides TFT technology with a distinct advantage over conventional CMOS technology.

The ambipolar operation of nc-Si TFTs also allows a single device type to be used to form a complementary inverter [9]. Such an arrangement ensures better inverter output range and a higher voltage gain than a source-follower inverter formed using an n-channel device. In contrast, many other low-temperature fabrication devices such as amorphous oxide TFTs operate solely in the n-channel mode. Therefore, inverters formed from such devices require either the integration of other devices such as resistors or use of a source follower configuration that prevents rail-to-rail output [20–22]. Both *n*- and *p*-channel organic TFTs have been recently developed and are the only other materials capable of producing complementary TFT inverters at low temperatures [23] for many of the applications discussed above. However, such devices typically have low mobilities, and therefore the circuits operate at very low switching speeds [24, 25]. Furthermore, rapid atmospheric degradation is observed in organic semiconductors [26], limiting their use.

In this paper, we present logic gates and ring oscillators that operate at low supply voltages formed using ambipolar nc-Si TFTs alone. The fabrication of these circuits is described in detail, followed by their electrical characterization. The operation of ring oscillators at different supply voltages is analyzed. The performance of these circuits is compared with that of similar circuits formed using alternate low-temperature materials. Finally, the circuits are electrically stressed for several hours to examine the effect of device degradation on their operation.

2. TFT Fabrication

The fabrication of nc-Si TFT-based circuits employs a four-level lithography process. The circuits contain 100 μm square pads at input and output nodes and were laid out for ease of electrical probing rather than the minimization of circuit area. A p-type Si wafer with moderate doping (10^{17} cm^{-3}) is used as the substrate on which 300 nm SiO_2 was grown with thermal oxidation. Initially, 80 nm Cr metal is deposited and patterned. This layer acts as source/drain of the individual TFTs as well as the bottom level of metal lines. All metal lines are 6 μm wide. Next, an 80 nm thick nc-Si layer is deposited using plasma-enhanced chemical vapor deposition (PECVD) at 13.56 MHz, 125 W RF power, 0.9 Torr, and 250°C deposition temperature in a 1 : 100 mixture of SiH_4 and H_2. A detailed description of the deposition condition is contained in [8]. The channel layer is then patterned with Cl chemistry-based plasma etching.

Following this, the HfO_2 gate dielectric with equivalent oxide thicknesses (EOTs) ranging from 7 nm to 2.5 nm was deposited using atomic layer deposition (ALD). EOTs were calculated assuming dielectric constant of 17 for HfO_2. This number is lower than the standard accepted value of 24 because the process temperature is 200°C. The third level of lithography was then used to pattern contact via holes through the gate dielectric, and 100 nm Au was used as contact metal. The final metal layer was Al (thickness 100 nm), used as gate metal as well as the top level of metal lines. A 2-hour long, 250°C anneal in forming gas completed the process. Individual transistors, inverters, logic gates, and the ring oscillators were fabricated using the same mask set. Figure 1 shows a schematic of the nc-Si TFT.

3. Electrical Characteristics of TFT and Inverter

Current-voltage (I-V) characteristics (both transfer and output) when a 20 μm × 10 μm nc-Si TFT with 20 nm HfO2 gate dielectric is operated with top-gate bias (grounding the substrate) are shown in Figures 2(a) and 2(b). The device exhibits ambipolar operation, that is, it operates in both the electron and hole regimes. The direction of current flow depends solely on the drain voltage. The applied gate voltage determines which charge carriers dominate in the channel: electrons constitute the charge flow when the gate voltage is positive and holes at negative bias.

Low hysteresis of less than 50 mV/dec. was observed in the *I-V* measurements (also Figure 2(a)), and the I_{ON}/I_{OFF} ratio when operated at a drain voltage of |1 V| is $>10^5$. At higher drain voltage values, the on/off ratio reduces because both hole and electron conduction occur for a larger range of gate voltages. Mobility values were extracted from the *I-V* characteristics. The maximum electron and hole mobilities observed are 20 cm^2/V·s and 5 cm^2/V·s, respectively. The corresponding subthreshold swing values are 0.6 V/decade and 0.65 V/decade.

Figure 3(a) shows the voltage transfer characteristics of a nc-Si TFT-based inverter ($W_{\text{pull-up}}/W_{\text{pull-down}} = 4$) at different operating voltages. The static CMOS topology was selected for the fabricated inverter since it offers the best output voltage range and voltage gain for ambipolar TFTs. Since the TFTs are ambipolar, no need exists for separate *n*- and *p*-channel devices in the inverter. The inverter exhibits close to peak-to-peak operation and high voltage gain (in the range 12–15). Slight deviation from peak-to-peak exists due to the ambipolar nature of the TFTs: the drive TFT does not completely turn off at low input and vice versa. The high gain can be attributed to the good saturation characteristics of the component devices. The dynamic characteristics of the inverter were also investigated by applying square voltage pulses at different frequencies. The inverter was able to respond closely to the input beyond 2 MHz [9], as shown in Figure 3(b). The switching speed could be minimized further by reducing the gate-to-source/drain overlap capacitance, which was not optimized in the current process.

4. Logic Gates

Logic gate circuits including NOR, NAND, OR, and AND were fabricated. OR and AND gates were realized by adding

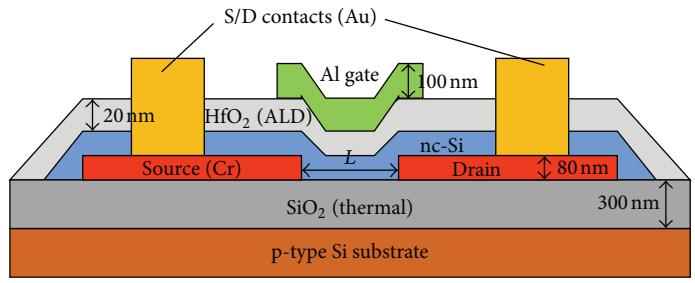

FIGURE 1: Schematic cross-section of a staggered top-gated nc-Si TFT.

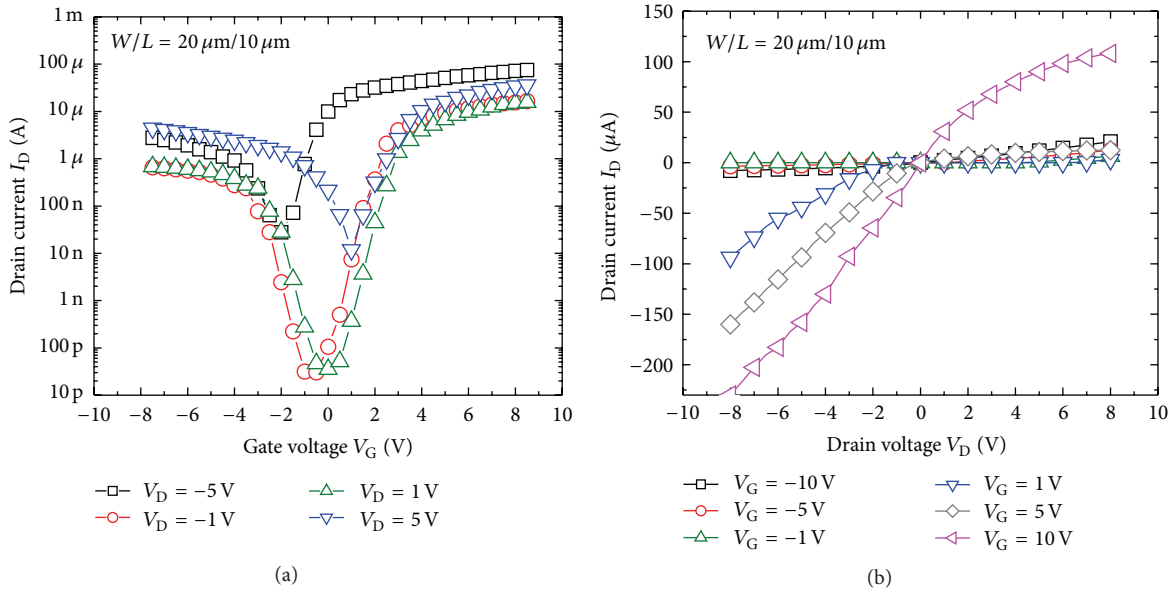

FIGURE 2: Current-voltage (I-V) characteristics of a 20 μm × 10 μm ambipolar nc-Si TFT with 20 nm HfO_2 gate dielectric. (a) Transfer characteristics ($I_D - V_G$) in both forward (symbols) and reverse (lines) directions illustrating the low hysteresis in the device and (b) output characteristics ($I_D - V_D$).

an inverter at the output of the NOR and NAND gates, respectively, and were composed of six ambipolar TFTs each (Figure 4). A single device type is sufficient for each gate, but TFTs were sized for minimum delay according to the circuit configuration, as shown in the figure.

Figure 5 shows the operation of the different logic gates at V_{DD} = 5 V. The input waveforms A and B have amplitude 5 V and frequency 100 kHz. The transition between input states occurs with rise and fall times of 10 ns. All possible combinations of inputs are shown. The outputs respond with no perceptible delay to each input change. The logic output values are correct in all cases, although the outputs deviated from the supply voltage or ground in some cases by up to 10% of V_{DD} due to the ambipolar nature of the TFTs. The nc-Si TFT-based logic gates operate at a similar frequency to high-quality organic transistor-based circuits at a much lower supply voltage [24].

5. Ring Oscillators

Three-, five-, or seven-stage ring oscillators were fabricated by connecting nc-Si TFT inverters in series, with the output of the last stage feeding back to the first. Figure 6 shows such a fabricated seven-stage ring oscillator. Each inverter was similar to the one in Section 3 and had a geometry ratio of four. To start the oscillations, the output of one of the stages was pulsed with a short square pulse. This set off the oscillations which stabilized at a set frequency depending on the number of stages and the supply voltage V_{DD}. Figure 7 shows the buildup of oscillations in three- and five-stage ring oscillators. At a supply voltage of 5 V, the oscillation frequencies are 21 kHz and 12 kHz, respectively. The total number of ring oscillators tested for each number of stages was approximately 15; the observed frequency variation was below 10%. The yield of operating circuits was >97%, which

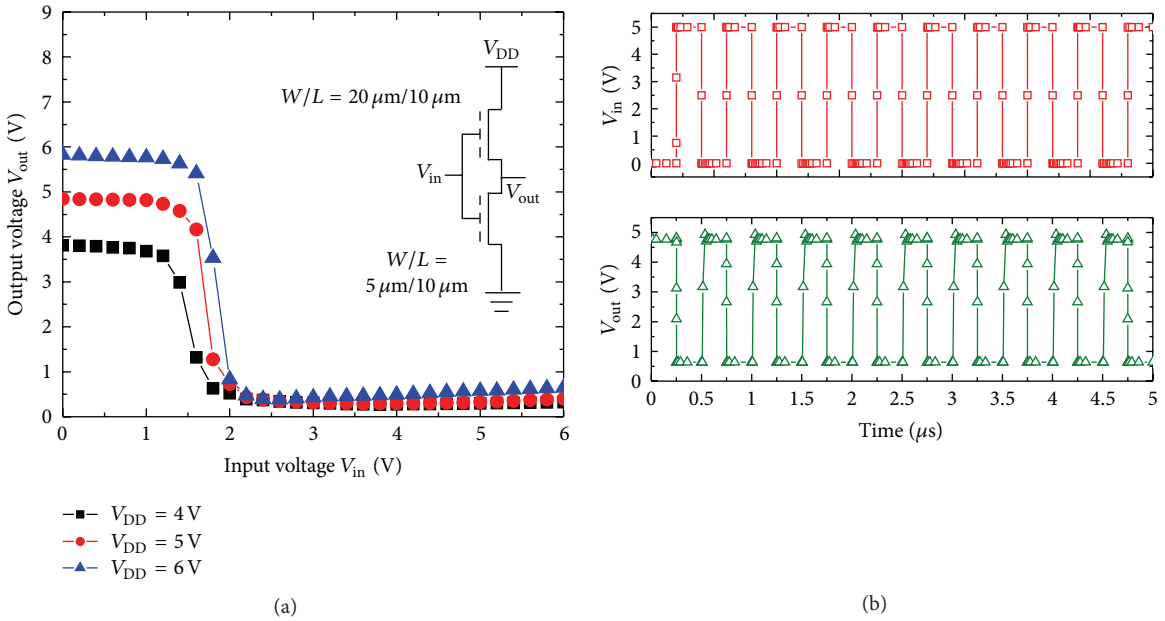

FIGURE 3: (a) Voltage transfer characteristics of an inverter formed using two ambipolar nc-Si TFTs with 20 nm HfO_2 gate dielectric measured at different operating voltages. (b) Operation of the inverter at 2 MHz input frequency and V_{DD} = 5 V.

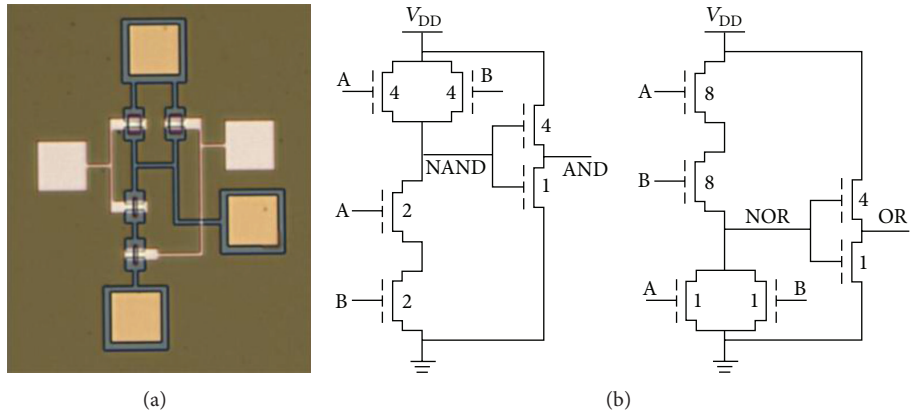

FIGURE 4: (a) Optical microscope image of a 2-input NAND gate fabricated using nc-Si TFTs. (b) Circuit diagram of the NAND, AND, NOR, and OR logic gates. The AND and OR gates are built by adding an inverter at the out of the NAND and NOR gates, respectively.

is reasonable for a first demonstration. A five-stage ring oscillator operating at 20 kHz (V_{DD} = 5 V) consumes approximately 0.5 μW.

The supply voltage was varied while testing the oscillators. An increase in voltage swing and a reduction in the propagation delay were observed with increase in V_{DD}. For instance, the circuit starts oscillating with V_{DD} as low as 3 V with propagation delay of ~14 μs/stage. At V_{DD} = 8 V, the frequency increases to 38 kHz, corresponding to a delay of 4 μs/stage. This trend is illustrated in Figure 8. The propagation delays compare well with other ring oscillator circuits fabricated using low-temperature technology [20, 22–28]. This is also the first instance of noncrystalline silicon TFT-based ring oscillators operating at low-(<5 V)-supply voltages. The operating frequency of these circuits would also benefit from reduced parasitic capacitance in the devices.

In addition to varying the supply voltage, ring oscillators with different channel lengths were also tested (retaining the same channel widths). Figure 9 shows the relationship between channel length and propagation delay for three different values of V_{DD}. The delay is minimum for L = 2 μm and increases with channel length, following a similar trend

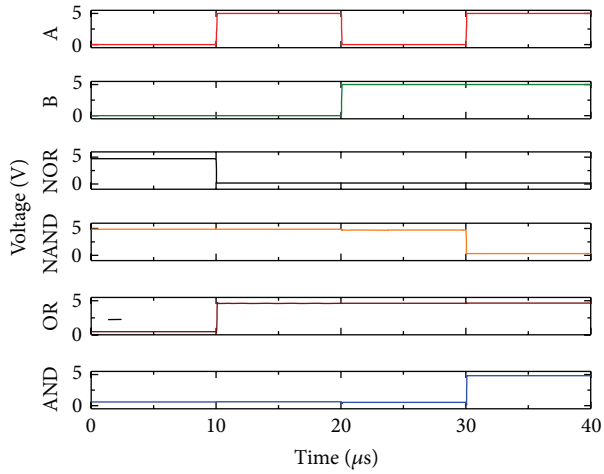

FIGURE 5: Operation of nc-Si TFT-based logic gates: (a) and (b) show input waveforms, and (c)–(f) show the outputs of OR, AND, NOR, and NAND gates, respectively.

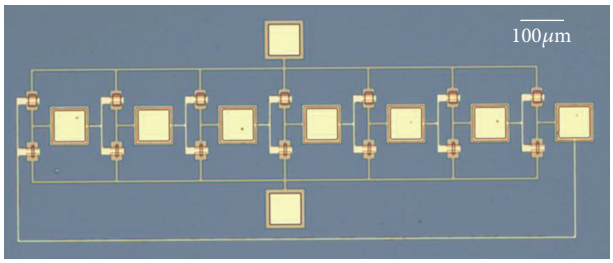

FIGURE 6: A fabricated seven-stage ring oscillator consisting of ambipolar nc-Si TFTs.

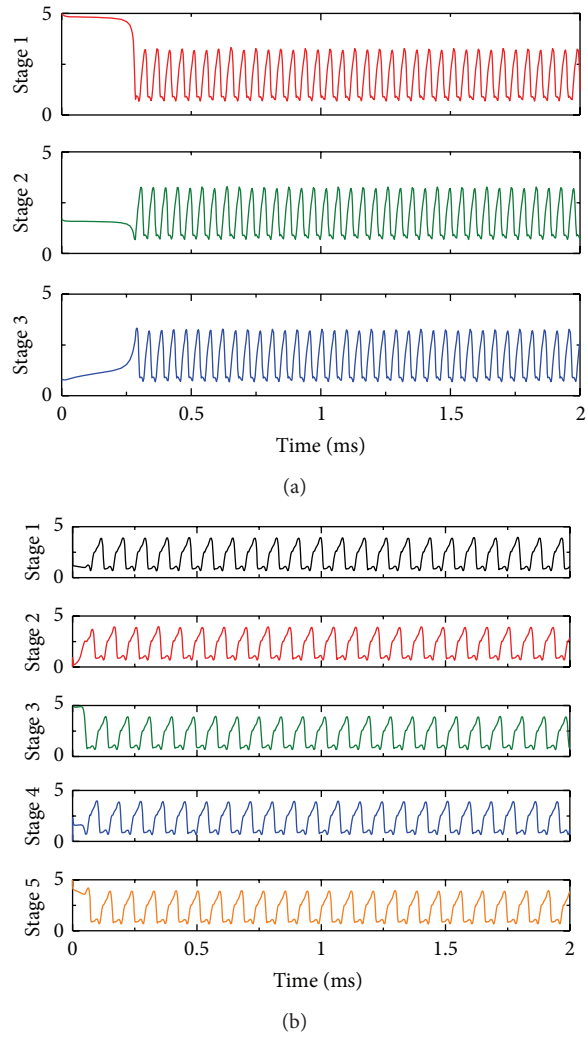

FIGURE 7: (a) Operation of a three-stage ring oscillator at $V_{DD} = 5$ V. Waveforms at the output of each stage are shown. The oscillation frequency is approximately 21 kHz. (b) Operation of a five-stage ring oscillator at $V_{DD} = 5$ V. The oscillation frequency is approximately 12 kHz.

as observed in [25]. This trend can be attributed to higher drive currents in TFTs with higher W/L values.

It is known that nc-Si TFTs suffer from threshold voltage degradation upon bias stressing [9, 13, 14, 29]. The dominant mechanism for this is believed to be defect state creation in the channel layer [5, 13]. To quantify the effect of device degradation on ring oscillator operation, a three-stage ring oscillator was operated at different supply voltages for increasing time periods. The oscillation frequency was measured after each stress period. The results (Figure 10) show that after long periods of continuous operation the oscillation frequency decreased for all supply voltages. The maximum reduction occurred for $V_{DD} = 7$ V in which case the frequency reduced by 43% after a stress period of 10^4 s. Similar trends were observed for each V_{DD} value. Although any device degradation is adverse to the circuit, the observed frequency reduction is a large improvement over other low-temperature fabricated ring oscillators [22]. This can be further improved by performing nc-Si depositions at slightly higher temperatures or potentially by further optimization of the deposition conditions.

6. Conclusion

In this work, logic gates and ring oscillators fabricated using ambipolar nc-Si TFTs have been demonstrated. Use of nc-Si as channel material enables low-cost large-area fabrication of circuits using these TFTs. The fabrication process employed uses low temperature (maximum of 250°C) and is CMOS compatible. The devices do not degrade upon exposure to the atmosphere and are robust. The logic gates were shown to operate with correct outputs at frequencies up to 100 kHz and rapid switching between states. Ring oscillators consisting of up to seven stages were fabricated and characterized. The oscillation frequencies varied from 8 kHz to 55 kHz depending on the supply voltage and channel length, corresponding to delays of approximately 3 μs to 20 μs per

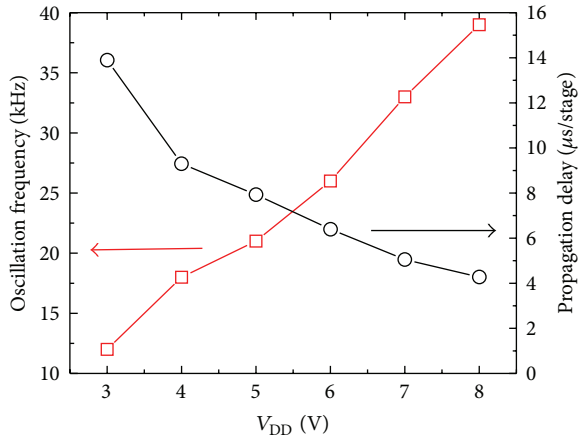

Figure 8: Variation of frequency of oscillation and propagation delay with supply voltage in a three-stage ring oscillator.

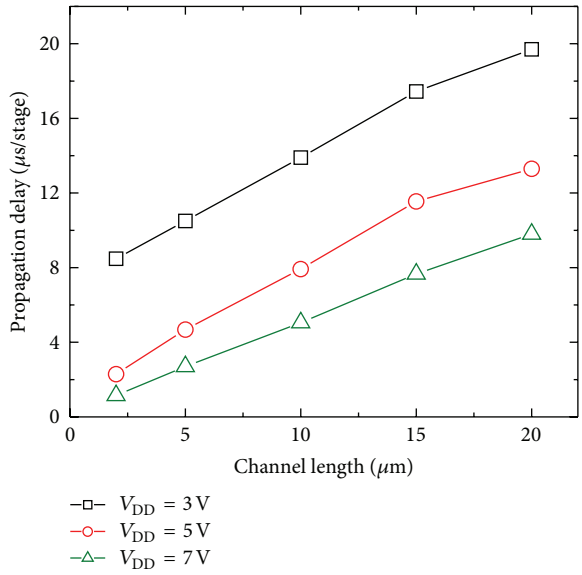

Figure 9: Variation of propagation delay with channel length in three-stage ring oscillators for different values of supply voltage.

stage. The yield and reproducibility of either type of circuit were >97%, which is reasonable for a first demonstration. Finally, the ring oscillator circuits were electrically stressed by continuous operation beyond 10^4 s to examine the effect of bias stress degradation of nc-Si TFTs. The oscillation frequencies reduced upon long periods of stress, but this reduction was lower than that observed in other circuits with low-temperature fabrication processes.

Although the circuits were fabricated as large area for ease of probing, nanoscale circuits using nc-Si TFTs are certainly feasible. Submicron nc-Si TFTs fabricated using electron

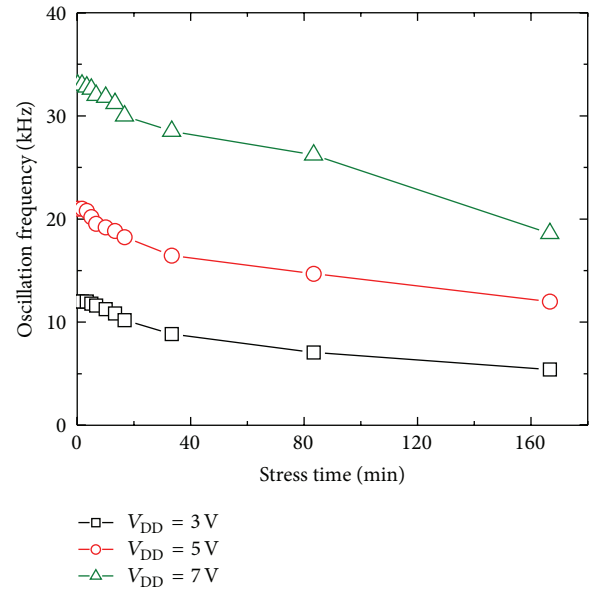

Figure 10: Effect of bias stress degradation on frequency of oscillation of a three-stage ring oscillator at various supply voltages.

beam lithography have been demonstrated elsewhere, and the same process could be extended to produce compact circuits.

References

[1] K. D. Cantley, A. Subramaniam, H. Stiegler, R. Chapman, and E. Vogel, "Hebbian learning in spiking neural networks with nano-crystalline silicon TFTs and memristive synapses," *IEEE Transactions on Nanotechnol*, vol. 10, no. 5, pp. 1066–1073, 2011.

[2] C. Koch, "Neuromorphic vision chips," *IEEE Spectrum*, vol. 33, no. 5, pp. 38–46, 1996.

[3] A. J. Snell, K. D. Mackenzie, W. E. Spear, P. G. LeComber, and A. J. Hughes, "Application of amorphous silicon field effect transistors in addressable liquid crystal display panels," *Applied Physics*, vol. 24, no. 4, pp. 357–362, 1981.

[4] T. Tsukuda, *Technology and Applications of Amorphous Silicon, Springer Series in Material Science*, vol. 37, Springer, Berlin, Germany, 2000.

[5] D. Knipp, R. A. Street, H. Stiebig et al., "Vertically integrated amorphous silicon color sensor arrays," *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1551–1558, 2006.

[6] I. C. Y. Kwong, H. J. Lee, and A. Sazonov, "Nanocrystalline silicon diodes for rectifiers on RFID tags," *MRS Proceedings*, vol. 1066, 2008.

[7] C. Min, Z. Weijia, W. Tianmin, J. Fei, L. Guohua, and D. Kun, "Nanocrystalline silicon films with high conductivity and the application for PIN solar cells," *Vacuum*, vol. 81, no. 1, pp. 126–128, 2006.

[8] A. Subramaniam, K. D. Cantley, R. A. Chapman, B. Chakrabarty, and E. M. Vogel, "Ambipolar non-crystalline-silicon TFTs with submicron dimensions and reduced threshold voltage shift," in *Proceeding of the 69th Annual Device Research Conference (DRC '11)*, June 2011.

[9] A. Subramaniam, K. D. Cantley, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, "Submicron ambipolar nanocrystalline silicon

thin-film transistors and inverters," *IEEE Transactions on Electron Devices*, vol. 59, no. 2, pp. 359–366, 2012.

[10] K. K. Likharev, "Neuromorphic CMOL circuits," in *Proceedings of the 3rd IEEE Conference on Nanotechnology Conference Digest (IEEE Nano '03)*, vol. 2, pp. 339–342, August 2003.

[11] Y. Nara, Y. Kudou, and M. Matsumura, "Application of amorphous-silicon field-effect transistors in three-dimensional integrated circuits," *Japanese Journal of Applied Physics*, vol. 22, no. 6, pp. L370–L372, 1983.

[12] B. Stannowski, R. E. I. Schropp, R. B. Wehrspohn, and M. J. Powell, "Amorphous-silicon thin-film transistors deposited by VHF-PECVD and hot-wire CVD," *Journal of Non-Crystalline Solids*, vol. 299–302, no. 2, pp. 1340–1344, 2002.

[13] M. J. Powell, C. Van Berkel, I. D. French, and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," *Applied Physics Letters*, vol. 51, no. 16, pp. 1242–1244, 1987.

[14] A. R. Hepburn, J. M. Marshall, C. Main, M. J. Powell, and C. Van Berkel, "Metastable defects in amorphous-silicon thin-film transistors," *Physical Review Letters*, vol. 56, no. 20, pp. 2215–2218, 1986.

[15] C. H. Lee, A. Sazonov, and A. Nathan, "High hole and electron mobilities in nanocrystalline silicon thin-film transistors," *Journal of Non-Crystalline Solids*, vol. 352, no. 9-20, pp. 1732–1736, 2006.

[16] A. Subramaniam, K. D. Cantley, R. A. Chapman, H. J. Stiegler, and E. M. Vogel, "Submicron ambipolar nanocrystalline-silicon TFTs with high-κ gate dielectrics," in *Proceedings of the International Semiconductor Device Research Symposium (ISDRS '11)*, December 2011.

[17] K. D. Cantley, A. Subramaniam, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, "SPICE simulation of nanoscale noncrystalline silicon TFTs in spiking neuron circuits," in *Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS '10)*, pp. 1202–1205, August 2010.

[18] H. Gleskova, S. Wagner, V. Gašparík, and P. Kováč, "150∘C amorphous silicon thin-film transistor technology for polyimide substrates," *Journal of the Electrochemical Society*, vol. 148, no. 7, pp. G370–G374, 2001.

[19] E. Y. Ma and S. Wagner, "Amorphous silicon transistors on ultrathin steel foil substrates," *Applied Physics Letters*, vol. 74, no. 18, pp. 2661–2662, 1999.

[20] C. G. Lee, T. Joshi, K. Divakar, and A. Dodabalapur, "Circuit applications based on solution-processed zinc-oxide TFTs," in *Proceedings of the 69th Device Research Conference, Conference Digest (DRC '11)*, June 2011.

[21] J. Sun, D. A. Mourey, D. Zhao et al., "ZnO thin-film transistor ring oscillators with 31-ns propagation delay," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 721–723, 2008.

[22] K. H. Kim, Y. H. Kim, H. J. Kim, J. I. Han, and S. K. Park, "Fast and stable solution-processed transparent oxide thin-film transistor circuits," *IEEE Electron Device Letters*, vol. 32, no. 4, pp. 524–526, 2011.

[23] T. D. Anthopoulos, D. M. De Leeuw, E. Cantatore et al., "Organic complementary-like inverters employing methanofullerene-based ambipolar field-effect transistors," *Applied Physics Letters*, vol. 85, no. 18, pp. 4205–4207, 2004.

[24] B. Crone, A. Dodabalapur, Y. Y. Lin et al., "Large-scale complementary integrated circuits based on organic transistors," *Nature*, vol. 403, no. 6769, pp. 521–523, 2000.

[25] H. Klauk, M. Halik, U. Zschieschang et al., "Flexible organic complementary circuits," *IEEE Transactions on Electron Devices*, vol. 52, no. 4, pp. 618–622, 2005.

[26] E. J. Meijer, D. M. De Leeuw, S. Setayesh et al., "Solution-processed ambipolar organic field-effect transistors and inverters," *Nature Materials*, vol. 2, no. 12, pp. 678–682, 2003.

[27] D. Zhao, D. A. Mourey, and T. N. Jackson, "Fast flexible plastic substrate ZnO circuits," *IEEE Electron Device Letters*, vol. 31, no. 4, pp. 323–325, 2010.

[28] K. Hiranaka, T. Yamaguchi, and S. Yanagisawa, "Self-alignment processed amorphous silicon ring oscillators," *IEEE Electron Device Letters*, vol. 5, no. 7, pp. 224–225, 1984.

[29] D. R. Allee, L. T. Clark, B. D. Vogt et al., "Circuit-level impact of a-Si: H thin-film-transistor degradation effects," *IEEE Transactions on Electron Devices*, vol. 56, no. 6, pp. 1166–1176, 2009.