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Research Article

A Novel Nanoscale FDSOI MOSFET with Block-Oxide

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We demonstrate improved device performance by applying oxide sidewall spacer technology to a block-oxide-enclosed Si body to create a fully depleted silicon-on-insulator (FDSOI) nMOSFET, which overcomes the need for a uniform ultrathin silicon film. The presence of block-oxide along the sidewalls of the Si body significantly reduces the influence of drain bias over the channel. The proposed FDSOI structure therefore outperforms conventional FDSOI with regard to its drain-induced barrier lowering (DIBL), on/off current ratio, subthreshold swing, and threshold voltage rolloff. The new FDSOI structure is in fact shown to behave similarly to an ultrathin body (UTB) SOI but without the associated disadvantages and technological challenges of the ultrathin film, because a thick Si body allows for reduced sensitivity to self-heating, thereby improving thermal stability.

1. Introduction

Semiconductor science, triggered by the impetus of a growing market for faster, more reliable, and less costly chips, has been undergoing a rapid technological development [1]. Many of these new technologies, however, suffer from undesirable side effects. For example, as the gate length of CMOS—the bulk complementary metal-oxide semiconductor—is decreased, short-channel effects (SCEs), such as drain-induced barrier lowering (DIBL) and threshold voltage (V_{TH}) rolloff, become a significant problem because S/D encroachment begins to limit the gate's ability to control the channel. Also, due to the existence of the PN junction between the Si substrate and the S/D regions, a large junction leakage current prevents the use of scaled-down transistors in low standby power (LSTP) applications. Moreover, the parasitic capacitance of the transistor may strongly affect the characteristics of CMOS devices [2–4]. Therefore, the use of planar technology for ultralarge-scale integrated (ULSI) circuits becomes more challenging.

Recently, silicon-on-insulator (SOI) technology has demonstrated promise for nano-CMOS scaling. Compared to its bulk Si counterparts, SOI offers reduced capacitance and lower OFF-state leakage current (I_{OFF}), mainly due to the presence of a buried oxide (BOX) layer under the Si active layer [5]. This can be attributed to the fact that the BOX can be seen as a "blocking layer" to reduce the drain electric field. Also, because the active region is fully isolated, it avoids the latch-up problem of classical CMOS devices.

The benefits of SOI technology, however, are not without associated problems. A partially depleted (PD) SOI transistor cannot achieve an improved performance in future sub-45 nm semiconductor devices, due to the electrical properties of PDSOI MOSFET relative to the thickness of the Si layer. It has been proved that a thick Si film makes reducing DIBL very difficult [6]. The fully depleted (FD) ultrathin body (UTB) SOI MOSFET is able to improve the short-channel characteristics but suffers from high S/D series resistance, because the semiconducting Si layer is, by definition, ultrathin. Also, when the gate-to-source overdrive voltage (V_{GT}) is high enough, the self-heating effect causes a negative incremental conductance in the UTBSOI MOSFET associated with thermal instability. Consequently, the reliability of SOI devices will be degraded by these issues [7–11].

Our previous studies revealed that some of the unique features of the FDSOI MOSFET with block-oxide (bFDSOI) could allow it to replace the UTBSOI structure for CMOS scaling [12–14]. The device parameters of bFDSOI and UTBSOI were not optimized; however, neither bFDSOI nor UTBSOI showed high drain ON-state current (I_{ON}). Now, equipped with a block-oxide-enclosed Si body using oxide sidewall spacer technology, this paper presents a fully

depleted silicon-on-insulator (FDSOI) nMOSFET to improve device performance, without using ultrathin silicon film. Also, the authors have optimized the device parameters to enhance current drive without losing the desired electrical characteristics.

This paper is organized as follows: the device structures and their corresponding simulations are described in Section 2. In Section 3, the electrical characteristics are compared between the bFDSOI-FETs and their counterparts in the FDSOI-FET, UTBSOI-FET, and elevated S/D (E-S/D) UTBSOI-FET before a brief summary is carried out in Section 4.

2. Device Structures and Simulations

ISE-TCAD was used to design and simulate the thin S/D and the recessed S/D bFDSOI-FETs. The key steps for processing the bFDSOI are shown in Figure 1. First, the Si body was patterned with e-beam (see Figure 1(a)), and for thin S/D bFDSOI-FET, 60 nm thick oxide was deposited using chemical vapor deposition (CVD) as a blocking layer. The deposited oxide layer was then etched back to form the sidewall spacers of the Si body (see Figure 1(b-1)). A layer of poly-Si (5 nm thick) was then deposited to act as an active layer (see Figure 1(c-1)). For the recessed S/D bFDSOI-FET, a 15 nm thick oxide was deposited and etched back to form the sidewall spacers of the Si body (see Figure 1(b-2)). Next, poly-Si was deposited and planarized with chemical mechanical polishing (CMP). Poly-Si (5 nm thick) was then redeposited to form the active region (see Figure 1(c-2)). For both bFDSOI-FETs, a 2.3 KeV boron difluoride (BF_2) channel implantation at a dosage of 1.15×10^{12} cm^{-2} was performed, followed by rapid thermal annealing. Hence, the values of V_{TH} for both devices were determined. Then, 1.4 nm thick oxide was grown and a 50 nm thick poly-Si layer was deposited, followed by gate patterning. After gate patterning, a layer of nitride was deposited and etched back by dry etching. Next, 10 nm oxide was deposited as an implantation screen layer. In order to form S/D regions for bFDSOI-FETs, arsenic ions were implanted at a dosage of 2.1×10^{14} cm^{-2} and an ion implantation energy of 14 KeV, followed by thermal annealing. As a result, the source/drain resistance for both devices was determined playing an important role in drain currents. The second sidewall spacers were then formed by dry etching. After contact formation, bFDSOI-FETs were achieved.

In this paper, some technical "tricks", such as S/D extension (SDE) implants [15], asymmetric halo [16], and retrograde channel profiles [17], were not used for our bFDSOI-FETs because the purpose of this work is to emphasize the importance of the block-oxide in reducing the SCEs. The device parameters used are listed as follows. For thin S/D and recessed S/D bFDSOI-FETs, typical values of Si body thickness (T_{Si}) and poly-Si channel thickness (T_{CH}) were 30 nm and 5 nm, respectively. Additionally, three types of SOI MOSFETs (FDSOI, UTBSOI, and E-S/D UTBSOI) were designed; the parameters were based on the same conditions for the simulation. For the FDSOI-FET, the typical value of T_{Si} is 30 nm. For the UTBSOI-FET, the typical value of T_{Si} ($= T_{CH}$) is 5 nm. For the E-S/D UTBSOI-FET, the typical value of T_{Si} ($= T_{CH}$) is 5 nm, and the raised S/D thickness is 35 nm. The other parameters, BOX thickness (T_{BOX}) and front-gate oxide thickness (T_{GOX}) are 50 nm and 1.4 nm, respectively.

3. Results and Discussion

The physics models in this paper, including the generation and recombination model, the effective intrinsic density model, and the basic mobility models, were specified for the I_{DS}-V_{GS} characteristics of bFDSOI-FETs and its counterparts. Among them, the mobility models include a doping-dependence model and a high-field-saturation model (velocity saturation for electrons), based on the hydrodynamic Canali model. Besides the models used in I_{DS}-V_{GS} simulation, a local-carrier temperature-dependent impact-ionization model is attached to the generation and recombination models, a transverse-field dependence model is attached to the basic mobility models, and a hydrodynamic model is used to simulate numerically the I_{DS}-V_{DS} characteristics of bFDSOI-FETs and its counterparts [18].

For bFDSOI-FETs, owing to the presence of single crystal Si body, the poly-Si active layer can be recrystallized after annealing. In the simulation study, the crystalline Si values used for bFDSOI-FETs were the same as those used for FDSOI and UTBSOI devices. The major parameters for the comparison are listed as follows. V_{DS} is the voltage bias applied between drain and source, $V_{TH,lin}$ is the linear threshold voltage at $V_{DS} = 0.05$ V, and $V_{TH,sat}$ is the saturation threshold voltage at $V_{DS} = 1.0$ V. The threshold voltage is extracted using the constant current method at $I_{DS} = 1\,\mu A/\mu m$. The saturation current (I_{ON}) is the drain current at $V_{GS} = V_{DS} = 1.0$ V. The leakage current (I_{OFF}) is the drain current at $V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V. DIBL is the difference between the $V_{TH,lin}$ and the $V_{TH,sat}$. In order to adjust the V_{TH} and optimize the I_{ON}/I_{OFF}, the barrier of doped poly-Si (gate electrode) is chosen as 0.45 eV because this is the difference between the poly-Si extrinsic Fermi level and the Si intrinsic Fermi level [18].

Figure 2 shows the surface potential plots for both the bFDSOI and SOI MOSFETs with gate length of $L_G = 30$ nm. As shown in Figure 2, there is no significant change in the potential for bFDSOI-FETs as V_{DS} increases, although a slight change in the potential is observed. However, the FDSOI MOSFET (green line) still shows an increase due to the SCEs. This means that the thick FD scheme cannot effectively handle the issue of DIBL. These results confirm that the influence of drain bias upon the channel current has been reduced. As a consequence, the block-oxide-enclosed Si body helps suppress the SCEs, leading to an improved subthreshold swing and a decrease in I_{OFF}. Unfortunately, the V_{DS} appears to drop across the S/D regions rather than the channel regions, which leads to smaller effective V_{DS} which then drops across the channel region. This is not the ideal condition for a comparison of the properties of the intrinsic devices designed. The reason for this is that we have

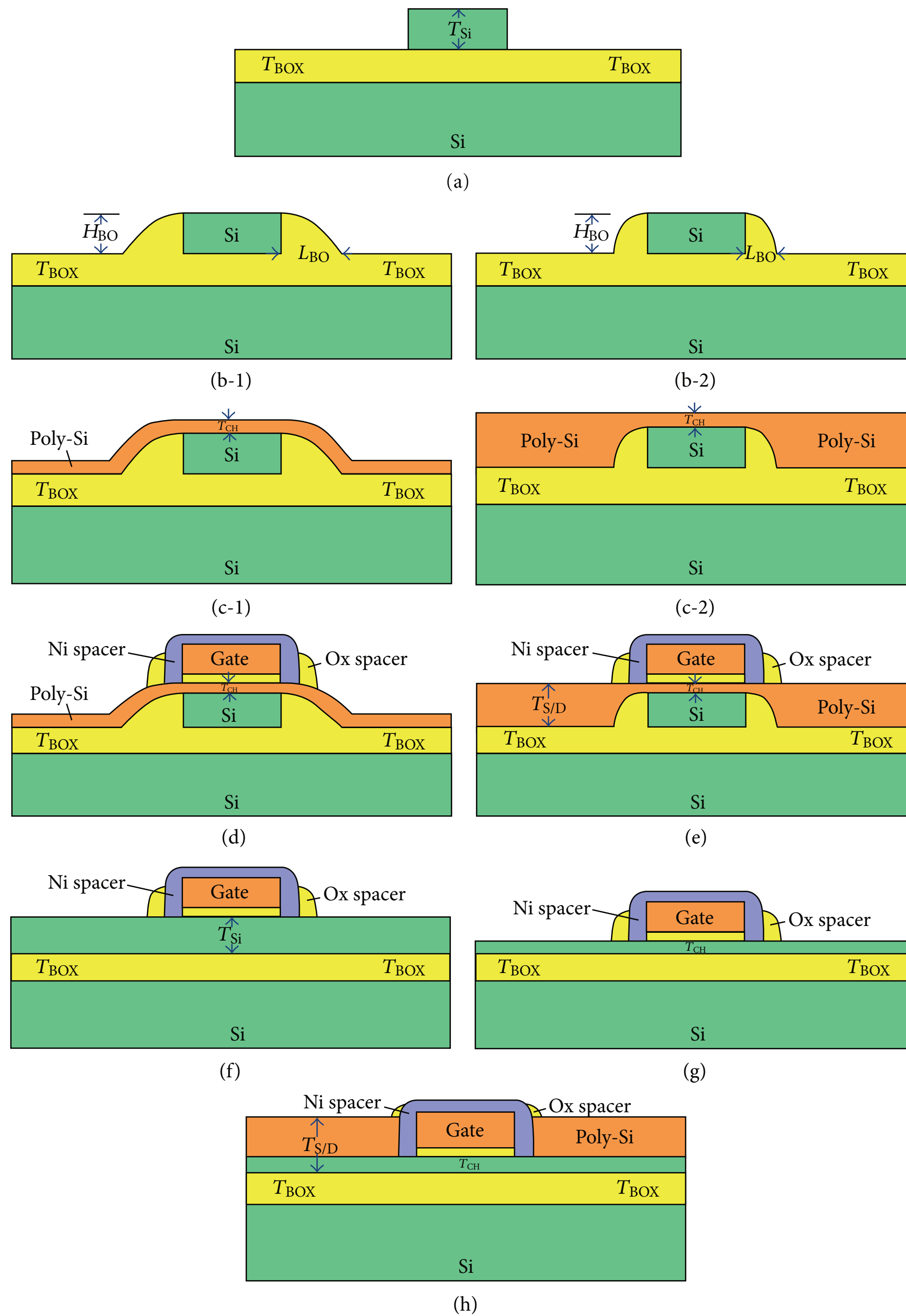

Figure 1: Schematic of the process flow of bFDSOI-FETs. (a) Si body patterning. (b-1) Block-oxide formation, where the height of the block-oxide (H_{BO}) is equal to the Si body thickness (T_{Si}) and the length of the block-oxide (L_{BO}) is 60 nm for thin S/D bFDSOI-FET. (b-2) Block-oxide formation, where the H_{BO} is equal to the T_{Si} and the L_{BO} is 15 nm for recessed S/D bFDSOI-FET. (c-1) Poly-Si deposition. (c-2) Poly-Si deposition, planarization, and deposition again. (d) A thin S/D bFDSOI-FET. (e) A recessed bFDSOI-FET. (f) An FDSOI-FET. (g) A UTBSOI-FET. (h) An E-S/D UTBSOI-FET. For thin S/D and recessed S/D bFDSOI-FETs, typical values of T_{Si} and poly-Si channel thickness (T_{CH}) are 30 nm and 5 nm, respectively. For FDSOI-FET, the typical value of T_{Si} is 30 nm. For UTBSOI-FET, the typical value of T_{Si} (= T_{CH}) is 5 nm. For E-S/D UTBSOI-FET, typical values of T_{Si} (= T_{CH}) and poly-Si raised S/D thickness are 5 nm and 30 nm, respectively. For other parameters, BOX thickness (T_{BOX}) and front-gate oxide thickness (T_{GOX}) are 50 nm and 1.4 nm, respectively.

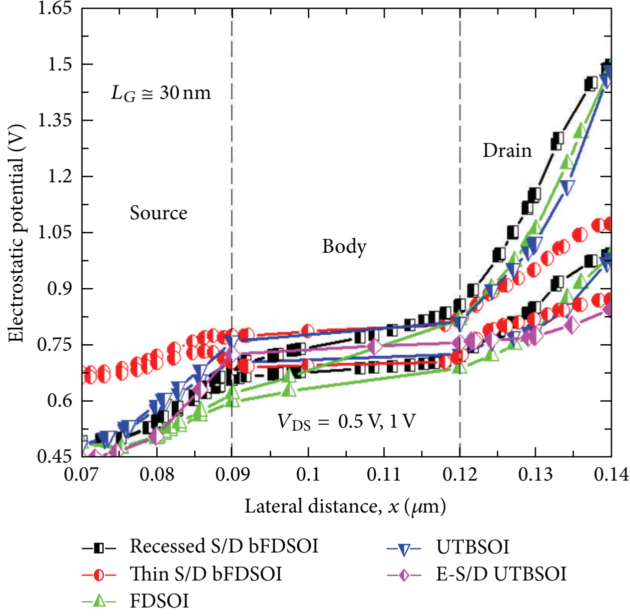

Figure 2: Simulated electrostatic potential (V) as a function of lateral distance along the FETs interface with gate length $L_G = 30$ nm.

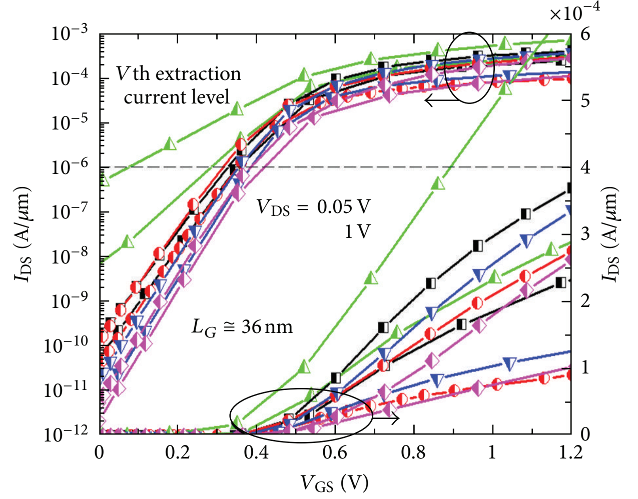

Figure 3: Comparison of bFDSOI and SOI MOSFETs I_{DS}-V_{GS} characteristics with gate length L_G = 36 nm. The symbols are the same as in Figure 2.

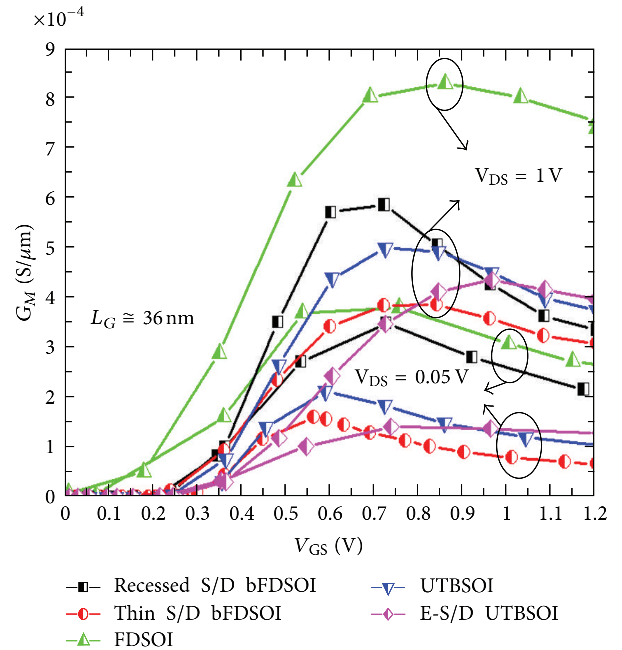

Figure 4: Comparison of bFDSOI and SOI MOSFETs G_M-V_{GS} characteristics with gate length L_G = 36 nm.

not optimized the S/D engineering in this study so that the characteristics are strongly dependent on the source/drain parasitic resistances. However, this study does predict the general trends for device scaling. Figure 3 shows the transfer characteristics of FETs with gate length L_G = 36 nm. Because of the block-oxide-enclosed Si body, bFDSOI-FETs show that DIBL is suppressed and subthreshold swing is improved. Furthermore, both thin S/D and recessed S/D bFDSOI-FETs show similar results compared to the UTBSOI-FET as well as the E-S/D UTBSOI-FET—additionally, those results are all better than those for the FDSOI-FET. In the UTBSOI-FET or E-S/D UTBSOI-FET, the subthreshold leakage current is the lowest among the transistors. Although FDSOI-FET shows the highest I_{ON} and transconductance ($G_{M,\,MAX}$ in Figure 4), it is very difficult to alleviate the SCEs in a thick body structure. For a given MOS device, transconductance is proportional to the square root of the drain-to-source current I_{DS} [19]. This suggests that thick S/D regions need to be introduced for an SOI to reduce series resistance. Yet a thick S/D structure alone cannot effectively reduce SCEs. Note that in Figure 5, the DIBL of bFDSOI-FETs is much smaller than that of the FDSOI-FET because the influence of drain bias on the channel current is reduced, as discussed earlier. Also, Figure 5 shows that as the gate length is reduced, the DIBL characteristics of the thin S/D bFDSOI-FET become slightly better than the recessed S/D bFDSOI-FET because the thin S/D structure possesses an effective method of suppressing SCEs. Nevertheless, either of the bFDSOI-FETs can alleviate the requirement of using an ultrathin channel to control SCEs in future nanodevices.

Figure 6 shows the I_{OFF} versus I_{ON} for the MOSFETs at different gate lengths. Thanks to its improved subthreshold swing, the bFDSOI-FETs show a lower I_{OFF} when compared with the FDSOI-FET. It should be noted that the FDSOI-FET shows the highest I_{ON} among transistors. As discussed earlier, thick S/D structure alone was unable to effectively reduce source and drain punch-through leakage, leading to the increase in I_{OFF}. On the one hand, UTBSOI-FET achieves the lowest I_{OFF}, mainly owing to the ultrathin S/D structure that suppresses punch-through and reduces the leakage current. This ultrathin S/D structure also allows the UTBSOI-FET to better control SCEs (see Figure 3), by reducing the effects of charge sharing. But the UTBSOI-FET has a poor I_{ON} because of the high series resistance caused by its ultrathin

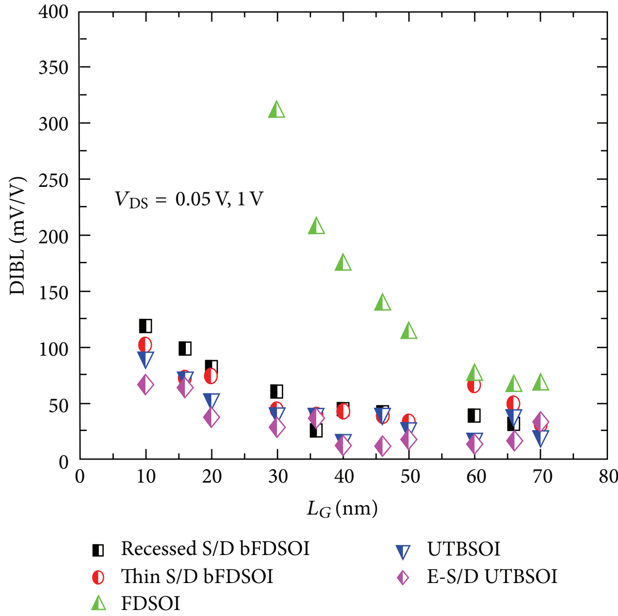

FIGURE 5: Simulated DIBL as a function of the gate length L_G for a low drain bias (V_{DS} = 0.05 V) and high drain bias (V_{DS} = 1.0 V). It is shown that the DIBL characteristics of the bFDSOI-FETs are better than those of the FDSOI-FET and similar to those of the UTBSOI-FET.

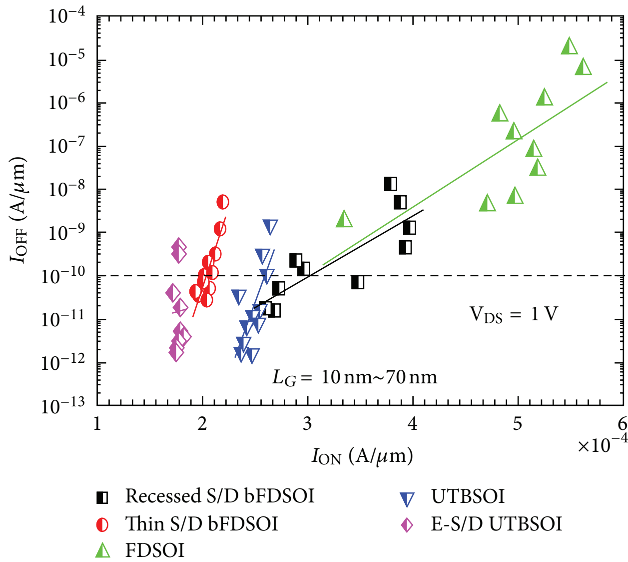

FIGURE 6: Simulated I_{OFF} versus I_{ON} for the MOSFETs at V_{DS} = 1.0 V. Mainly due to improved subthreshold swing, bFDSOI-FETs produce higher on/off current ratio than FDSOI-FET.

S/D regions. In the case of the E-S/D UTBSOI-FET, due to the nonoptimized S/D doping (because we use the same process conditions and parameters to fabricate all devices except those unique respective structures), this results in the longest channel length among all five transistors, and a poor I_{ON} is obtained. That is why the E-S/D UTBSOI-FET shows a better subthreshold swing and lower leakage current compared to

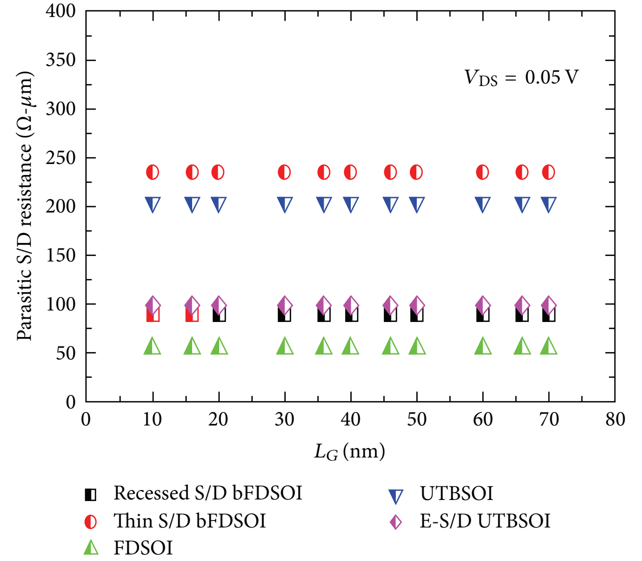

FIGURE 7: Simulated $R_{S/D}$ in different transistors for a low drain bias (V_{DS} = 0.05 V) and high gate bias (V_{GS} = 5.0 V). As shown in the figure, other than the thin S/D bFDSOI and UTSOI devices, devices show lower $R_{S/D}$ because of thick S/D regions.

the UTBSOI-FET as also shown in Figure 3 and smaller DIBL with decreasing gate length as shown in Figure 5. Therefore, the long channel leads to the small channel current and transconductance as shown in Figure 4. Both of the bFDSOI-FETs have similar results to the UTBSOI-FET. This is because the combined applications of a thick Si body and a block-oxide in a FDSOI MOSFET are used to minimize the effects of charge sharing.

Figure 7 shows the S/D series resistance ($R_{S/D}$) for the different transistors, which was extracted at V_{DS} = 0.05 V and V_{GS} = 5.0 V [20]. Compared with the thin S/D bFDSOI-FET and the UTBSOI-FET, both of the recessed S/D bFDSOI-FET and the FDSOI-FET have a very low $R_{S/D}$ because of their thick S/D regions. Furthermore, owing to the raised S/D scheme, the E-S/D UTBSOI-FET reveals a similar $R_{S/D}$ when compared to the recessed S/D bFDSOI-FET. We also consider that due to the recessed S/D scheme, the bFDSOI-FET can get a relatively lower $R_{S/D}$ than that of the E-S/D UTBSOI-FET. In other words, the junction depth that is different for both devices may be a reason why the $R_{S/D}$ of the recessed S/D bFDSOI-FET is relatively smaller. The low $R_{S/D}$ is desirable for SOI devices in high-performance applications, but ultrathin S/D regions have difficulty achieving a low $R_{S/D}$. Although the FDSOI-FET shows the lowest $R_{S/D}$ among the transistors, it is difficult to reduce DIBL and other SCEs. For the recessed S/D bFDSOI-FET, the combined applications of a thick S/D and a block-oxide are an effective way of reducing $R_{S/D}$ as well as DIBL. For the thin S/D bFDSOI-FET, it is difficult to reduce $R_{S/D}$ because of its thin S/D regions, but the thinness of these regions makes it easy to reduce DIBL. On the other hand, the E-S/D UTBSOI-FET also exhibits a smaller $R_{S/D}$ compared to the UTBSOI-FET; however, the Miller capacitance is one of the most important issues for high-frequency applications.

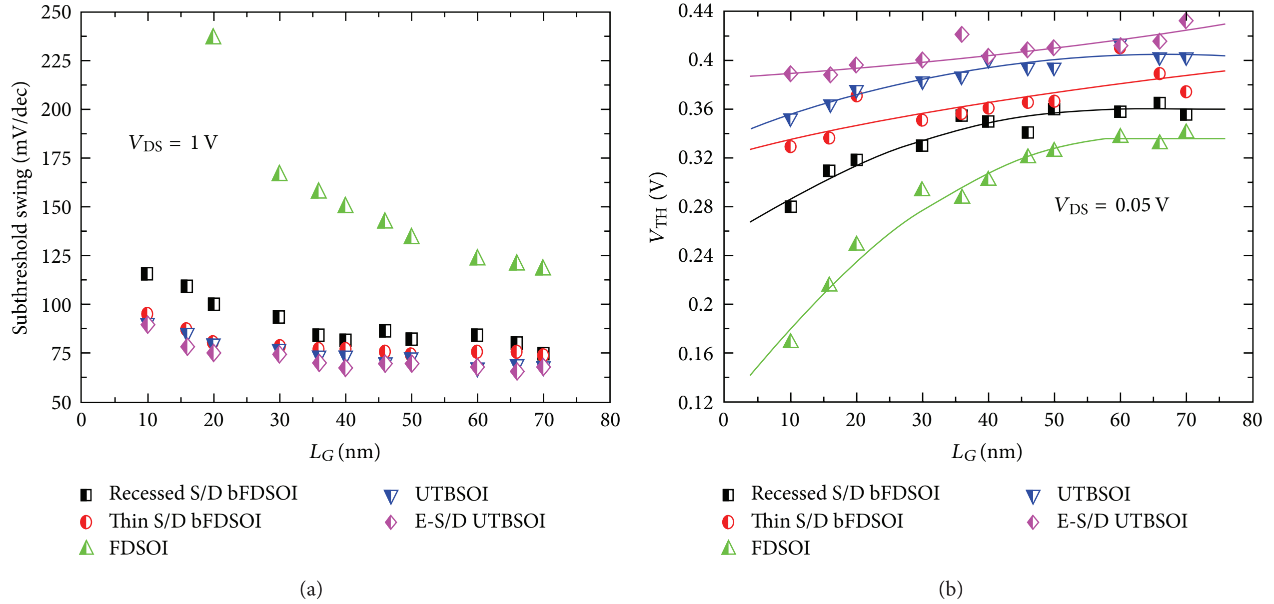

Figure 8: Simulated (a) subthreshold swing and (b) V_{TH} dependence on the gate length L_G. The bFDSOI-FETs show improved subthreshold swing and better V_{TH} rolloff than FDSOI-FET, similar to the UTBSOI-FET.

The subthreshold swing and V_{TH} of MOSFETs, as a function of the gate length, are presented in Figure 8. Because of the good gate controllability over the active channel, the bFDSOI-FET has an improved subthreshold swing and a better V_{TH} rolloff when compared with the FDSOI-FET. According to recent trends, SOI FETs limit the device performance itself since a uniform film thickness below 10 nm is needed for improving the subthreshold swing [21, 22]. In brief, SOI devices need to conform to the rule that $T_{Si} \leq L_G/4$ [23]. The use of a block-oxide in FDSOI design can alleviate the requirement for a uniform ultrathin Si film, thereby making the characteristics of the bFDSOI-FETs like those of the UTBSOI-FET with or without an E-S/D scheme, even though the total body thickness (including the single crystal Si body and the poly-Si film deposited afterward) is 35 nm in the bFDSOI-FETs.

One of the key issues associated with SOI-based transistors is self-heating effects (SHEs), because the reliability of SOI devices is severely affected by thermal instability. To investigate the influence of SHEs on the device structures, various gate-to-source overdrive voltages (V_{GT}) are applied to the devices. With V_{GT} = 1.0 V, thin S/D bFDSOI-FET still shows good behavior in suppressing SHEs. However, FDSOI, UTBSOI, and E-S/D UTBSOI devices, in contrast, suffer from serious thermal effects because the self-heating-induced negative differential conductance (NDC) is observed in the output curves, as shown in Figure 9. The authors also found that the 35 nm thick body bFDSOI structures can help transistors to endure more heat generated in the channel. Although the body of the FDSOI is thicker than that of the UTBSOI, a higher drain current also results in more heat energy and eventually leads to a reduction of the drain current I_{DS} when the FDSOI enters into the saturation region. For the recessed bFDSOI-FET, due to the higher drain

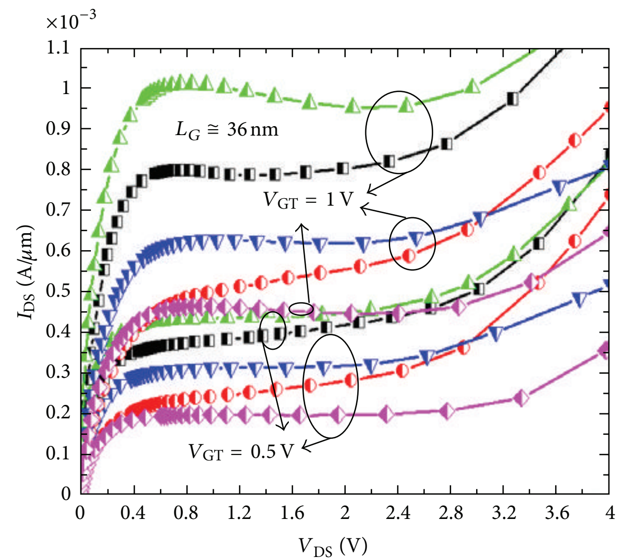

Figure 9: Comparison of bFDSOI and SOI MOSFETs I_{DS}-V_{DS} characteristics with gate length L_G = 36 nm. The symbols are the same as in Figure 2.

current compared to that of the thin S/D bFDSOI-FET, the self-heating-induced NDC is also observed in the output curves. However, the recessed S/D bFDSOI-FET still provides better self-heating immunity than SOI devices owing to its thick body scheme. Additionally, due to the lower current in the bFDSOI device than in the UTBSOI, self-heating is not dominant. If the drain current is high enough, self-heating is still a significant problem for the bFDSOI-FETs, as it is in UTBSOI devices. Nevertheless, owing to the thick body and the block-oxide schemes, requiring a uniform UTB

structure for suppression of SCEs can be excluded. This relaxes the technology requirement in a UTB application. In addition, the power supply voltage will eventually decrease in order to reduce the power consumption in the IC circuits. Therefore, the thermal instability in the bFDSOI-FETs can be diminished via a choice of low power supply (i.e., $V_{cc} < 1.0$ V).

In the case of low drain bias, self-heating is not significant; hence the NDC is not obviously observed in the output characteristics. The better control of SCEs the transistor has, the higher output resistance (r_o) the transistor possesses. That is why the UTBSOI with or without an E-S/D structure can produce a higher r_o compared to the FDSOI, with or without a block-oxide scheme. In addition, because large drain current results in large G_M, both FDSOI and recessed bFDSOI devices show a larger G_M than those of other transistors. In order to compare the incremental voltage gain ($A_V = G_M/G_D = G_M r_o$), it is believed that the UTSOI with or without E-S/D devices can produce a higher voltage gain as compared to the FDSOI with or without block-oxide scheme, despite the fact that their G_M is lower. It is because the poor short-channel behavior leads to a small r_o observed in output curves for the FDSOI with or without the block-oxide scheme. If the self-heating is dominant, it is not a fair comparison chiefly owing to the NDC phenomenon that results in negative r_o.

Figure 10 shows the electron temperature along the MOSFETs' channel surface with gate length $L_G = 36$ nm. For bFDSOI-FETs, the thermal stability can be improved with the addition of a thick body, which results in a lower electron temperature in the channel. Although an ultrathin S/D structure alone shows excellent subthreshold characteristics, SHEs will become a severe problem for SOI-based transistors in particular, as SHEs would likely block the use of SOI MOSFETs in high-performance CMOS applications. It is worthwhile noting that a high-temperature electron possessing high transportation, rotation, and vibration energy will result in the increased probability of phonon scattering and surface scattering, thereby increasing thermal resistance and aggravating self-heating. In contrast to both of these SOI-based transistors, bFDSOI-FETs can alleviate the requirement of uniform ultrathin films to control SCEs, thereby leading to high device reliability. As a result, the thermally induced vibrations of the atoms in the bFDSOI-FETs are ameliorated by its thick body. The body thickness of the FDSOI is thicker than that of the UTBSOI, but a higher I_{DS} also results in more heat energy and eventually leads to a serious reduction of the carrier mobility.

The simulation results in this paper suggest that a metal-gate material and a high-k dielectric should be introduced into the bFDSOI-FET devices. The use of a metal gate would allow the V_{TH} to be optimized even for a lightly doped ultrathin body. In addition, the metal gate, when used with a high-k dielectric, would allow the I_{ON}/I_{OFF} ratio to be improved [24, 25]. This is because the work function of the metal gate can help transistors to adjust the V_{TH} while the high-k dielectric can also relax the requirement of ultrathin gate oxide to reduce the gate-tunneling leakage current.

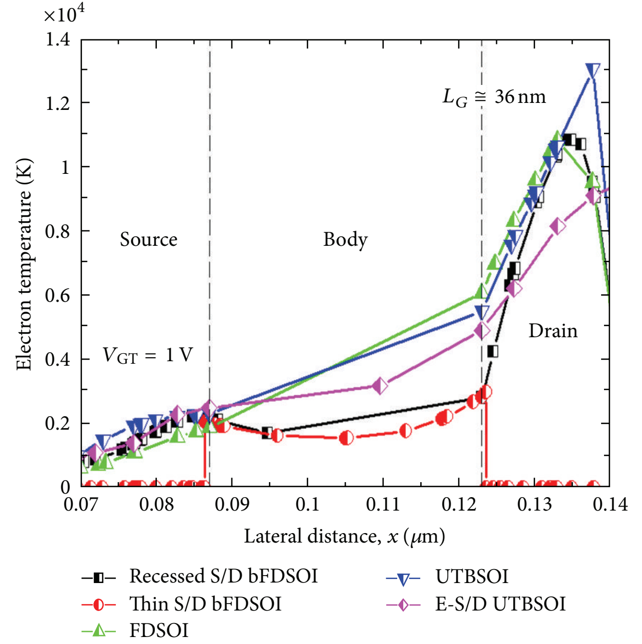

Figure 10: Simulated lateral electron temperature (K) as a function of lateral distance along the MOSFETs channel surface with gate length $L_G = 36$ nm.

Two important issues caused by the bFDSOI-FETs are addressed here: (1) the quality of poly-Si and (2) the non-self-aligned process. In the bFDSOI-FETs, the Si film used in this study for comparison is the same as that used in the FD and UTB SOI devices. The mobility of bFDSOI-FETs is actually affected by the poly-Si film. Although the lattice scattering caused by phonons in the bFDSOI-FETs can be reduced by its thick body, the poor quality of poly-Si also results in reduced mobility. Some methods of improving the quality of poly-Si are now described. In general, after making S/D regions by ion implantation, it is believed that poly-Si can be recrystallized because the poly-Si is directly connected to the single crystal Si body. Moreover, advanced recrystallization techniques can also be applied to the bFDSOI process to improve the quality of the poly-Si. Another key issue is the non-self-aligned process used in bFDSOI-FETs. In fact, self-aligned technology is not applicable in the bFDSOI-FETs presented. The misalignment problem will limit the bFDSOI-FETs' performance. All of these issues, including the quality of poly-Si channel and the self-alignment of bFDSOI-FETs, will be addressed in our future research work.

4. Conclusion

In this paper a new planar FDSOI MOSFET with block-oxide has been presented and analyzed. The bFDSOI-FET is equipped with a block-oxide on the sidewall of Si body that helps improve the control of SCEs without requiring a uniform UTBSOI structure. As indicated by the two-dimensional (2D) simulation results, the authors found that

the characteristics of the bFDSOI-FETs (a reduced DIBL, a higher on/off current ratio, an improved subthreshold swing, and a better V_{TH} rolloff behavior as compared with the FDSOI-FET) are similar to the UTBSOI-FET, because the block-oxide-enclosed Si body helps to diminish the influence of V_{DS} upon the channel current, resulting in desirable device characteristics. Although the short-channel properties of bFDSOI-FETs are somewhat worse than those of UTBSOI-FETs, the results are acceptable. Moreover, both types of bFDSOI-FETs also exhibit significantly lower channel temperature due to their thick bodies. It should be noted that this thick body, including the single crystal Si body and the poly-Si film deposited afterwards, are used to tolerate much of the heat being generated in the channel when compared with the UTBSOI-FET. As a result, the thermal stability of the bFDSOI-FETs can be improved by reducing the scattering of lattice atoms. Compared with the UTBSOI-FET, a thickness requirement of below 10 nm and uniform ultrathin film are excluded for the bFDSOI-FETs to diminish the charge-sharing effect without increasing self-heating. The bFDSOI-FETs are therefore found to improve the reliability of SOI CMOS devices and somewhat relax the critical technology requirement for potential applications.

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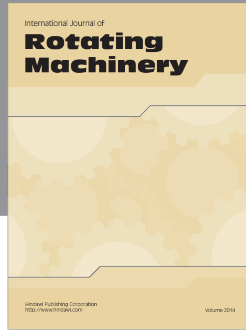
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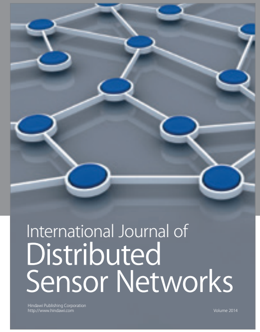
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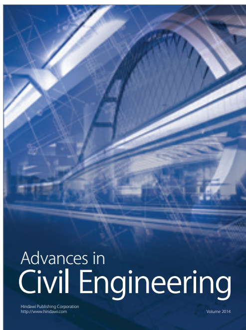
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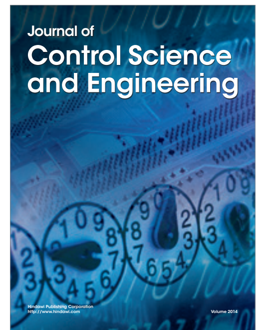
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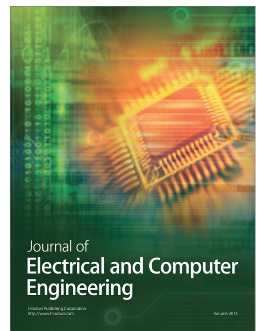
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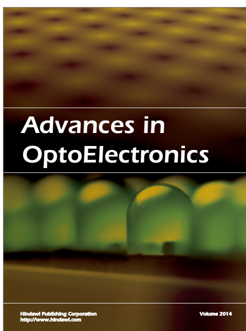
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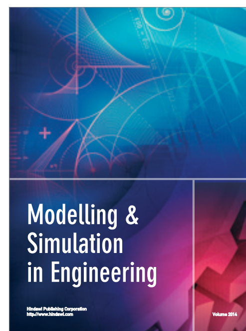
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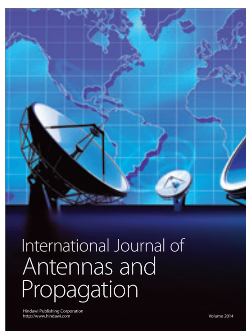
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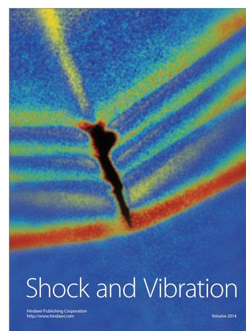
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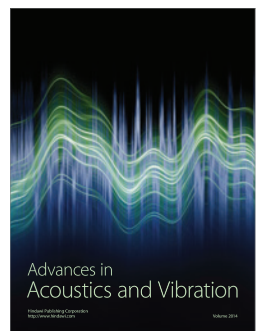
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