Hindawi Publishing Corporation
Active and Passive Electronic Components
Volume 2013, Article ID 685939, 8 pages
http://dx.doi.org/10.1155/2013/685939

Research Article

Voltage-Mode Four-Phase Sinusoidal Generator and Its Useful Extensions

Sudhanshu Maheshwari

Department of Electronics Engineering, Z. H. College of Engineering and Technology, A.M.U., Aligarh 202 002, India

Correspondence should be addressed to Sudhanshu Maheshwari; sudhanshu_maheshwari@rediffmail.com

Received 19 February 2013; Revised 15 April 2013; Accepted 15 April 2013

Academic Editor: Ali Umit Keskin

This paper introduces a new voltage-mode second-order sinusoidal generator circuit with four active elements and six passive elements, including grounded capacitors. The frequency and condition of oscillation can be independently controlled. The effect of active element's nonidealities and parasitic effects is also studied; the proposed topology is good in absorbing several parasitic elements involved with the active elements. The circuit is advantageous for generating high frequency signals which is demonstrated for 25 MHz outputs. Several circuit extensions are also given which makes the new proposal useful for real circuit adoption. The proposed theory is validated through simulation results.

1. Introduction

Four-phase sine-wave generators with voltage outputs progressively separated by 90° apart find useful applications in communication and instrumentation systems and hence have been well covered in open literature [1–4]. Some of the earlier works based on transconductance-*C* approach [1] offered compact realization with low transistor counts, but limited in frequency when compared to current conveyor based works [2]. Very novel addition to the literature witnessed compact bread-boarding solutions with scope of future integration of new active elements, like DO-CIBA [3]. Meanwhile, traditional approach of employing band-pass filter for quadrature oscillator realization, capable of generating four-phase outputs, continues to attract recent attention [4]. The four-phase voltage-mode circuit of [5] uses five opamps and five passive components, most of which are in floating form. The works as mentioned so far [1–5] falls in the category of second-order networks. Another variety of circuits employed third-order networks to generate quadrature voltage outputs, with a possibility of extension to four phases by additional active elements [6]. The active-*C* network of [6] used current controlled conveyors and three capacitors. Though the circuit in [6] was intended to generate four-phase current outputs, two quadrature voltage outputs were simultaneously available, a fact not mentioned therein. The discussion on quadrature oscillators' review is worth a voluminous work and can be restricted here, in view of a recent work [3, and cited therein]. In spite of this restriction, there are many works which find mention for their value, without belittling hundreds of other works, not mentioned herein [7–14]. For instance the work in [10] was a first attempt to use DVCC for oscillator application. Another work later [11] presented voltage-mode quadrature oscillator based on two DDCC and five grounded passive components, which can be extended for four phases by employing additional active building blocks.

This work is based on the realization of four-phase voltage-mode oscillator employing band-pass filter as reported in a recent work [15]. Although, the available work proposed a four-phase oscillator with voltage outputs, which was based on a third-order network [15], the new proposed circuit is based on a second-order network, thus providing a new unreported solution with effective results. The proposed circuit is based on four differential voltage current conveyors (DVCCs), four resistors, and two capacitors, unlike the available work, where three resistors and capacitors each were used [15]. The similarity of the new proposed circuit with available one [15] may only be deceptive, since the two works differ in order by "one," as also mentioned in the following. Circuit parasitic considerations, nonideal issues,

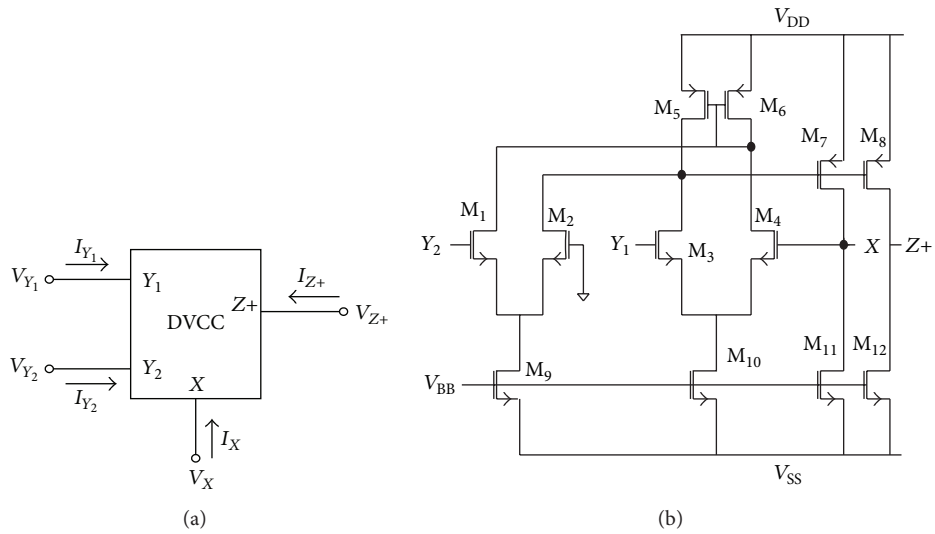

Figure 1: Differential voltage current conveyor with $Z+$ output. (a) Symbol and (b) CMOS implementation.

and circuit variations along with the workability are given to support the technical novelty of the proposal.

2. Circuit Description

The proposed voltage-mode four-phase sinusoidal generator circuit is based on DVCCs, whose symbol and circuitry are shown in Figure 1, followed by the actual oscillator circuit in Figure 2. The DVCC of Figure 1 is described by the relationship

$$I_{Y1} = I_{Y2} = 0, \qquad V_X = V_{Y1} - V_{Y2}, \qquad I_{Z+} = I_X. \tag{1}$$

It may be noted that the circuit of DVCC with only $Z+$ stage requires 12 transistors only and can be used as DDCC, by ungrounding the gate of M_2, naming it as Y_3, with the modified $V_X = V_{Y1} - V_{Y2} + V_{Y3}$, along with $I_{Y3} = 0$. The DVCC/DDCC based analog circuit design continues to be a favorable research topic till recently [4, 16–18]. The basic scheme along with the proposed circuit is shown in Figures 2 and 3, respectively. The circuit requires four active elements and six passive elements, with the advantage of both grounded capacitors. Inverting band-pass transfer function of the basic scheme of Figure 2 is realized from node Y_3 of DDCC-1 to node V_B in Figure 3. The inverting gain factor ($-k$) of Figure 2 is realized using DVCC-4 along with R_3 and R_4 in Figure 3. It may be noted that the inverting amplifier used is one of the several analog blocks as available in [15]. It may be noted that the DDCC-1 has unused Z terminal, which need not to be implemented, thus reducing the implementation of DDCC-1 by two transistors. Routine analysis of the circuit of Figure 3 (along with the block diagram of Figure 2) yields the following characteristic equation:

$$s^2 + sb(1-k) + a = 0,$$
$$\text{where, } a = \frac{4}{R_1R_2C_1C_2}, \tag{2}$$
$$b = \frac{2}{R_1C_1}, \quad k = \frac{2R_4}{R_3}.$$

The frequency of oscillation (FO) and the condition of oscillation (CO) are found from (3) as follow:

$$\text{FO} : f_o = \frac{1}{\pi\sqrt{R_1R_2C_1C_2}}, \qquad \text{CO} : 2R_4 \geq R_3. \tag{3}$$

Equation (3) can be easily interpreted for the variation of FO independent of CO, by the frequency determining passive components; whereas, the CO requires setting of separate resistors. The four-phase voltage outputs are related as follows:

$$V_A = -\frac{sR_1C_1}{2}V_B, \qquad V_B = -\frac{sR_2C_2}{2}V_C, \qquad V_D = -V_B. \tag{4}$$

At the frequency of oscillation, the previous equation can be expressed as follows:

$$V_A = -j\frac{\omega_o R_1C_1}{2}V_B, \qquad V_B = -j\frac{\omega_o R_2C_2}{2}V_C, \qquad V_D = -V_B. \tag{5}$$

For a design with equal resistors ($R_1 = R_2 = R$) and equal capacitors ($C_1 = C_2 = C$), the angular frequency of oscillation is obtained from (3) as $\omega_o = 2/\text{RC}$; then (5) reduces to

$$V_A = -jV_B, \qquad V_B = -jV_C, \qquad V_D = -V_B. \tag{6}$$

Equation (6) shows equal amplitudes for the four outputs, which are separated in phase progressively by 90°.

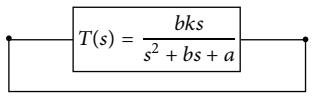

Figure 2: Basic scheme of oscillator realization.

3. Parasitic Considerations

The circuit of Figure 3 is next analyzed for the involvement of DVCC parasitic elements. It is a well-known fact that the parasitic effects are circuit-topology dependent. A current conveyor circuit with resistive X terminations is suited for absorbing the X terminal intrinsic resistance (R_X), although the net value does increase by R_X. Similarly, a current conveyor-based network with capacitive terminations at Y and/or Z terminals is good from the point of absorption of parasitic capacitance at these terminals (C_Y and/or C_Z, resp.), though the net value at those nodes does increase. Resistive terminations at Z terminal with moderate design values (few KΩ's) also does not hinder the circuit behavior much from the ideal, as the parasitic resistance at Z (R_Z) is relatively much higher than the externally connected resistor, appearing in shunt. Coming to the circuit of Figure 3, it may be noted that the various external passive elements are modified due to the parasitics as follows:

$$C_1' = C_1 + C_Z + 3C_Y, \qquad C_2' = C_2 + C_Z + 2C_Y,$$
$$R_I' = R_I + R_X, \quad I = 1, 2, 3, \tag{7}$$
$$R_4' = R_4 // R_P, \qquad R_P = \left(\frac{R_Y}{2}\right) // R_Z.$$

The nonideal FO and CO are thus found as follows:

$$\text{FO} : f_o' = \frac{1}{\pi\sqrt{R_1' R_2' C_1' C_2'}}, \qquad \text{CO} : 2R_4' \geq R_3'. \tag{8}$$

Equations (7)-(8) suggest that the actual FO would be slightly smaller than the desired FO, but the circuit topology does provide the designer scope of nullifying the parasitic effects, by predistorting the passive components. The actual errors as a result of parasitic elements would be given in the results' section.

4. Nonideal Transfer Gain Effects

A nonideal DVCC is characterized by the following relationship:

$$V_X = \beta_1 V_{Y1} - \beta_2 V_{Y2}, \qquad I_{Y1} = I_{Y2} = 0, \qquad I_{z+} = \alpha I_x. \tag{9}$$

Here, the voltage transfer gains from Y_i, $i = 1, 2$, to X terminal is denoted by β_i, and current transfer gain form X terminal to $Z+$ terminal is α. The proposed circuit's topology (Figure 3) is such it nullifies the transfer gain effect from Y_1 to X, thus easing the nonideal expression rid of β_1. An analysis of the circuit using the nonideal description yields the oscillator's characteristic equation as follows:

$$s^2 + s\frac{(1+\alpha)\beta^2}{R_1 C_1}\left[1 - (1+\alpha)\beta\frac{R_4}{R_3}\right] + \frac{(1+\alpha)^2\beta^3}{R_1 R_2 C_1 C_2} = 0. \tag{10}$$

It may be noted that the β_2 for different DVCCs is taken identical to simplicity of the expression, thus dropping the suffix. The nonideal FO and CO in light of the previous equation thus become

$$\text{FO} : f_o = \frac{(1+\alpha)\sqrt{\beta^3}}{2\pi\sqrt{R_1 R_2 C_1 C_2}}, \qquad \text{CO} : (1+\alpha)\beta R_4 \geq R_3. \tag{11}$$

Equation (11) needs to be first interpreted in terms of frequency errors, as the numerator would be slightly smaller than the ideal expression (3), thus causing a decrement in the actual frequency of oscillation in comparison to the designed value. A similar effect was found in previous section after incorporation of parasitic elements. Thus it is to be appreciated that the FO would be slightly smaller than the desired value, to be further commented upon in results' section. Secondly, (11) has been derived with the assumption that the transfer gains for various DVCCs would be identical, which is quite practical, especially for integrated realizations. Now, the appearance of β with power 3/2 may be quite annoying from sensitivity perspective, but actually it is equal to three different β_2s for different conveyors. With this clarification, the sensitivity of FO with respect to all active and passive elements is found to be within unity in magnitude, ensuring good performance.

5. Verification Results

The four-phase oscillator of Figure 3 was simulated using the DVCC of Figure 1 using PSPICE tool. The parameters' details are listed in many recent works, hence not repeated here [14, 15]. The circuit was designed with capacitive elements of 10 pF and frequency determining resistors ($R_1 = R_2$) as 3 KΩ, thereby yielding a theoretical frequency of oscillation as 10.6 MHz from (3). The CO was adjusted through setting R_3 in the vicinity of 4 KΩ, retaining $R_4 = 2$ KΩ. The output waveforms are shown in Figure 4, where the FO is found as 10.25 MHz, resulting in an error in FO of approximately 3%. The spectrum of the four outputs is shown in Figure 5; the THD is found to be around 1.1%. The proposed circuit provides interesting options for tunability through either R_1 and/or R_2 without restriction on their ratios or involvement in CO, a preferred method exhibited in most of the related literatures on the subject. However, the circuit topology used [15] has a scope of being used as a potential analog cell for field programmable analog arrays, where programmable capacitor arrays are employed. In such applications, an array of equal capacitors is available, which need to be switched so as to vary a circuit parameter. With this view, the tunability of the proposed oscillator is studied by using capacitive elements of values 8 pF, 6 pF, and 4 pF so as to result in FO as 12.5 MHz,

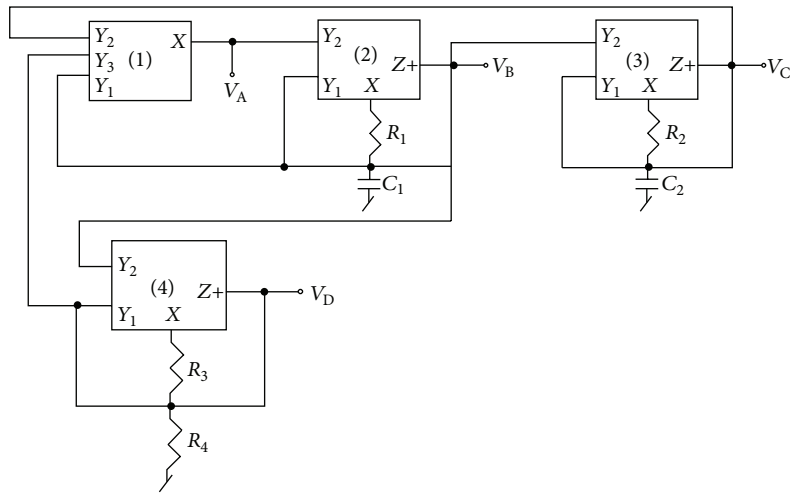

Figure 3: Proposed four-phase oscillator circuit.

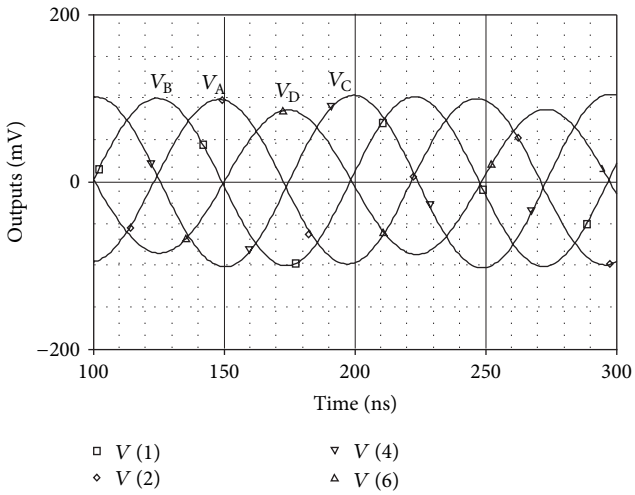

Figure 4: Voltage outputs of the proposed circuit.

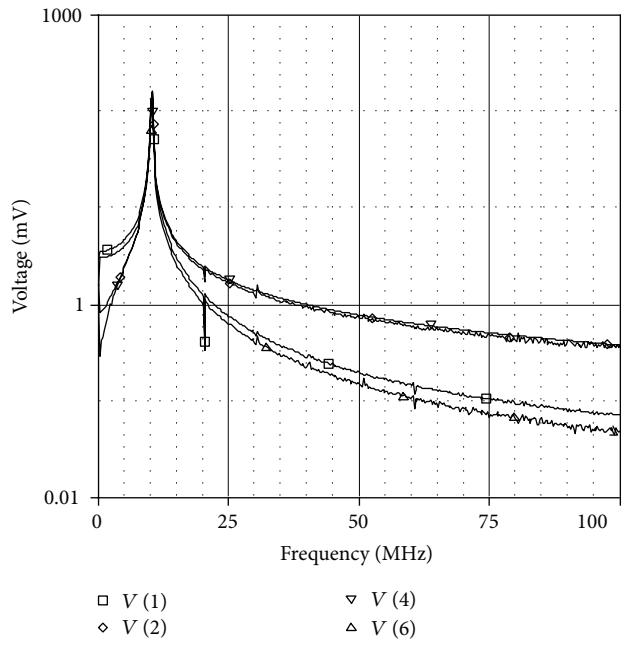

Figure 5: Fourier spectrum of outputs with FO = 10.25 MHz.

17.5 MHz, and 25 MHz, respectively. The spectrum of the output waveforms is shown in Figure 6, which confirms the practical utility of the proposed circuit.

6. Circuit Extensions

This section presents some useful circuit extensions by simple modifications to the proposed circuit of Figure 3. Several variations with distinct features are given as useful future adoptions.

6.1. Eight Outputs' Circuit. The voltage-mode four-phase oscillator of Figure 3 can be extended for explicit four-phase current outputs by employing Z-stages. Additional $Z+$ and $Z-$ stages incorporation in DVCC-2 and DVCC-3 each result in four current outputs spaced progressively 90 degrees apart. With this modification (addition), the circuit can be used as a complete four-phase oscillator with both voltage as well as current outputs. The resulting circuit is unique in light of the available literature, by simultaneously generating eight outputs in all. The previously referred circuit (with eight outputs capability) is also simulated to support the theory. Additional $Z+$ and $Z-$ stages each in DVCC-2 and DVCC-3 are implemented so as to result in four-phase current outputs. For the presentation of results, the $Z-$ stages are incorporated in the above-mentioned conveyors so as to generate the quadrature current outputs as shown in Figure 7, with the same design as given earlier for voltage outputs. The Fourier spectrum is next shown in Figure 8, with the FO as 10.25 MHz. It may again be noted that two additional outputs (phase inverted with respect to the ones shown in Figure 7) would be available at $Z+$ terminals of the conveyors.

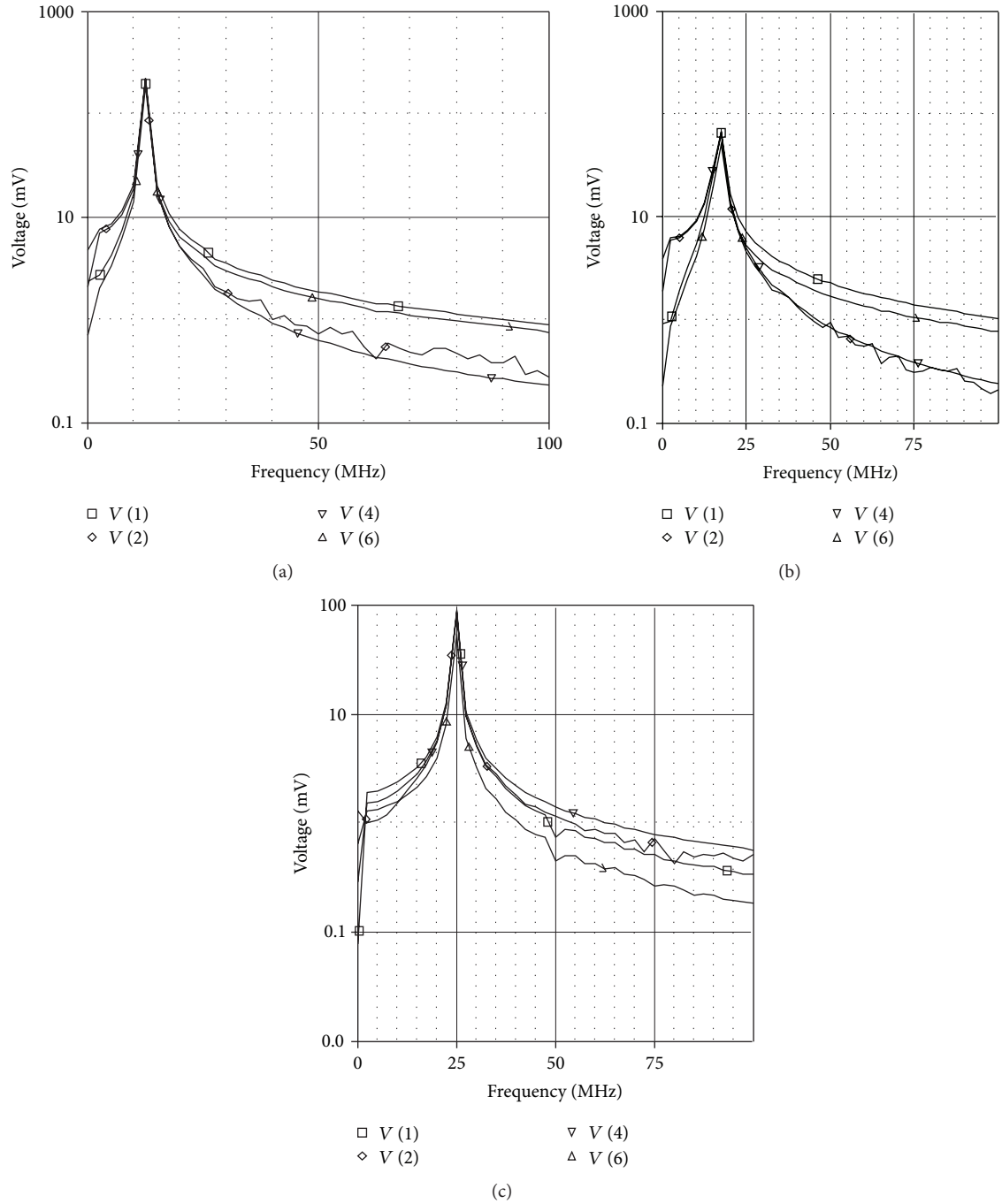

Figure 6: Fourier spectrum for different "C." (a) $C = 8$ pF, FO = 12.5 MHz; (b) $C = 6$ pF, FO = 17.5 MHz; (c) $C = 4$ pF, FO = 25 MHz.

6.2. Circuit with Simpler Configuration. Circuit with simpler configuration can be obtained by leaving the Z terminal unused while retaining the circuit's functionality. This modification results in an FO half of what is obtained for Figure 3, and the CO reduces to $R_4 \geq R_3$. The resulting circuit is simpler in the sense that Z stages need not to be implemented (please note that current outputs as mentioned in following section will not be available here). More importantly, the parasitic capacitance C_z in (7) disappears as a result of this modification, enabling reduction in errors in FO, for a given capacitor (C_1, C_2) based design as compared to the circuit of Figure 3. This also provides a design guideline to use smaller capacitance-based design for a permissible FO error. On the other hand, in order to obtain the same FO range as in circuit of Figure 3, the modified circuit would necessitate smaller resistance values, which makes "R_x" induced error more influential, when compared to the circuit of Figure 3. Such discussions often lead to unending arguments, best

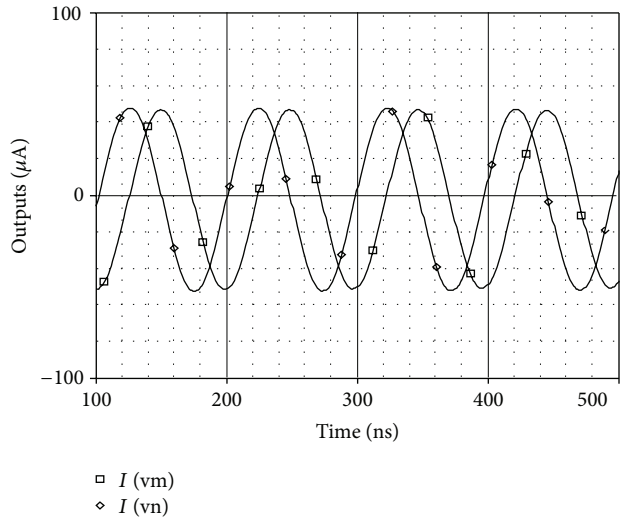

Figure 7: Quadrature current outputs for extended circuit.

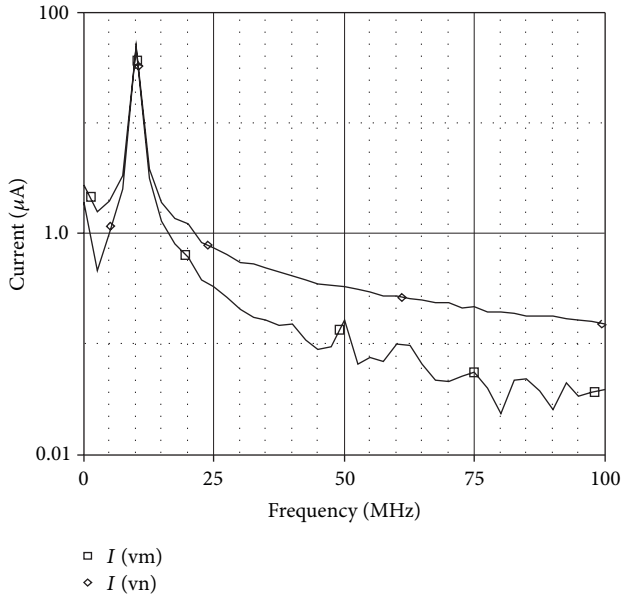

Figure 8: Fourier spectrum of the current outputs with FO = 10.25 MHz.

attributed to the artistic mysteries of analog circuit design. Notwithstanding, newer topologies are actually synthesized, as a result of such discussions.

6.3. Circuits with Tunable DVCCs. Another circuit enhancement is the use of voltage controlled DVCC as was introduced in [19]. In such case, the X-terminated resistors are eliminated, and instead the intrinsic X terminal resistance becomes effective, which is tunable through the bias voltage as has been shown in [19]. Though limited tenability is achieved, the circuit does become a voltage controlled oscillator. Alternatively, current controlled DVCCs can be employed in place of conventional DVCCs. The X terminal resistors are again replaced by intrinsic resistance. The circuit's frequency of oscillation can then be tuned through the bias currents. However, the relative complexity involved will almost double, as the CC-DVCC is a combination of CCCII and DVCC, as has been very well demonstrated in some useful novel works [20, 21].

6.4. Use of Current Gain Variable DVCC. Very interesting circuit advancement can be obtained by employing current gain variable DVCCs. It may be noted that conventional DVCC has unity current transfer gain from X to Z terminal. This may be varied to obtain a current-gain variable DVCC. The concept of current-gain variable current conveyors has its origin from some earlier works [22–25]. The proposed circuit of Figure 3 is a promising candidate for the purpose, as is evident from the nonideal expressions (10)-(11). These suggest that the oscillator's frequency and condition are a function of current transfer gain "α." If α is made variable, then the FO can be tuned through it, rather than the external passive elements. A simple way to achieve this is to vary the aspect ratio of transistors comprising the Z stage as was also given in [14], but for amplitude control in that particular work. A more practical way is to tune the current gain and hence the frequency of the oscillator by digital means as given in the following.

6.5. Digitally Controlled Circuit. A last future enhancement is the use of a digitally controlled current transfer gain stage, which has been recently employed in some work [26, and cited therein]. The current transfer gain "α" can be digitally controlled through an n-bit control work so as to vary the frequency of the oscillator. In such an oscillator, none of the external passive elements need to be varied for frequency tuning. The complete circuit digital control and analog can thus be made compatible to standard IC technologies. Further details of the above-mentioned circuit extensions are not to be further elaborated for brevity reasons.

7. Some Interesting Remarks

The topic of this paper assumes significance in light of some interesting works which continue to appear till recently in the open literature [27, 28]. As far as the quadrature oscillator's (with two quadrature outputs) extension to four outputs is concerned, additional inverters can be employed in such cases. A DVCC with input voltage at Y_2 and the output at X (with rest unused terminals) can perform the function of an inverter. The X terminal resistance (R_x) along with output capacitance (C_x) by way of forming a low-pass filter (lossy integrator) results in finite (although) high pole frequency, thus in a way limiting high frequency operation with poorer THD, as compared to the proposed circuit, where lossless integrators provide infinite pole frequency. Thus the distortions at high frequency would not be as much in the proposed circuit as in a quadrature oscillator with inverters to generate four signals. This justifies the use of the proposed structure, as compared to the one with additional inverters. Coming to the possible application of quadrature oscillators, their utility in quadrature mixers, single sideband generation vector voltmeters, and so forth have often been highlighted

in literature. The circuits with quadrature outputs along with their inverted versions (four phases) are of special interest as two floating output sources of quadrature signals. In such an application, the circuit can also be referred to as a differential output quadrature oscillator. Other possible applications of four-phase quadrature signals can be in quadrature phase shift keying, as well. Besides, when four quadrature signals are passed through comparators, they become a source of four-phase clock generators. In nutshell, the proposed circuit and their extensions presented in the preceding section cover useful application areas.

8. Conclusion

The paper deals with a new proposal for voltage-mode four-phase oscillator circuit with independent control of FO as well as CO and use of grounded capacitors and a circuit topology suited to minimizing the parasitic effects and applicability to high frequency. Nonideal and parasitic study is also given. Some useful circuit extensions for a simpler topology, for simultaneous four-phase current outputs, voltage/current tunable oscillator, and digitally controlled circuit are also given. The new proposals are enrichment to the available knowledge on the subject.

Acknowledgment

The author is thankful to the anonymous reviewers for positive feedback on the paper. The author also thanks Professor Ali Umit Keskin, Academic Editor, for recommending the paper.

References

[1] I. A. Khan and S. Khwaja, "An integrable gm-C quadrature oscillator," *International Journal of Electronics*, vol. 87, no. 11, pp. 1353–1357, 2000.

[2] P. Beg, I. A. Khan, and M. T. Ahmed, "Tunable four phase voltage mode quadrature oscillator using two CMOS MOCCIIs," in *Proceedings of the International Multimedia, Signal Processing and Communication Technologies (IMPACT '09)*, pp. 155–157, Aligarh, India, March 2009.

[3] V. Biolková, J. Bajer, and D. Biolek, "Four-phase oscillators employing two active elements," *Radioengineering*, vol. 20, no. 1, pp. 334–339, 2011.

[4] S. Maheshwari, J. Mohan, and D. S. Chauhan, "High input impedance voltage-mode universal filter and quadrature oscillator," *Journal of Circuits, Systems and Computers*, vol. 19, no. 7, pp. 1597–1607, 2010.

[5] T. Parveen, I. A. Khan, and M. T. Ahmad, "Realization of four phase sinusoidal quadrature oscillator using operational amplifier," *Journal of Active and Passive Electronic Devices*, vol. 2, pp. 171–176, 2007.

[6] S. Maheshwari and I. A. Khan, "Current controlled third order quadrature oscillator," *IEE Proceedings—Circuits, Devices and Systems*, vol. 152, no. 6, pp. 605–607, 2005.

[7] A. M. Soliman, "Simple sinusoidal RC oscillators using current conveyors," *International Journal of Electronics*, vol. 42, pp. 61–77, 1975.

[8] A. M. Soliman, "Two integrator loop quadrature oscillators: a review," *Journal of Advanced Research*, vol. 4, no. 1, pp. 1–11, 2013.

[9] R. Senani, "New canonic single-resistance-controlled sinusoidal oscillator using a single current conveyor," *Electronics Letters*, vol. 15, no. 18, pp. 568–569, 1979.

[10] S. S. Gupta and R. Senani, "Grounded-capacitor current-mode SRCO: novel application of DVCCC," *Electronics Letters*, vol. 36, no. 3, pp. 195–196, 2000.

[11] M. Kumngern and K. Dejhan, "DDCC-based quadrature oscillator with grounded capacitors and resistors," *Active and Passive Electronic Components*, vol. 2009, Article ID 987304, 4 pages, 2009.

[12] D. Biolek, A. Ü. Keskin, and V. Biolkova, "Quadrature oscillator using CDTA-based integrators," *WSEAS Transactions on Electronics*, vol. 3, no. 9, pp. 463–469, 2006.

[13] J. W. Horng, C. L. Hou, C. M. Chang, Y. T. Lin, I. C. Shiu, and W. Y. Chiu, "First-order allpass filter and sinusoidal oscillators using DDCCs," *International Journal of Electronics*, vol. 93, no. 7, pp. 457–466, 2006.

[14] S. Maheshwari and B. Chaturvedi, "High output impedance CMQOs using DVCCs and grounded components," *International Journal of Circuit Theory and Applications*, vol. 39, no. 4, pp. 427–435, 2011.

[15] S. Maheshwari, "Analogue signal processing applications using a new circuit topology," *IET Circuits, Devices and Systems*, vol. 3, no. 3, pp. 106–115, 2009.

[16] H. O. Elwan and A. M. Soliman, "Novel CMOS differential voltage current conveyor and tits applications," *IEE Circuits Devices Systems*, vol. 144, pp. 856–860, 1997.

[17] W. Chiu, S. I. Liu, H. W. Tsao, and J. J. Chen, "CMOS differential current conveyors and their applications," *IEE Circuits Devices Systems*, vol. 143, pp. 91–96, 1996.

[18] K. Pal, "Modified current conveyors and their applications," *Microelectronics Journal*, vol. 20, no. 4, pp. 37–40, 1989.

[19] S. Maheshwari, "A canonical voltage-controlled VM-APS with grounded capacitor," *Circuits, Systems, and Signal Processing*, vol. 27, no. 1, pp. 123–132, 2008.

[20] P. Prommee, M. Somdunyakanok, and S. Toomsawasdi, "CMOS-based current-controlled DDCC and its applications," in *Proceedings of the IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems (ISCAS '10)*, pp. 1045–1048, June 2010.

[21] P. Prommee and M. Somdunyakanok, "CMOS-based current-controlled DDCC and its applications to capacitance multiplier and universal filter," *AEU—International Journal of Electronics and Communications*, vol. 65, no. 1, pp. 1–8, 2011.

[22] C. A. Papazoglou and C. A. Karybakas, "Non interactive electronically tunable CCII-based current mode biquadratic filters," *IEE Circuits Devices Systems*, vol. 144, pp. 178–184, 1997.

[23] C. A. Karybakas and C. A. Papazoglou, "Low-sensitive CCII-based biquadratic filters offering electronic frequency shifting," *IEEE Transactions on Circuits and Systems II*, vol. 46, no. 5, pp. 527–539, 1999.

[24] W. Surakampontorn and P. Thitimajshima, "Integrable electronically tunable current conveyors," *IEE Proceedings, Part G*, vol. 135, no. 2, pp. 71–77, 1988.

[25] W. Surakampontorn and K. Kumwachara, "CMOS-based electronically tunable current conveyor," *Electronics Letters*, vol. 28, no. 14, pp. 1316–1317, 1992.

[26] I. A. Khan and M. T. Simsim, "A novel impedance multiplier using low voltage digitally controlled CCII," in *Proceedings of*

the IEEE GCC Conference and Exhibition (GCC '11), pp. 331–334, Dubai, UAE, February 2011.

[27] A. M. Soliman, "Transformation of oscillators using Op Amps, unity gain cells and CFOA," *Analog Integrated Circuits and Signal Processing*, vol. 65, no. 1, pp. 105–114, 2010.

[28] S. Maheshwari and R. Verma, "Electronically tunable sinusoidal oscillator circuit," *Active and Passive Electronic Components*, vol. 2012, Article ID 719376, 6 pages, 2012.