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Research Article

Modeling of the Channel Thickness Influence on Electrical Characteristics and Series Resistance in Gate-Recessed Nanoscale SOI MOSFETs

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Ultrathin body (UTB) and nanoscale body (NSB) SOI-MOSFET devices, sharing a similar W/L but with a channel thickness of 46 nm and lower than 5 nm, respectively, were fabricated using a selective "gate-recessed" process on the same silicon wafer. Their current-voltage characteristics measured at room temperature were found to be surprisingly different by several orders of magnitude. We analyzed this result by considering the severe mobility degradation and the influence of a huge series resistance and found that the last one seems more coherent. Then the electrical characteristics of the NSB can be analytically derived by integrating a gate voltage-dependent drain source series resistance. In this paper, the influence of the channel thickness on the series resistance is reported for the first time. This influence is integrated to the analytical model in order to describe the trends of the saturation current with the channel thickness. This modeling approach may be useful to interpret anomalous electrical behavior of other nanodevices in which series resistance and/or mobility degradation is of a great concern.

1. Introduction

Nanoscale silicon-on-insulator (SOI) *metal-oxide-semiconductor field-effect transistor (MOSFET)* based devices are the building blocks of up-to-date systems allowing ultrafast data processing. This is in accordance with efforts to develop new generation of ultra-fast computers based on combined electronic and signal processing on one hand [1] and advanced generations of nanoscale devices (NSB) for communication systems [2, 3] on the other hand. In this paper, we report the influence of the silicon channel thickness on the electrical characteristics of SOI MOSFET NSB, and we present an accurate model permitting to evaluate the series resistance and the saturation current as a function of the thickness or of the gate voltage, when part of the aim is to explain the anomalous transport behavior of the thinner channels having a channel's thickness as low as 1.6 nm and obtained by a selective gate-recessed process [4].

The excellent control of the short channel effects, achievable by means of UTB SOI MOSFET architectures, makes them good candidates for ultimate nanometrics scale. Consequently, the transport properties' study of thin semiconductor films has attracted considerable attention in the recent years.

In this paper, we present the influence of the NSB's channel thickness on the series resistance in order to complete the unified model of the NSB's electrical characteristics. In addition to last years' existing knowledge in series resistance, these novel interpretative approach and analytical model can be useful for the prediction of transport phenomena at the nanoscale and the correction of electrical characteristics.

2. Methodology

2.1. SIMOX Preferred Wafer Processing Technology. Several techniques were developed in the past to create silicon-on-insulator (SOI) devices [5–8], since their implementation was found promising [9–11] for ULSI [12], low power [13], military and space [14], and cost reducing [15] applications. Nowadays, SOI wafers are mainly fabricated using the UNIBOND

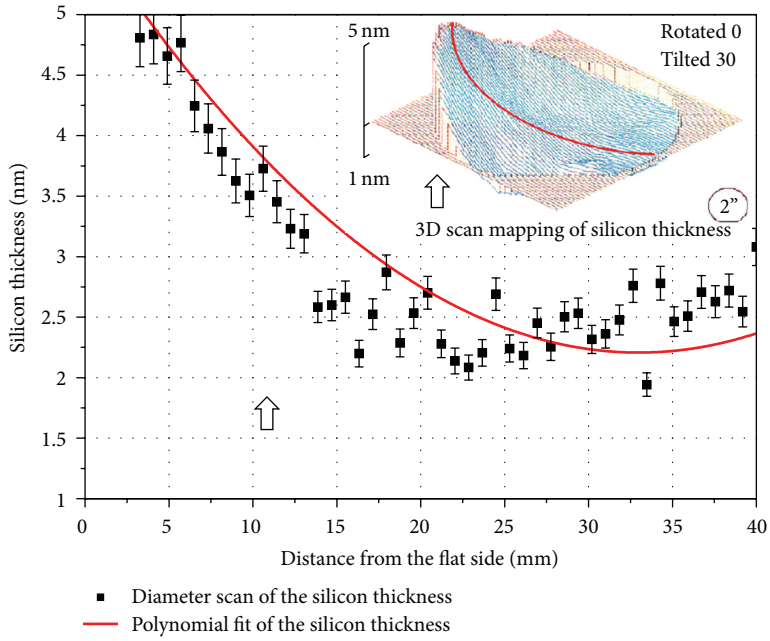


Figure 1: Gradient of SOI thicknesses measured by spectrophotometry across a 2″ diameter SIMOX test wafer after thinning using the gate-recessed process. The fitting curve here is serving as a visual guide of the thickness distribution.

line of SOI wafers and the smart cut process technologies, patented by SOITEC Company, allowing excellent thickness uniformity [16]. However, for this research purpose, the former SOITEC technology called Separation-by-IMplanted-Oxygen (SIMOX) was preferred because of the clear advantage of presenting an initial gradient of the SOI thickness across the same wafer. This desirable gradient is conserved during the processing of the nanoscale body (NSB) devices as shown in Figure 1, in which are presented spectrophotometry measurements of SOI thicknesses gradient across a 2″ diameter SIMOX test wafer after thinning using the gate-recessed process. Consequently, it is possible to study the thickness influence on the NSB electrical characteristics. In Figure 2, the tested NSB devices are presented with their respective channel thicknesses ranging from 1.6 to 4.6 nm as measured by spectrophotometry. The accuracy of the critical channel thickness of 1.6 nm was confirmed by in ex situ HRTEM measurement.

2.2. Accurate Calibration of the Oxidation Furnace. The most challenging step was the accurate controlled thinning process of the SOI layer using local oxidation in the sub 10 nm range of thickness, while the source and the drain regions remained in their original thickness. In order to check the capability of accurate thinning, preliminary tests of thinning were performed in order to reach thicknesses lower than 10 nm, when characterizing the furnace parameters like furnace temperature, duration of the oxidation, and growth rate [17].

2.3. Device Processing Using Recessed-Gate Channel Technology. The local oxidation was performed by using a nitride mask layer of 38 nm (nitride 1) grown on a thin oxide layer

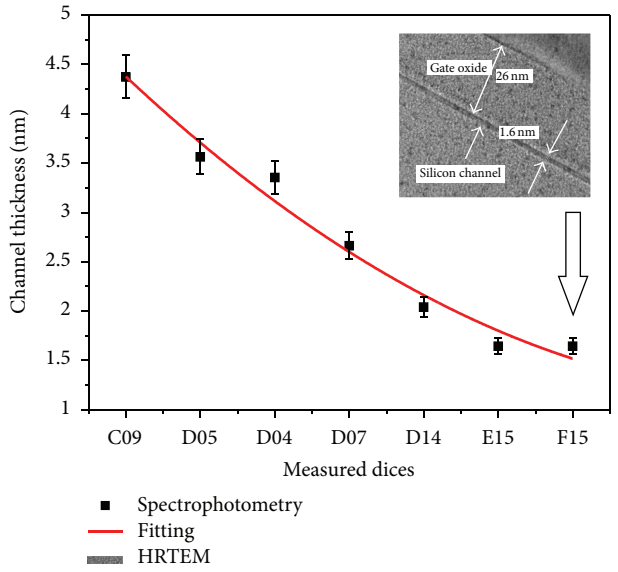


Figure 2: Spectrophotometry measurements of the channel thickness performed on the tested dices containing Nano-Scale Body (NSB) devices (from 4.4 to 1.6 nm). The dices were cut from the same 2″ diameter SIMOX wafer. The accuracy of the measurements is confirmed by inserted HRTEM picture for the smallest channel thickness value (1.6 nm). The fitting is serving as a visual guide of the thickness distribution.

(PAD OX) of 15 nm. The role of the pad oxide was to serve as an interface between the nitride and the silicon to prevent mechanical stresses. A first etching of the nitride and pad oxide layer at the extremities of the active region allowed their oxidation into a 700 nm thick field oxide (FOX). A second

etching, performed at the center of the nitride region, allowed exposure of the channel region, while the surrounding nitride capped the source and drain areas. Two steps of oxidation were then performed. First, a 75 nm thick sacrificial oxide layer, called channel oxide (CHAN OX), was grown in order to significantly decrease the channel's thickness to about 10 nm, before removal. The second phase of the oxidation (25 nm thick), called gate oxidation (GOX), was a more accurate step making possible a final nanoscale thickness of the channel, in the range of 1.6 nm to 6.5 nm, and serving as the gate oxide itself, when the thickness distribution uniformity and the Si-SiO_2 interface quality [18] are serving as important parameters [19, 20]. In order to get reference devices, that is, having an initial silicon channel close to 46 nm, the nitride mask was not etched, so the gate insulator layer is made of the 38 nm thick nitride layer deposited on the 15 nm PAD OX layer.

2.4. Fabrication of the Contact Electrodes. Then, a polycrystalline silicon layer of 220 nm was deposited over the gate oxide, oxidized, and patterned to form the gate electrode. Before the source/drain/gate phosphorus implant, a thin layer nitride (nitride 2) of 30 nm was deposited in order to prevent further oxidation of the thin silicon layer during the implant's thermal annealing. A Plasma-enhanced chemical vapor deposition (PECVD) oxide (silox 2) of 350 nm thickness was deposited followed by an aluminum metallization step to define the contact areas.

2.5. TCAD Simulation of the Device Processing. In order to perform a deeper and accurate analysis of the process limitations, the layers deposition process was translated to a model of the device using TCAD (TSUPREM-4) software. One of the main outputs of the program is the 2D device cross-section, which includes among others the exact boundaries of the various layers of materials in the structure.

In Figure 3, we present a cross-section of the NSB including the source, gate, and drain (resp., S, G, and D) parts and a zoom of the gate-recessed silicon channel. As presented in the upper insert, the active region (source, gate, and drain terminals) which is built of layers described previously, is terminated by aluminum contacts (layer 10) in the vertical axis and limited by field oxide (layer 07) borders in the horizontal axis. The buried oxide (layer 02) is serving as a barrier between the bulk silicon (layer 01) and the gate-recessed silicon channel (layer 03).

The lower insert of Figure 3 represents a zoom-in of the gate-recessed channel, when the silicon layer was thinned from 46 nm to 1.6 nm minimal thickness, as confirmed by HRTEM picture in Figure 2. This points out the advantage of the recessed process in which only the silicon channel is thinned, while the source and the drain extensions remain in their original thickness. So the series resistance of the drain and of the source should not be affected *a priori* by the thinning process.

In addition to Figure 3, presenting a simulated TCAD cross-view of the device layers, a complementary list of the process parameters was presented in summarizing Table 1.

3. Results

3.1. I_{DS}-V_{GS} Characteristics in the Linear Domain. Using the semiconductor characterization system (SCS-4200) from Keithley Ltd., *I-V* measurements (room temperature, dark conditions) were performed on a selection of four NSB devices (E15, G15, C12, and C03), having the same channel width and length ($W/L = 80\,\mu m/8\,\mu m$) but a channel thickness (t_{SI}) below 5 nm: 1.6, 2.4, 2.9, and 4.9 nm, respectively. Since the front gate oxide (GOX) thickness is 26 nm, as checked by HRTEM and ellipsometry, the front gate capacitance (C_{ox}) is evaluated to 138 nF/cm^2. Back gate contact was kept floating for all devices. The drain currents (I_{DS}) versus gate voltage (V_{GS}) characteristics (from −4 to +4 V) were measured in the linear domain (constant low $V_{DS} = 0.1$ V) and are presented in Figure 4 for the four NSBs.

By increasing V_{GS} from −4 V to −1 V, I_{DS} slowly decreases and slightly depends on t_{SI}, indicating a leakage phenomenon (negative resistance) similar to the gate-induced drain leakage (GIDL) observed for both classic and SOI-MOSFET devices [21].

For V_{GS} from −1 V to −0.5 V, the steep linear increasing observed at least for $t_{SI} = 4.9$ nm, which is combined to the low order of magnitude, characteristic of the subthreshold regime. We note that the subthreshold slope is strongly degraded by decreasing the channel thickness.

However, for positive V_{GS} values, above the apparent threshold voltage located around −0.5 V, the characteristics are bent and turned into a linear dependence on V_{GS} indicating a constant transconductance g_m in the whole positive domain of V_{GS}. Since our devices are considered as long channel devices ($L = 8\,\mu m$), the effective mobility (μ_{eff}) can be extracted from g_m in the linear domain by the following equation based on the classic gradual channel approximation:

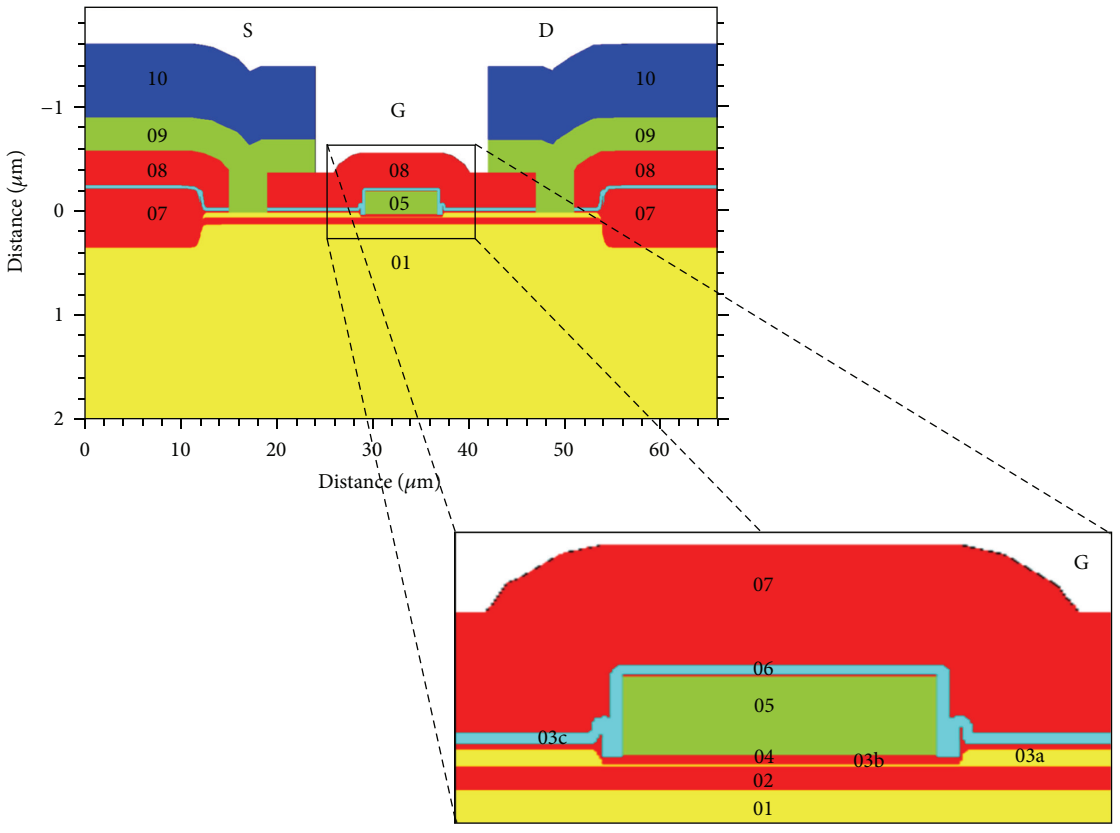
for $V_{GS} \geq 0$,

$$g_m \equiv \left.\frac{\partial I_{DS,lin}}{\partial V_{GS}}\right|_{V_{DS}} = \frac{W}{L}\mu_{eff}\left(\frac{\partial Q_n}{\partial V_{GS}}\right)V_{DS} \sim \frac{W}{L}\mu_{eff}C_{ox}V_{DS}, \quad (1)$$

$$\text{so } \mu_{eff} = \frac{Lg_{m,lin}}{WC_{ox}V_{DS}}. \quad (2)$$

According the extracted values g_m from Figure 4 for $V_{DS} = 0.1$ V and for other V_{DS} values (lower than 0.5 V to stay in the linear domain), we can estimate the effective mobility (μ_{eff}) independently of V_{GS} and V_{DS} for the four NSBs as seen in Figure 5.

Surprisingly the values were found lower than 10 cm$^2/V_s$ and weakly decreasing with t_{SI}. However, as far as we know, such a low order of magnitude was never reported in the main works dealing with sub 5 nm nanoscale SOI-MOSFET devices [22–24]. Moreover, the effective mobility is expected to decrease at low and high effective field values (due to the interface scattering degradation factor [25]), so g_m should decrease with V_{GS} and not be a constant with V_{GS} as seen from Figure 4.



01: bulk silicon	07: field oxide (FOX)
02: buried oxide (BOX)	08: silox
03a: original silicon-on-insulator	08: silox (SOX)
03b: gate-recessed silicon channel	09: polysilicon source/drain contact
03c: pad oxide (PAD OX)	10: aluminum
04: gate oxide (GOX)	S: source
05: polysilicon	G: gate
06: nitride	D: drain

FIGURE 3: Cross-view of a TCAD (Tsuprem4) simulated nanoscale devices using the gate-recessed channel process. The layers deposition sequence is described in the text.

3.2. Effective Mobility versus Series Resistance at Zero V_{GS}. The electron mobility in similar SOI-MOSFETs is known to be strongly degraded by decreasing the channel thickness below 5 nm. Several important works have attributed the degradation to a combination of Coulomb scattering generated by surface states [23], surface roughness [24–26], and enhanced phonon [27] scattering mechanisms. According to [23], the surface roughness is described as a quantum effect mechanisms dominating at low temperature but strongly dependent on the channel thickness t_{SI} below 4 nm even at room temperature. The mobility is found to decrease theoretically as a t_{SI}^{6} law.

Such a discrepancy with our extracted effective mobility behavior inclined us to interpret our measurements in terms of a parasitic drain-source series resistance that overwhelm the intrinsic channel conductance g_d and "screen" the previously cited scattering mechanisms.

Indeed, it is well established that if source drain series resistance R_{SD0} competes with the channel conductance a decreasing of the drain current can be measured [28]. In the linear domain, at zero V_{GS}, the drain current can be described by the following equation:

$$\text{For } V_{GS} = 0 \geq V_T,$$

$$I_{DS,lin} = \left(\frac{g_d}{1 + g_d R_{SD0}}\right) V_{DS} \longrightarrow \frac{V_{DS}}{R_{SD0}} \quad \text{for } g_d \ll R_{SD0}, \tag{3}$$

where g_d is the conductance of the channel.

Table 1: Process parameters for deposited layers.

Layer number	Layer name	Layer acronym	Layer thickness [nm]	Function and properties
01	Bulk silicon	Bulk		Substrate p-type (10^{15} cm^{-3}) Resistivity: 14–22 Ω · cm Orientation ⟨100⟩
02	Buried oxide	BOX	70	Bulk insulator O^+ implantation energy: 120 keV (2.35 hours) Dose: 0.39 10^{18} O^+/cm^2 Anneal: 1320°C (6.00 hours)
03a	Silicon-on-insulator	SOI	46	p-type (10^{15} cm^{-3}) regular transistor channel in UTB devices and nonreduced SOI in NSB devices (source-drain extensions)
03b	Gate-recessed silicon	GRS	1.6–6.5 range	Thinned transistor channel in NSB devices
03c	Pad oxide	PAD OX	15	Relieve stress from silicon to nitride at high temperature
04	Gate oxide	GOX	26	Gate insulator
05	Polysilicon	Poly	220	Gate electrode
06	Nitride 2	Nit	30	Prevent further oxidation of the thin silicon layer during the implant's thermal annealing (NSB)
07	Field oxide	FOX	700	Active area insulator
08	Silox	SOX	350	Contact opening mask for source/drain and gate passivation
09	Polysilicon	Poly	220	Source/drain polycontacts Source/drain doping obtained by phosphorous implant Dose $D = 2.5\,10^{15}$ cm^{-2} Energy $E = 30$ keV HTA High temperature annealing $T = 1000$°C, (30 min)
10	Aluminum	Al	500	Source/drain metal contacts

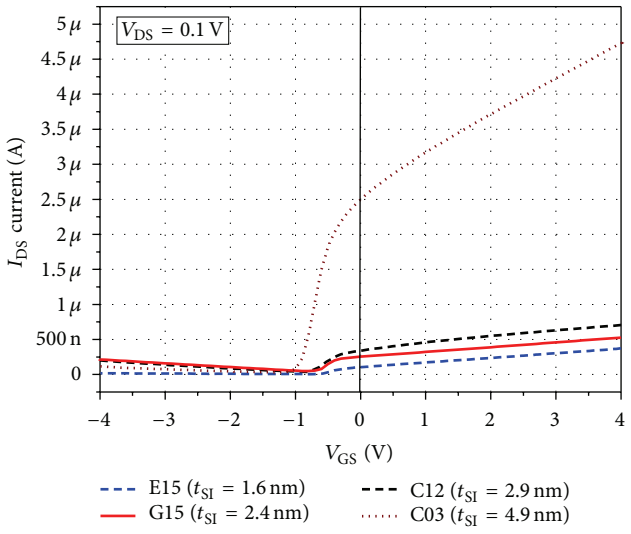


Figure 4: I_{DS}-V_{GS} characteristics measured at V_{DS} = 0.1 V for four NSB devices (dices E15, G15, C12, and C03) having a channel thickness (t_{SI}) of 1.6, 2.4, 2.9, and 4.9 nm, respectively.

Thus, by dividing the V_{DS} fixed value (0.1 V) by the intercept value of I_{DS} at zero V_{GS} a very large series resistance (R_{SD0}) can be calculated. By varying V_{DS} for low values (below 0.4 V), we got a linear dependence of I_{DS} with V_{DS} at zero V_{GS}, that is, confirmed explicitly by (3).

In Figure 6, the R_{SD0} values, as extracted from Figure 4, and μ_{eff}, evaluated from (1), are plotted versus the four selected channel thicknesses. The classic R_{SD0} vs. $1/t_{SI}$ hyperbolic decay due to the current spreading is plotted for reference but could not match the extracted values. As seen in the same figure, the best fit is found exponential as follows:

$$R_{SD0} = R^*_{SD0} e^{-t_{SI}/t_0} \tag{4}$$

with $R^*_{SD0} = 4.54\,\text{M}\Omega$ and $t_0 = 1.03$ nm.

In Figure 6, the μ_{eff} dependence on t_{SI} is found to be far from the theoretical t^6_{SI} dependence due to the roughness scattering [23, 24]. Moreover, the remote Coulomb scattering due to interface charges and reported to decay exponentially with t_{SI} in the subdeca-nanometer range [25] cannot match the extracted values of μ_{eff}. The interpretation of R_{SD} dependence with t_{SI} will be examined later in the paper (Section 4).

3.3. Extraction of the Series Resistance Degradation Factor with V_{GS}. In Figure 4, for positive V_{GS} values, the linear trend of I_{DS} with V_{GS} can be described by the following expression:

$$\text{For } V_{GS} > 0, \quad I_{DS,lin} = \frac{V_{DS}}{R_{SD0}} + g_m V_{GS}. \tag{5}$$

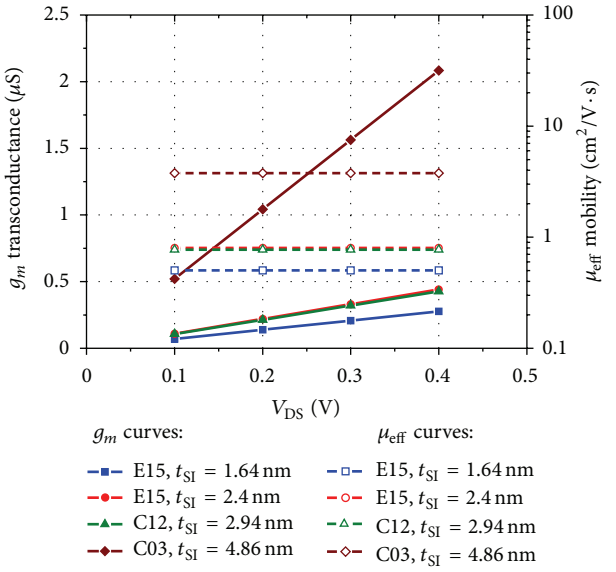


FIGURE 5: Extracted transconductance g_m and effective mobility μ_{eff} versus V_{DS} for four NSB devices (dices E15, C12, G15, and C03) having a channel thickness (t_{SI}) of 1.6, 2.4, 2.9, and 4.9 nm, respectively. g_m is extracted from Figure 4 as the slope of the I_{DS}-V_{GS} for positive V_{GS}.

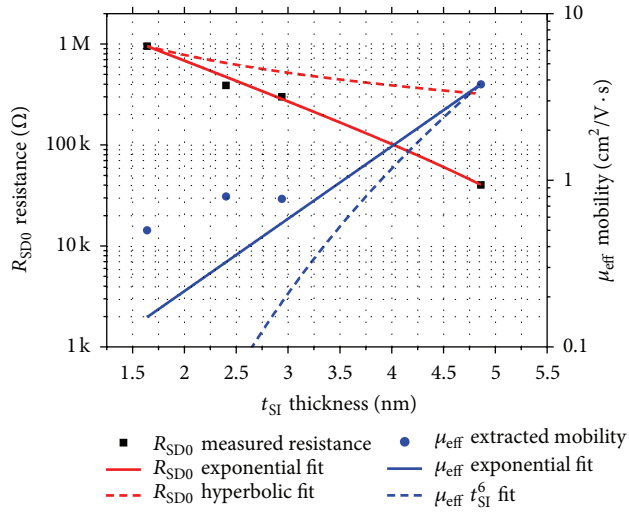


FIGURE 6: Semilog plot of R_{SD0} and μ_{eff} versus channel thickness for four NSB devices (dices E15, C12, G15, and C03) having a channel thickness (t_{SI}) of 1.6, 2.4, 2.9, and 4.9 nm, respectively. R_{SD0} is extracted from Figure 4 as the ratio of the V_{DS} constant value (0.1 V) to the drain current measured at zero V_{GS}. μ_{eff} is extracted from (2).

We can generalize (3) using a V_{GS} dependent series resistance R_{SD}. Since in the linear domain, $I_{DS,lin}$ has a Ohmic behavior with V_{DS}, and the R_{SD} expression can be extracted (5) as

For $V_{GS} > 0$,

$$I_{DS,lin} \equiv \frac{V_{DS}}{R_{SD}} \Longrightarrow R_{SD} = \frac{R_{SD0}}{1 + (g_m R_{SD0}/V_{DS})\, V_{GS}} \equiv \frac{R_{SD0}}{1 + \theta V_{GS}}, \quad (6)$$

where θ is the series resistance degradation factor (units V^{-1}).

The decreasing of R_{SD} at high positive V_{GS} has been already observed in classic MOSFET and LDD device [29, 30]. Consequently, θ can be extracted from g_m for a given R_{SD0} and V_{DS} from Figure 4. In Figure 7, θ is plotted versus the four selected channel thicknesses.

An hyperbolic fit best fit the θ decay with the channel thickness as follows:

$$\theta = \frac{\theta^*}{t_{SI}} \quad (7)$$

with $\theta^* = 1.1\,\text{nm} \cdot \text{V}^{-1}$.

Finally, the drain-source series resistance can be expressed by the following expression depending on t_{SI} and V_{GS}:

$$R_{SD} = \frac{R^*_{SD0} e^{-t_{SI}/t_0}}{1 + \theta^* V_{GS}/t_{SI}}. \quad (8)$$

3.4. I_{DS}-V_{DS} Characteristics and Model of the Saturation Current for NSB. In Figure 8 we present the measured I_{DS}-V_{DS} characteristics (sweeping V_{DS} from 0 to 15 V) for V_{GS} = 4 V

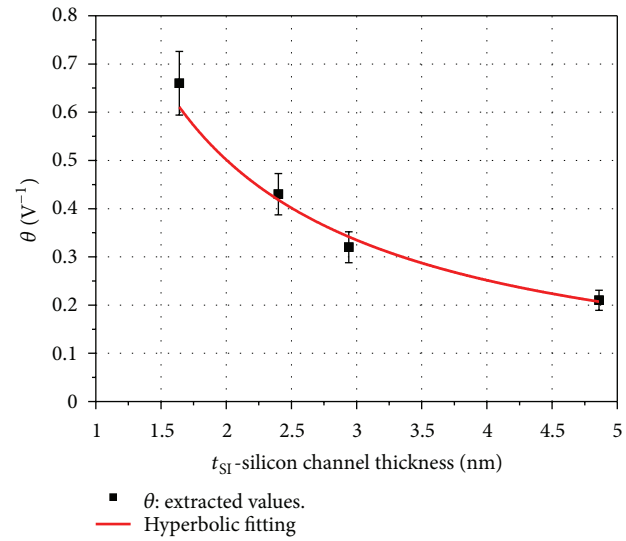


FIGURE 7: plot of theta versus the four channel thicknesses.

for NSB having, respectively, a channel thickness of 4.9 and 1.6 nm. On the one hand, for a given V_{GS}, the saturation current is decreased by decreasing the channel thickness t_{SI}. On the other hand, for a given V_{GS}, the saturation voltage is almost constant by decreasing the channel thickness. We propose a model to describe these saturation trends with t_{SI}.

3.5. Dependence of the Saturation Current $I_{DS,sat}$ on the Channel Thickness t_{SI} for NSB. Assuming that, for a given V_{GS}, the variation of the NSB's saturation voltage $V_{DS,sat}$ is

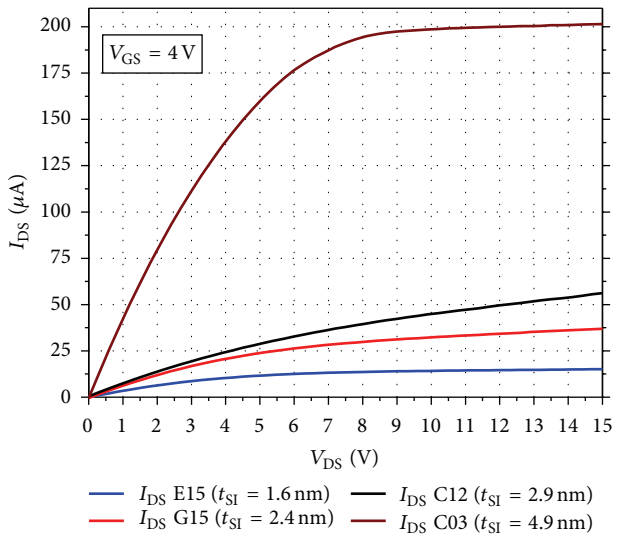


FIGURE 8: Measured I_{DS}-V_{DS} characteristics for NSB's thickness for four NSB devices (dices E15, C12, G15, and C03) having a channel thickness (t_{SI}) of 1.6, 2.4, 2.9, and 4.9 nm, respectively.

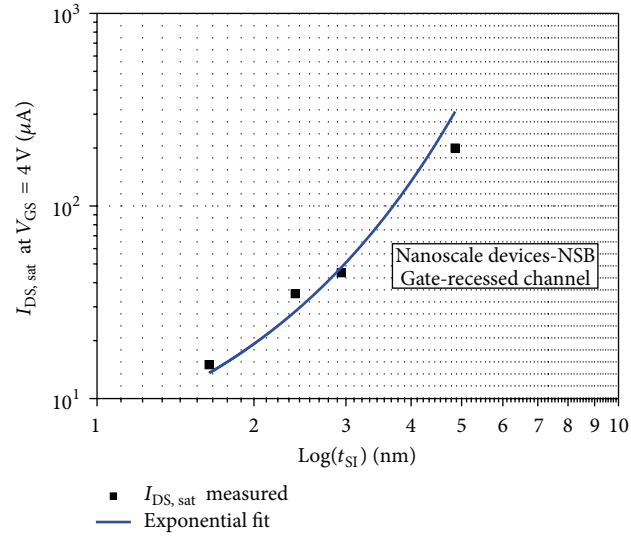


FIGURE 9: Measured saturation current (for V_{GS} = 4 V and V_{DS} = 15 V) versus channel thickness for NSB devices and fitted by the model given by (12).

mainly due to the R_{SD} drop voltage, and we can write the following:

$$\Delta V_{DS,sat} \approx \Delta\left(R_{SD} I_{DS,sat}\right). \tag{9}$$

Since the variation of $V_{DS,sat}$ is found weak with the t_{SI} especially below 4 nm, we can derive from (9)

$$\begin{aligned} \Delta V_{DS,sat} \approx 0 &\Longrightarrow R_{SD}\Delta I_{DS,sat} \approx -I_{DS,sat}\Delta R_{SD} \\ &\Longrightarrow \frac{\Delta I_{DS,sat}}{I_{DS,sat}} \approx -\frac{\Delta R_{SD}}{R_{SD}}. \end{aligned} \tag{10}$$

From (8) we can approximate (10) for V_{GS} = 4 V and low t_{SI} by

$$\frac{\Delta R_{SD}}{R_{SD}} \approx -\frac{t_{SI}}{t_0}. \tag{11}$$

By integrating (10) for V_{GS} = 4 V we get finally the modeled saturation current as function of the channel thickness t_{SI} according to

$$I_{DS,sat}\left(V_{GS} = 4\,\text{V}\right) \sim I_0\left(V_{GS} = 4\,\text{V}\right) \cdot e^{t_{SI}/t_0}. \tag{12}$$

In Figure 9, the modeled saturation current from (12) is plotted versus the channel thickness for NSBs. We can notice a good agreement with the measured saturation current (for V_{DS} = 15 V and V_{GS} = 4 V) for the different NSB's channel thicknesses.

4. Complementary Results for the Elucidation of Series Resistance

In order to corroborate our interpretation and to discriminate it from the carrier mobility, we added several results based on the classic R_m-L technique [31, 32] and the gate-to-channel capacitance measurement (or "split C-V" method) [33]. R_m is the measured resistance of the device defined by the reciprocal slope of the I_{DS}-V_{DS} linear characteristics, that is, $1/g_d$. We compared the measurements between two kinds of devices: NSB devices having a channel thickness of 1.6 nm and reference UTB devices, having a 46 nm channel thick. The channel width is fixed to 80 μm.

4.1. R_m-L Technique. In Figure 10, we compared for both the devices, the measured R_m taken at different gate lengths (L = 6 μm, 8 μm, and 100 μm), and for different positive gate voltages (V_{GS} = 0 V, 1 V, and 4 V). For the UTBs, R_m exhibits a linear growth trend with L, and a decreasing trend with V_{GS} as expected from the classic MOSFET channel resistance [31, 32]. Surprisingly, for NSB devices, R_m is found almost constant with L. This result indicates that the contribution of the channel resistance R_{ch} may be negligible for our devices. Assuming that R_m is a serial association of R_{ch} with the series source-drain resistance R_{SD}, R_m can be then approximated by R_{SD}.

Moreover, as seen in Figure 10, for NSB devices, R_m is found decreasing with V_{GS}. This is consistent with the trend already described in (6) for L = 8 μm. Therefore, these results indicate that the NSB resistance is not related to the intrinsic channel resistance but is apparently overwhelmed by an external series resistance that is almost independent of L. Although, series resistance is usually an association of contributions such as sheet contact resistance, spreading resistance, and other "wire resistance" [34, pages 223–225], none of these contributions exhibits the strong channel dependence like what is observed here. In our case, the measures resistance should be related to another scattering phenomenon.

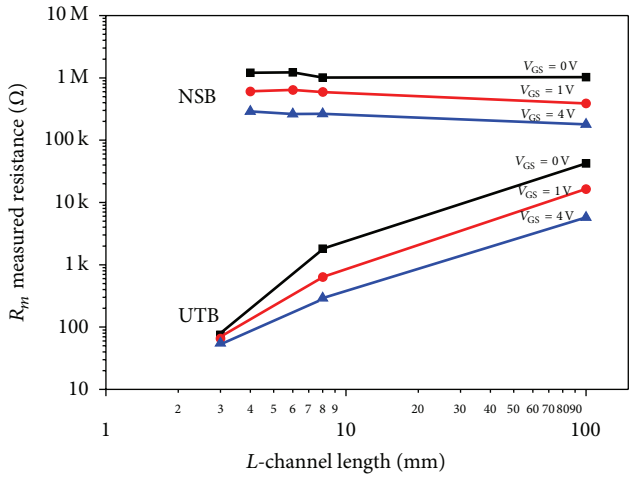


FIGURE 10: Comparison of the measured resistance R_m for NSB's devices having a channel thickness of 1.86 nm, with UTBs devices (46 nm channel thick), as function of channel length (L) and several V_{GS} positive values.

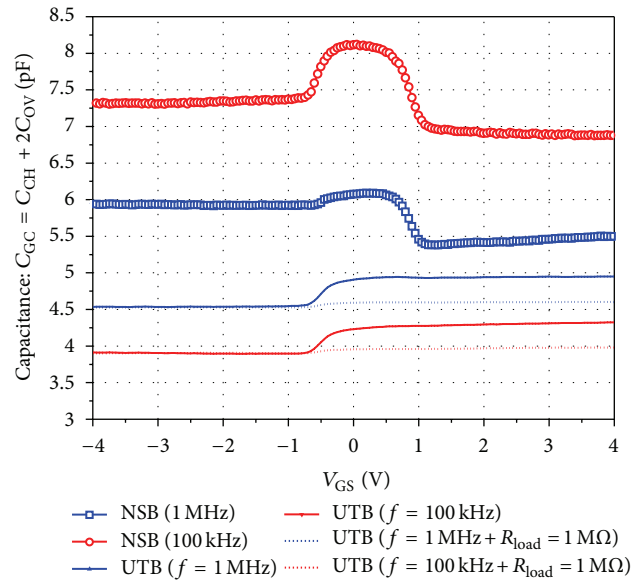


FIGURE 11: Representation of the gate-to-channel capacitance C_{GC} as a function of the V_{GS} voltage for UTB and NSB devices (at 100 kHz and 1 MHz).

4.2. Gate-to-Channel Capacitance C_{GC} versus Gate Voltage V_{GS}. In order to investigate the contribution of the inversion layer of the channel to the electrical conduction of the NSB, the gate-to-channel capacitance (C_{GC}) were measured versus V_{GS} for two frequencies (f = 100 kHz and f = 1 MHz) and compared to UTB's results. In this setup, the drain and source contacts are connected together to the voltage supply, while the substrate contact is grounded to shunt the source-substrate and drain-substrate capacitances. As presented in Figure 11, it clearly appears that below the threshold voltage V_T (about −0.5 V) the UTB's gate-to-channel capacitance is limited by a large overlap (or fringing) capacitance $2C_{ov}$ of about 4.5 pF and 3.9 pF at 1 MHz and 100 kHz, respectively. The overlap or fringing regions are located at the channel edges and/or the source and drain extension regions beside the channel. The positive shift of the capacitance with the frequency may be due to the influence of the cable capacitance on the offset capacitance value (significant at 1 MHz). Above V_T, C_{GC} increases and saturates, since the contribution of the channel capacitance (C_{CH}) is increasing and gets into its strong inversion value as observed in SOI-MOSFET [35]. However, the hump amplitude (0.4 pF) is found lower than the value expected for the UTB's front gate capacitance (0.8 pF). The similitude of the UTB curves for the both frequencies shows that the interface traps below the gate are not responding and then are negligible for these devices.

For the NSB device having the same dimensions than the previous UTB (W/L = 80/8 (μm)) but a channel thickness as low as 1.4 nm and below V_T, C_{GC} is also limited by a large overlap (or fringing) capacitance $2C_{ov}$ (both extensions regions) of about 6 pF and 7.3 pF at 1 MHz and 100 kHz, respectively. The small difference of C_{ov} between NSB and UTB may be due to the additional parasitic capacitance due to the thinning process. Like UTB's C_{GC} increases and saturates with hump amplitude of 0.7 pF still lower than the expected value for the NSB's front gate capacitance (0.9 pF). However, C_{GC} steeply decreases for positive V_{GS} before saturating to a value lower than the initial $2C_{ov}$ value. Moreover, the C_{GC} maximum at zero V_{GS} (contribution of the channel) decreases strongly by increasing the frequency from 100 kHz to 1 MHz. This frequency dependence could be explained by the presence of charged interface states that contribute to an additive capacitive component to C_{GC} at lower frequency [34, 35]. This is corroborated also by the degradation of subthreshold slope, as seen in Figure 4 and by the negative voltage threshold that makes our devices to be "depletion type" devices. These interface traps, located below the gate and at the upper silicon/silicon oxide interface, may be introduced during the thinning (oxidation) step of the gate-recessed process. Consequently, these trapped charges may also contribute to the Coulomb scattering as mentioned above [23] and contribute to the exponential decay of the measured resistance.

In order to check the influence of a huge series resistance on the previous C_{GC}-V_{GS} graph a serial load resistance of 1 MΩ is connected between the voltage supply and the UTB's source. From Figure 11, we can see that the capacitance hump is drastically reduced (to 0.05 pF) for both frequencies as expected from the capacitance relationship with series resistance assuming a parallel equivalent circuit [34, pages 88–90]. The overlap capacitance is reduced to 1.5 pF (compensated in the graph for comparison sake with unload UTB). So the series resistance may explain the decreasing of C_{GC} in the 0-1 V range for NSB devices in particular at 1 MHz but less at 100 kHz. One can interpret this difference by the fact that the surfaces states are more responsive at lower frequency and consequently could "shield" the series resistance effect. Moreover, since R_{SD} is decreasing with V_{GS}, its influence weakens at higher V_{GS} values, so it may explain the increase of C_{GC} at V_{GS} higher than 1 V at 1 MHz for NSB devices.

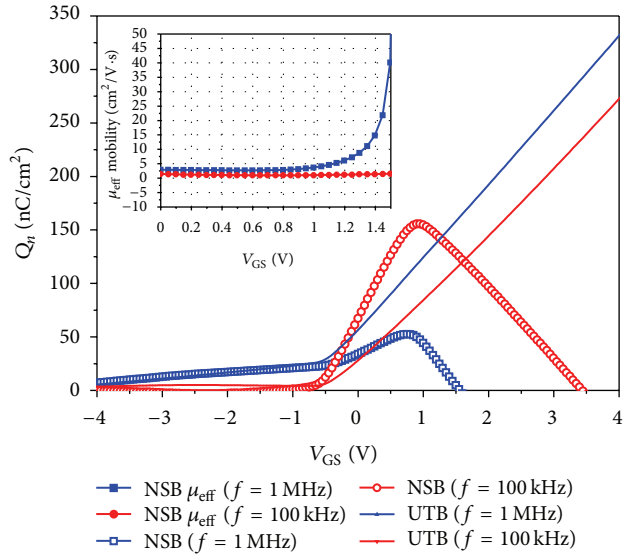


FIGURE 12: Representation of the mobile charge density Q_n as a function of the V_{GS} voltage for UTB and NSB devices (at 100 kHz and 1 MHz).

4.3. Mobile Charge Density and Effective Mobility Dependence with V_{GS}. The mobile charge density Q_n (C/cm^2) of the channel can be evaluated by integrating the previous curves C_{GC}-V_{GS} after subtracting the $2C_{OV}$ values (to extract the channel contribution C_{CH}) and by normalizing to the gate area (80 μm × 8 μm). In Figure 12, Q_n is plotted versus V_{GS} for UTB and NSB at 100 kHz and 1 MHz. While for UTB, the mobile charge density is increasing linearly in strong inversion (above V_T), and it is decreasing steeply and vanishing for NSB. By combining Q_n with the measured conductance ($1/R_m$) for a given V_{GS}, we can extract the effective mobility according to [34, page 541]

$$\mu_{\text{eff}} = \frac{L}{W} \cdot \frac{1}{R_m} \cdot \frac{1}{Q_n}. \tag{13}$$

For UTB, the mobility values extracted from (13) are compatible with the universal mobility curve [34, page 546] with an order of magnitude of 1000 cm^2/Vs. However, for NSB, the effective mobility values are smaller than 5 cm^2/Vs (but almost constant) with VGS in the 0–1.5 V range at 100 kHz (see insert in Figure 11). For 1 MHz, effective mobility is increasing with V_{GS}. These mobility values are compatible to these extracted. As already mentioned above, this value is a too low value compared to literature for the same kind of devices. Moreover, the increase of μ_{eff} at high V_{GS} values observed for both frequencies is not compatible with the expected degradation of the mobility at high effective field as reported in the literature [21–27]. This reveals the limitation of the mobility extraction method based on the C-V analysis in case of strong series resistance dependent on gate voltage. Consequently, in our case, the interpretation of the anomalously low conductance of the NSB relative to UTB could be better described by a series resistance model rather than by a conducting inverted channel for positive V_{GS} values. Another explanation of the exponential decay of the R_{SD0} with t_{SI} may be related to a quantum "skin-effect" phenomenon due to the electron wave function penetration at the oxide-channel interfaces [36], but here the trapping charge and coulomb scattering seem to better match our results.

5. Conclusion

Nanoscale SOI MOSFET devices were fabricated using a selective recess gate thinning process to get channel thicknesses scaling from 4.9 nm down to 1.6 nm. The electrical characteristics were measured and interpreted as a gate controlled series resistance. The resistance is found to decay exponentially with the channel thickness. An analytical model of the saturation current for the nanoscale devices was extracted accordingly. The model is found satisfying to fit the exponential dependence of the measured saturation current with the channel thickness. As suggested by the C-V dependence on frequency, this degradation may be related to a high charge density trapped at the channel-gate oxide interface. We admit that the exact origin of the conductance degradation is not trivial and more in depth work is needed. But, in our case, the series resistance interpretation was found more physically coherent than the extraction of the effective channel mobility from the split C-V technique that may lead to erroneous values and anomalous trends with V_{GS}.

Conflict of Interests

The authors have no conflict of interests associated with this paper.

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References

[1] D. Esseni, P. Palestri, and L. Selmi, "Nanoscale MOS transistors, semi-classical transport and applications," *Cambridge University Press*, 2011.

[2] A. Karsenty, A. Sa'ar, N. Ben-Yosef, and J. Shappir, "Enhanced electroluminescence in silicon-on-insulator metal-oxide-semiconductor transistors with thin silicon layer," *Applied Physics Letters*, vol. 82, no. 26, pp. 4830–4832, 2003.

[3] D. Abraham, A. Chelly, D. Elbaz, S. Schiff, M. Nabozny, and Z. Zalevsky, "Modeling of current-voltage characteristics of the photoactivated device based on SOI technology," *Active and Passive Electronic Components*, vol. 2012, Article ID 276145, 7 pages, 2012.

[4] M. Chan, F. Assaderaghi, S. A. Parke, S. S. Yuen, C. Hu, and P. K. Ko, "Recess channel structure for reducing source/drain series resistance in ultra-thin SOI MOSFET," in *Proceedings of the IEEE International SOI Conference*, pp. 172–173, October 1993.

[5] S. Cristaloveanu and S. S. Li, *Methods of Forming SOI Wafers—Electrical Characterization of S.O.I. Material and Devices*, Ch 2, Kluwer Academic Publishers, 1995.

[6] S. Cristoloveanu, "Status, trends and challenges of silicon-on-insulator technology—SOI metamorphosis silicon," *IEEE Circuits and Devices Magazine*, vol. 15, no. 1, pp. 26–32, 1999.

[7] M. Bruel, B. Aspar, B. Charlet et al., ""Smart cut": a promising new SOI material technology," in *Proceedings of the IEEE International SOI Conference*, pp. 178–179, October 1995.

[8] B. Dance, "European SOI Comes of Age," *Semiconductor International*, pp. 83–90, 1994.

[9] L. Peters, "SOI takes over where silicon leaves off," *Semiconductor International*, 1993.

[10] M. Alles and S. Wilson, "Thin film silicon on insulator: an enabling technology," *Semiconductor International*, vol. 20, no. 4, pp. 67–74, 1997.

[11] A. Auberton-Herve and T. Nishimura, "SOI-based devices. Status overview," *Solid State Technology*, vol. 37, no. 7, 1994.

[12] A. J. Auberton-Herve, J. M. Lamure, T. Barge, M. Bruel, B. Aspar, and J. L. Pelloie, "SOI Materials for ULSI Applications," *Semiconductor International*, pp. 97–104, 1995.

[13] T. E. Thompson, "SOI sandwich promises fast, low-power ICs," *Electronic Business Today*, pp. 43–47, 1995.

[14] J. Rhea, "DARPA low power program aims at mobile applications," *Military & Aerospace Electronics*, 1996.

[15] P. H. Singer, "U. S. Chipmakers: Penny-Wise, Million-Dollar Foolish," *Semiconductor International*, 1995.

[16] M. Bruel, B. Aspar, B. Charlet et al., ""Smart cut": a promising new SOI material technology," in *Proceedings of the IEEE International SOI Conference*, pp. 178–179, October 1995.

[17] A. Karsenty, *Study of the electrical and electro-optical phenomena in thin SOI MOS transistors [Ph.D. thesis]*, Hebrew University of Jerusalem, The Fredy & Nadine Hermann Graduate School of Applied Science, Microelectronics & Electro-Optics Divisions, 2003.

[18] L. Do Thanh and P. Balk, "Elimination and generation of Si-SiO_2 interface traps by low temperature hydrogen annealing," *Journal of The Electrochemical Society*, vol. 135, no. 7, pp. 1797–1801, 1988.

[19] S. Cristoloveanu and T. Ouisse, in *The Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface 2*, C. R. Helms and B. E. Deal, Eds., pp. 309–318, Plenum Press, New York, NY, USA, 1993.

[20] V. V. Afanos'ev, A. G. Revesz, and H. L. Hughes, "Confinement phenomena in buried oxides of SIMOX structures as affected by processing," *Journal of the Electrochemical Society*, vol. 143, no. 2, pp. 695–700, 1996.

[21] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Gate-induced drain leakage in FD-SOI devices: what the TFET teaches us about the MOSFET," *Microelectronic Engineering*, vol. 88, no. 7, pp. 1301–1304, 2011.

[22] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5 nm," in *Proceedings of the IEEE International Devices Meeting (IEDM '02)*, pp. 47–50, December 2002.

[23] K. Uchida, J. Koga, and S. Takagi, "Experimental study on carrier transport mechanisms in double- and single-gate ultrathin-body MOSFETs—Coulomb scattering, volume inversion, and δTSOI-induced scattering," in *Proceedings of the IEEE International Electron Devices Meeting*, pp. 805–808, December 2003.

[24] K. Uchida and S. Takagi, "Carrier scattering induced by thickness fluctuation of silicon-on-insulator film in ultrathin-body metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 82, no. 17, pp. 2916–2918, 2003.

[25] D. Esseni, A. Abramo, L. Selmi, and E. Sangiorgi, "Physically based modeling of low field electron mobility in ultra-thin single and double-Gate SOI n-MOSFETs," *IEEE Transactions on Electron Devices*, vol. 50, no. 12, pp. 2445–2455, 2003.

[26] F. Gámiz, J. B. Roldán, P. Cartujo-Cassinello, J. A. López-Villanueva, and P. Cartujo, "Role of surface-roughness scattering in double gate silicon-on-insulator inversion layers," *Journal of Applied Physics*, vol. 89, no. 3, pp. 1764–1770, 2001.

[27] F. Gamiz, J. B. Roldán, and J. A. López-Villanueva, "Phonon-limited electron mobility in ultrathin silicon-on-insulator inversion layers," *Journal of Applied Physics*, vol. 83, pp. 4802–4806, 1998.

[28] K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, *Semiconductor Device Modeling For VLSI*, Prentice Hall Series in Electronics and VLSI, C. S. Sodini Series, 1993.

[29] K. K. Ng and W. T. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFET's ," *IEEE Transactions on Electron Devices*, vol. 33, no. 7, pp. 965–972, 1986.

[30] M. Y. Kwong, C. Choi, R. Kasnavi, P. Griffin, and R. W. Dutton, "Series resistance calculation for source/drain extension regions using 2-D device simulation," *IEEE Transactions on Electron Devices*, vol. 49, no. 7, pp. 1219–1226, 2002.

[31] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET Channel Length," *IEEE Electron Device Letters*, vol. 1, no. 9, pp. 170–173, 1980.

[32] C. H. Chu Hao, B. Cabon-Till, S. Cristoloveanu, and G. Ghibaudo, "Experimental determination of short-channel MOSFET parameters," *Solid State Electronics*, vol. 28, no. 10, pp. 1025–1030, 1985.

[33] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Improved split C-V method for effective mobility extraction in sub-0.1-μm Si MOSFETs," *IEEE Electron Device Letters*, vol. 25, no. 8, pp. 583–585, 2004.

[34] D. K. Schroder, *Semiconductor Material and Device Characterization*, Ch 8, Wiley, 2nd edition, 1998.

[35] F. A. Ikraiam, R. B. Beck, and A. Jakubowski, "Modeling of SOI-MOS capacitors C-V behavior: partially- and fully-depleted cases," *IEEE Transactions on Electron Devices*, vol. 45, no. 5, pp. 1026–1032, 1998.

[36] A. I. Khan, M. K. Ashraf, and A. Haque, "Influence of wave function penetration on short channel effects in nanoscale double gate MOSFETs," in *Proceedings of the IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC '07)*, pp. 109–112, December 2007.