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Research Article

Sinusoidal Generator with $\pi/4$-Shifted Four/Eight Voltage Outputs Employing Four Grounded Components and Two/Six Active Elements

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This paper presents a new circuit proposal for multiphase sine-wave generation, employing two active elements and four grounded passive elements. The proposed oscillator provides four 45° phase-shifted voltage outputs. Incorporation of additional inverters for generation of eight-phase outputs is further shown. Simultaneous current outputs can also be generated with additional output stages. The compact circuit structure is studied for nonideal and parasitic effects and simulation results are given, which are in good agreement with the theory. The utility of the proposal for $\pi/4$-QPSK generation is explored as an interesting application example with supporting results.

1. Introduction

The differential-input version of second generation current conveyor has now become a standard active element for analog signal processing [1–4]. The generation of sinusoidal waveforms using current conveyors was first explored long back [5]. Development of new communication techniques and instrumentation needs led to the demand for phase-shifted sinusoidal signals, which resulted in quadrature and multiphase sinusoidal generators [6–10]. The use of two differential (or differential difference) voltage current conveyors (DVCC/DDCCs) for this purpose was found to be appropriate by several researchers and hence some works successfully demonstrated the aforesaid application. Whereas several works contributed oscillators with quadrature property employing only two DVCCs, there is a further scope of work where four-phase signals with $\pi/4$ radian separation are generated [8–11]. Even other two active element based works also demonstrate quadrature relationship in the four outputs [12–14]. There are few works which generate $\pi/4$ radian shifted signals employing a relatively large number of active elements ([14] and the references cited therein). This paper proposes a new two-DVCC and four-grounded components' based oscillator with four-phase voltage outputs, each with $\pi/4$ radian separation. The circuit is also extended for eight-phase generation, by employing additional inverters. PSPICE results along with a critical study are presented to validate the new circuit.

This paper is organized in subsequent sections in the following order. Section 2 is related to the actual circuit proposal. Section 3 deals with the comparison of proposed circuit with relevant oscillators employing two DVCCs. Section 4 presents the nonideal and parasitic considerations. Section 5 is devoted to the actual simulation results. An interesting application example in quadrature phase shift keying (QPSK) is given in Section 6. Section 7 is the paper's conclusion to be followed by references.

2. Circuit Description

The new proposed two-DVCC based circuit for four-phase sinusoidal generation is shown in Figure 1. It is to be noted that the DVCC with only $Z+$ output stage is employed, which requires only 12 transistors in its implementation. The DVCC with only $Z+$ output is characterized by

$$I_{Y1} = I_{Y2} = 0, \qquad V_X = V_{Y1} - V_{Y2}, \qquad I_{Z+} = I_X. \quad (1)$$

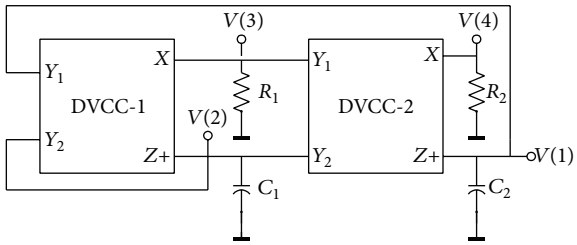

Figure 1: Proposed sinusoidal generator circuit.

The circuit schematic of such a DVCC is given in Figure 2. The four-phase oscillator circuit of Figure 1 has the following characteristic equation:

$$s^2 + s\left[\frac{1}{R_1C_1} - \frac{1}{R_2C_2}\right] + \frac{1}{R_1R_2C_1C_2} = 0. \quad (2)$$

The frequency of oscillation (FO) and the condition of oscillation (CO) are found as follows:

$$\text{FO}: f_o = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}; \qquad \text{CO}: R_2C_2 \le R_1C_1. \quad (3)$$

The relationship between the four generated outputs of Figure 1 is given as

$$\begin{aligned} V(4) &= sR_1C_2V(1), \\ V(1) &= \left(1 + sR_1C_1\right)V(2), \\ V(3) &= sR_1C_1V(2). \end{aligned} \quad (4)$$

Alternatively, the above equation may be simplified for equal component based design, namely, $R_1 = R_2 = R$ and $C_1 = C_2 = C$, as follows:

$$\begin{aligned} \frac{V(4)}{V(3)} &= \sqrt{2}\angle 45^\circ, \\ \frac{V(3)}{V(1)} &= \frac{1}{\sqrt{2}}\angle 45^\circ, \\ \frac{V(1)}{V(2)} &= \sqrt{2}\angle 45^\circ. \end{aligned} \quad (5)$$

Equation (5) suggests that the four outputs will have a progressive shift of 45°. $V(4)$ leads to $V(3)$ by 45°; $V(3)$ leads to $V(1)$ by 45°, and $V(1)$ leads to $V(2)$ by 45°. Equation (5) further suggests equal amplitudes for $V(4)$ and $V(1)$ at the FO. The other two outputs $V(3)$ and $V(2)$ are also equal in magnitudes but 0.707 times the outputs $V(4)$ and $V(1)$. It is to be noted that for equal component design the frequency of oscillation becomes FO = 1/2ΠRC.

It may be noted that four current outputs can also be obtained by employing additional Z stages within the DVCCs, so as to enable simultaneous access to current outputs, which is not shown here, with a view to retain the use of DVCC with only one Z+ output. The proposed circuit can be further extended for eight outputs, by incorporating

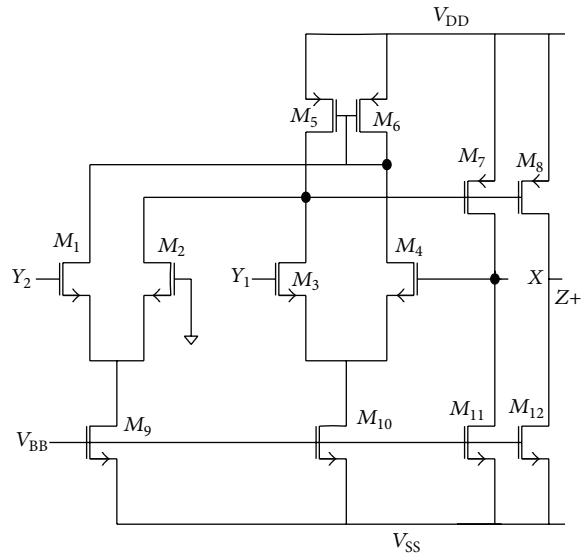

Figure 2: DVCC with only Z+ output.

inverters, so as to yield an eight-phase oscillator, at the cost of additional DVCCs. It may be noted that a DVCC with input at Y_2 and output at X (rest terminals grounded) realizes a possible inverter for the purpose. Here, the Z stage transistors need not be implemented. The aspect would be further explored later in the application's section.

3. Comparative Study

The proposed circuit is compared with two-DVCC based oscillators [8–11] in tabulated form as shown in Table 1, which shows that the proposed circuit offers compact realization, by employing fewer Z stages as compared to other works. The closest work [8] uses eight Z-stages to obtain four voltage and four current outputs. The proposed work, if extended to four current outputs, along with four voltage outputs would only require six Z-stages. When compared to all other available works with progressive 90° shifted outputs, the proposed work provides progressive 45° separated four output signals.

Though not from a comparative point of view, there are several two active element based oscillators in technical literature. Out of a large number of works, the circuits based on two CCIIs (second generation current conveyors), two CFOAs (current feedback operational amplifiers), two CDTAs (current differencing transconductance amplifiers), and so forth (just to name a few) are some examples of the rich literature on the subject ([15–20] and the references cited therein). All these circuits have their own advantages but do not provide four-phase features. Some three active element based works include resistorless tunable oscillator with two voltage and two current outputs [15], and a four-phase circuit using three active and eight passive components [16]. A recent work on oscillator provides electronically tunable circuit with voltage and current outputs for low frequency operation [17]. As far as the feature of 45° separated four outputs is concerned, it is not available in any of these

Table 1: Comparison with other DDCC/DVCC based works.

Reference	Number of resistors	Number of capacitors	Output voltages	Output currents	Total number of Z stages used	Maxm. FO shown (MHz)
[8]	2	2	4	4	8	0.8
[9]	2	2	2	2	4	0.13
[10]	2	2	2	3	6	8
[11]	3	2	2	NA	2	1.6
Work	**2**	**2**	**4**	**—/4**	**2/6**	**14**

NA: not available or not shown in the work.

works. Thus, the new proposal does provide knowledge enrichment on the subject of oscillator realization [4–22]. As a further thought, it is worth mentioning that the literature on oscillator realization using commercially available chips includes sea of knowledge based on op-amps, OTAs, CFOAs, and so forth. Even the ones based on not readily available chips have been successfully realized employing off-the-shelf chips.

4. Nonideal and Parasitic Considerations

4.1. Nonideal Study. A more realistic DVCC is characterized by nonunity current and voltage transfer gains, namely, α and β, respectively. The nonideal DVCC is described by the following relationship:

$$I_{Y1} = I_{Y2} = 0, \qquad V_X = \beta\left(V_{Y1} - V_{Y2}\right), \qquad I_{Z+} = \alpha I_X. \tag{6}$$

The nonideal FO and CO are now found as

$$\text{FO}: f_o = \frac{\sqrt{\alpha_1\alpha_2\beta_1\beta_2}}{2\pi\sqrt{R_1R_2C_1C_2}}, \qquad \text{CO}: \alpha_1R_2C_2 \leq \alpha_2\beta_2R_1C_1. \tag{7}$$

From (7), the active and passive sensitivities of FO are analyzed and found as

$$S^{fo}_{R_1,R_2,C_1,C_2} = -S^{fo}_{\alpha_1,\alpha_2,\beta_1,\beta_2} = -0.5. \tag{8}$$

Equation (8) shows that the sensitivities are within 0.5 in magnitude, thus signifying good sensitivity performance.

4.2. Parasitic Effects. Further study concerns the parasitic elements of DVCCs and their influence on circuit performances. It has been well founded that current conveyors with resistive termination at X port are appropriate with a view to absorb X-terminal resistance (R_x). The proposed circuit with two resistors at X-terminal fulfills this feature. A good design must ensure the selection of external resistors to be in few kilo-ohms range to minimize the deviations in circuit parameters due to finite R_x. This is further necessary in view of the output voltages being tapped, namely, $V(3)$ and $V(4)$, across the two resistors. The Y to X transfer relationship with finite R_x incorporation becomes

$$V(3) = \frac{1}{1 + R_{x1}/R_1}\left[V(1) - V(2)\right], \qquad V(4) = \frac{1}{1 + R_{x2}/R_2}\left[V(3) - V(2)\right]. \tag{9}$$

A design ensuring $R_i \gg R_x$, $i = 1, 2$ results in ideal voltage transfer gains from Y to X terminals; that is, $V(3) = V(1) - V(2)$ and $V(4) = V(3) - V(2)$. However, it may further be noted that a value of R_i in few KΩ ensures good design, which does not violate integration limits of resistive values.

Next, a current conveyor based circuit design with capacitive terminations at Y and/or Z ports is good in absorbing the parasitic capacitances C_y and C_z, respectively. A good design around a current conveyor must then ensure appropriate selection of external capacitors, so as to minimize the parasitic effects. The proposed circuit with capacitive terminations at Y-Z shorted terminal, in both cases, fulfills the feature and hence is good at absorbing parasitic effects. The effective values of capacitances are given as

$$C_{1\text{eff}} = C_1 + 2C_Y + C_Z, \qquad C_{2\text{eff}} = C_2 + C_Y + C_Z. \tag{10}$$

Equation (10) is written assuming matched DVCCs, which is quite a genuine assumption especially for integrated environment, hence dropping suffix from the parasitic capacitances. A good design, as also mentioned above, will ensure minimal errors in FO, which may rise for smaller external capacitance selection. This is to be further discussed in the simulations' section.

5. Simulation Results

The CMOS circuit of DVCC with only Z+ output (Figure 2) is simulated using a supply voltage of ±2.5 V with V_{BB} as −1.6 V. The parameters' listing is available in many of the recent works, hence not repeated here for brevity reasons [4]. The circuit was designed using 10 pF capacitors and R_2 = 4 KΩ, R_1 adjusted in the vicinity (4.003 KΩ) to get sustained outputs. The theoretical FO for this design is 3.98 MHz. The four outputs are shown in Figure 3, where the simulated value of FO is found to be 3.98 MHz, which is the same as the theoretical value. In consistency with the theory, the amplitudes of $V(1)$ and $V(4)$ are equal, whereas those of $V(2)$ and $V(3)$ are 0.707 times the other two, any minute differences

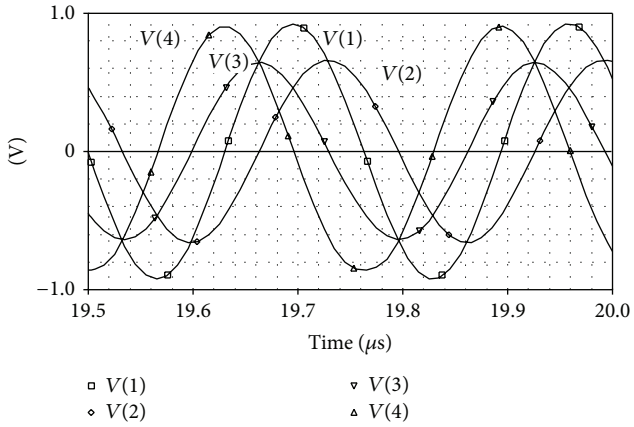

Figure 3: Four-phase outputs of the proposed circuit.

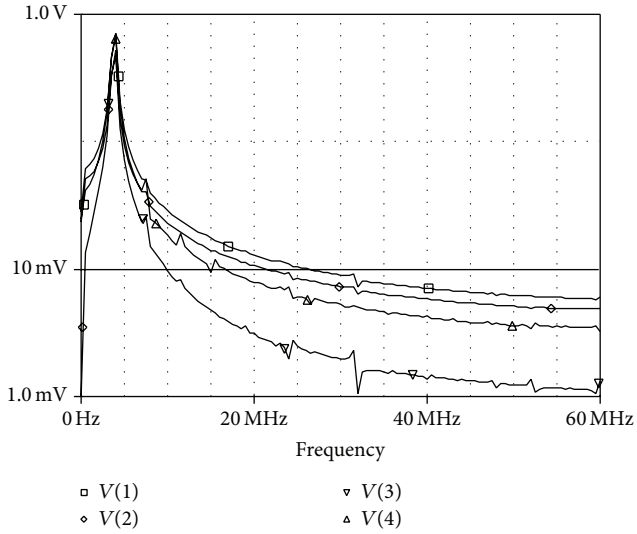

Figure 4: Fourier spectrum of the outputs.

occurring due to finite (nonunity) transfer gains. The Fourier spectrum of the outputs is further given in Figure 4, showing highly selective FO peaks with 3.6% or 6% THD in different waves. The tuning aspect of oscillator is also examined by using capacitors of different values so as to yield the variation as shown in Figure 5. The theoretical and simulated FO track each other for values of capacitors up to 5 pF below which errors start appearing because of parasitic effects. It may be noted that the resistive elements were not disturbed while varying the FO through capacitive elements. The condition of matched component implementation is therefore not a serious issue with modern integration techniques. Besides resistive elements, the programmable capacitor arrays (PCA) provide a second and more effective option for frequency tuning. Capacitance multipliers are another tuning option. These approaches are especially useful where the frequency and condition of oscillation have dependent terms. The CO for instance can be set using resistive elements, while the FO can be set through capacitive elements, as has been shown in Figure 5.

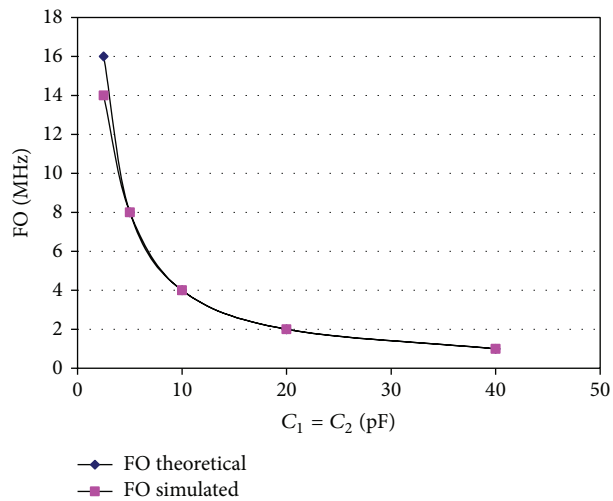

Figure 5: FO variation with different capacitors.

6. Application Example

The proposed circuit is further extended for eight-phase operation by incorporating DVCC based inverters as discussed in earlier section (shown in Figure 6), thus enabling generation of 45° separated eight outputs. The inverted versions of the four signals are obtained from the proposed circuit by using a DVCC based inverter in each case. The proposed circuit with eight $\pi/4$ radian separated signals has useful applications in $\pi/4$-QPSK signal generation. In this case, the signal set consists of two QPSK schemes, one rotated by 45° with respect to the other. For instance,

$$x_1(t) = A_c \cos\left(\omega_c t + \frac{k\pi}{4}\right) \quad k \text{ odd},$$
$$x_1(t) = A_c \cos\left(\omega_c t + \frac{k\pi}{4}\right) \quad k \text{ even}. \tag{11}$$

The phasor diagram for the eight outputs is shown in Figure 7. The modulation is performed by alternatively taking the output from each QPSK generator. Conceptual generation of $\pi/4$-QPSK signal is also shown in Figure 8, where alternative selection of two QPSK sets is shown. Equal amplitude outputs can be generated using only two additional scaling elements at the $V(2)$ and $V(3)$ outputs using DVCC itself so as to obtain Figure 9. It is worth mentioning that DVCC with only $Z+$ stage (Figure 2) is employed for the purpose with input at Y_2, (Y_1 grounded) scaled resistive terminations at X and $Z+$, so as to obtain scaled output at $Z+$. The four quadrature outputs are next shown (Figure 10) in each set, which are rotated by 45°. It may be noted that phase modulation with 8-phase values is used in EDGE (enhanced data rates for GSM evolution), which is considered a 2.5 generation (2.5 G) cellular system [23].

Keeping in view the particular application, the consideration of phase noise and frequency stability is of importance. For study of both of these aspects, oscillator is viewed as

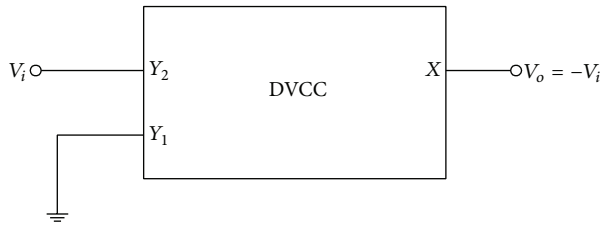

Figure 6: DVCC based inverter.

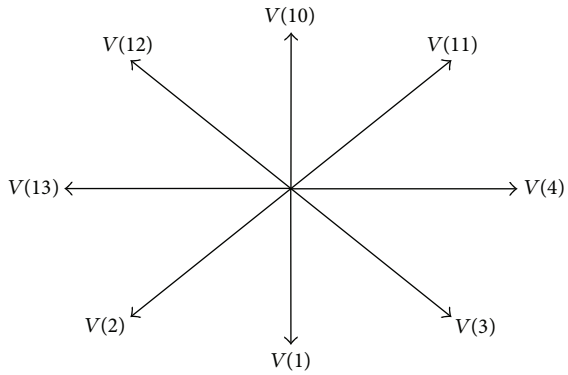

Figure 7: Phasor diagram for the 8-phase outputs.

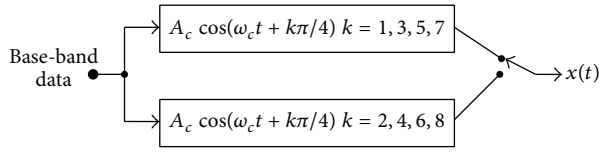

Figure 8: Conceptual generation of $\pi/4$-QPSK signal.

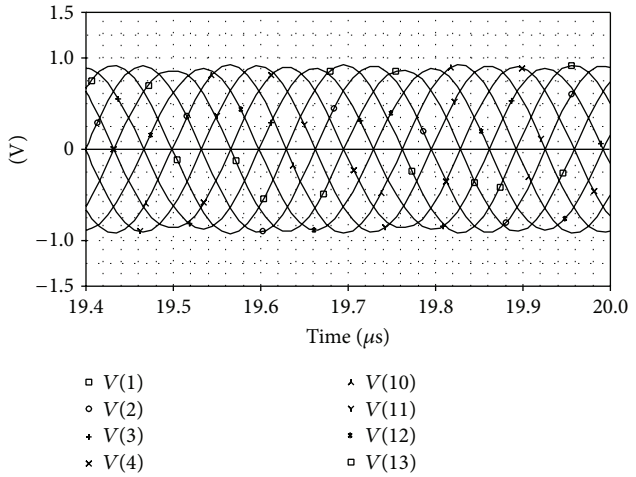

Figure 9: Equal amplitude eight outputs using two additional scaling elements.

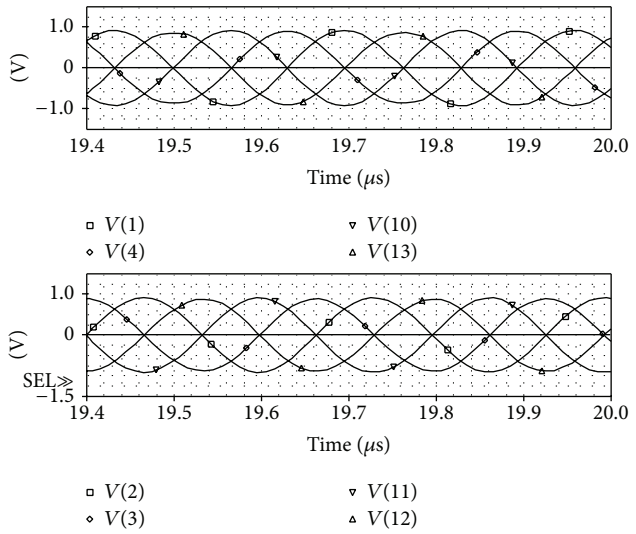

Figure 10: Four-quadrature-output alternate with 45° rotation.

a feedback system and the phase of the open loop transfer function is examined. Stability of the frequency of oscillation is determined by the slope of the phase response: a steep phase function results in more stable frequency. Similarly, the phase noise also depends on the slope of the phase function. Larger slope implies greater restoration property of the frequency of oscillation, and the frequency of the output waveforms remains constant for successive cycles. All these aspects are well depicted through the phase function, its slope and the stability factor indicator at FO as shown, respectively, in the plots of Figure 11. Both the stability factor and the phase noise performance are found to be good.

7. Conclusion and Discussion

This paper proposes a new multiphase oscillator employing two active elements, namely, differential voltage current conveyors and four grounded passive components. The proposed circuit generates four voltage outputs which are separated progressively in phase by 45°. Based on the used active element type and count, it is the first compact circuit for the purpose. The circuit is further extended for eight-phase operation by employing additional inverters, realized using DVCCs. As far as the transistors' count is concerned, it may be noted that the generation of four phases requires only 24 transistors. For eight-phase operation, the additional inverters using DVCC require 10 more transistors in each case. Thus eight-phase operation uses 64 transistors in all. Therefore, it seems that the four-phase generation is especially quite economical from transistors' count perspective. Complexity can be considerably reduced even for eight phase outputs, if simpler inverters are used in place of DVVC based ones. In either case, the use of inverters further adds to the feature of low output impedance for cascading purpose. On the other hand, counting on the number of active elements, four/eight phase outputs require two/six active elements. The circuit can also be extended to provide current outputs, by employing additional Z stages. The nonideal and parasitic considerations are also given, with the emphasis on the circuit's suitability to absorb various parasitic effects. Sensitivity figures are also analyzed and found to be low. The simulation results are

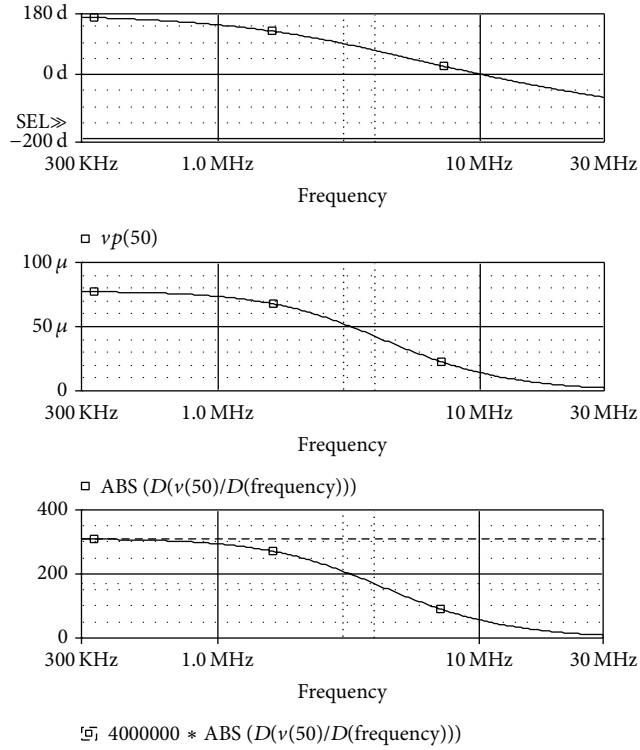

Figure 11: Phase function, phase slope function, and stability performance at FO of the proposed oscillator.

found to be in close proximity to the theoretical values, thus validating the new circuit proposal. An interesting application of the eight-phase sinusoidal oscillator in $\pi/4$-QPSK signal generation is further discussed, in support of the circuit's practical utility.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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