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Research Article

Y-Function Analysis of the Low Temperature Behavior of Ultrathin Film FD SOI MOSFETs

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The respective transfer characteristics of the ultrathin body (UTB) and gate recessed channel (GRC) device, sharing same *W/L* ratio but having a channel thickness of 46 nm, and 2.2 nm respectively, were measured at 300 K and at 77 K. By decreasing the temperature we found that the electrical behaviors of these devices were radically opposite: if for UTB device, the conductivity was increased, the opposite effect was observed for GRC. The low field electron mobility and series resistance R_{SD} values were extracted using a method based on *Y*-function for both the temperatures. If R_{SD} low values were found for UTB, very high values (>1 MΩ) were extracted for GRC. Surprisingly, for the last device, the effective field mobility is found very low (<1 cm^2/Vs) and is decreasing by lowering the temperature. After having discussed the limits of this analysis.This case study illustrates the advantage of the *Y*-analysis in discriminating a parameter of great relevance for nanoscale devices and gives a coherent interpretation of an anomalous electrical behavior.

1. Introduction

The *Y*-method for parameters' extraction which was first published more than two decades ago [1] had for purpose to isolate the source/drain series resistance ($R_{SD} = R_S + R_D$) influence from the intrinsic channel mobility factor. The method, which relies on combining drain current and transconductance transfer characteristics, enables reliable values of the threshold voltage V_T [2], the low field mobility μ_0, and the mobility attenuation coefficient θ_1 to be obtained. With time, this method was proved to remain compatible with previously existing ones, avoiding second order derivative procedure, and therefore to be applicable for inline parametric test extraction in the microelectronics industry [3]. It was also improved to overcome the difficulties encountered by applying the conventional techniques [4] and was applied to more complex devices having an architecture of nanoscale double-gate transistors [5] and fully depleted SOI MOSFETs with high-*k* and metal gate [6] and to devices in saturation regime [7]. This smart technique also permits the extraction of the gate voltage dependence of the series resistance [8].

The low temperature study of MOSFETs' general behavior [9–12], effective mobility [13–15], and source/drain series resistance [16] was started two decades ago while the focus of those analyses mainly remained fixed on the bulk silicon transistors. With the years, several useful models and laws were developed to treat these MOS devices. For example, a generalized law for drain current modeling was developed for silicon MOS transistors from liquid helium to room temperatures [17], as well as a method for parameter extraction which was oriented for very low temperatures [18].

Since the SOI technology became very attractive for high-performance and low-power applications (low leakage current, latch-up elimination, high soft error immunity, smaller subthreshold swing, reduced parasitic capacitance, simple device structure and process, etc.), similar low temperature research and deep analyses started on SOI MOSFETs, when focusing on the operation mode [19, 20], threshold voltage [21, 22], accentuated self-heating phenomenon [23], and parameters' extraction [24, 25].

The low temperature properties of SOI transistors are rather different from those of bulk devices as a consequence of the specific mechanisms existing in SOI structures. The

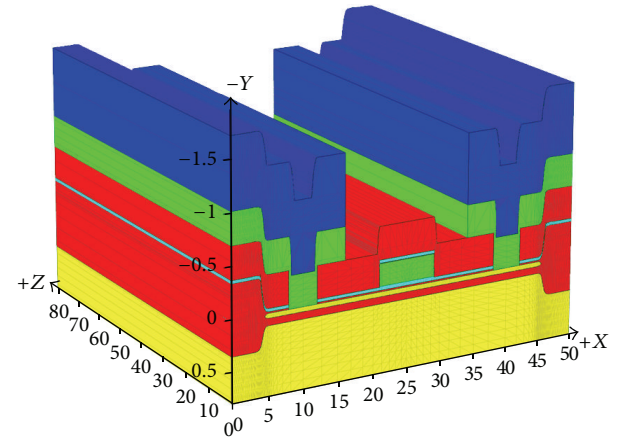
device is partially depleted (PD) in the high temperature range and becomes fully depleted (FD) in the low temperature range. The reduction of the V_T slope at low temperature occurs when the full depletion of the silicon film prevents the further extension of the depletion region under the gate [21]. Therefore, a substantial reduction of the variation of V_T versus temperature can be achieved in a fully depleted SOI MOSFET because of the suppression of the variation of the depletion charge with the temperature.

In this paper, we present the influence and behavior of series resistance at low temperature for FD-SOI MOSFETs by comparing between ultrathin body (UTB) and gate recessed channel (GRC) devices. The parameter extraction is performed above the threshold voltage using Y-function method. This aims to explain the anomalous transport behavior of the GRC device between room temperature and 77 K. This study comes to complete our previous works where we first evidenced the gate dependence of the series resistance (R_{SD}) in this device, using classic I-V modeling [26] and R_m-L and C-V techniques [27–29], and used the Y-function method for parameters' extraction [30] for room temperature results.

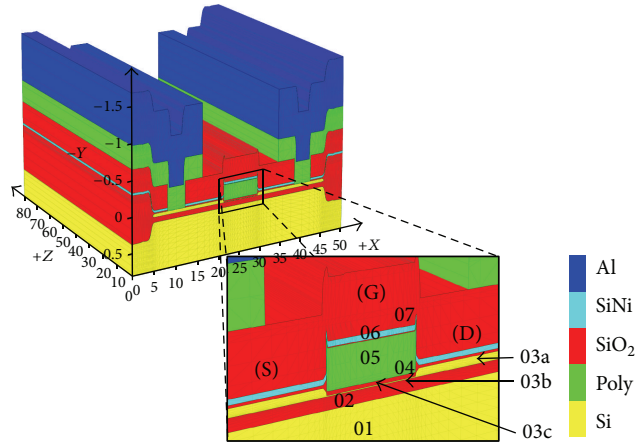
2. Device Processing and TCAD Simulation

The layers deposition process was simulated by a commercial 3D TCAD process simulator (Csuprem) from Crosslight Software Inc. [31] according to the real process conditions we used to fabricate our devices as previously published [32]. The simulated 3D structure of the ultrathin body (UTB) device having a 46 nm thick body and channel and W/L ratio of 10 (80 μm/8 μm) and used as a reference device is presented in Figure 1(a). In Figure 1(b), we show the simulated 3D structure of 4.6 nm thick channel obtained by the gate recessed process, that is, the gate recessed channel (GRC) device having the same W and L values. As presented in the upper insert the active region (source, gate, and drain terminals) is terminated by aluminum contacts (layer 10) in the vertical axis and limited by field oxide (layer 07) borders in the horizontal axis. The buried oxide (layer 02) is serving as a barrier between the bulk silicon (layer 01) and the gate recessed silicon channel (layer 03).

The lower insert of Figure 1(b) represents a zoom-in of the gate recessed channel, when the silicon layer was thinned from 46 nm to 4.6 nm. This points out advantage of the recessed process in which only the silicon channel is thinned while the source and drain regions and their respective extensions remain in their original (body) thickness. In addition to Figure 1, a complementary list of the process parameters at which most of them are used in the simulator was presented in summarizing Table 1. Both GRC and UTB devices were modeled in TCAD by applying almost the same process parameters used in their physical fabrications.



(a)



07. Field oxide	03c. Pad oxide (PAD OX)
06. Nitride	02. Buried oxide (BOX)
05. Polysilicon	01. Bulk silicon
04. Gate oxide (GOX)	(G) = gate
03a. Original silicon on insulator	(D) = drain
03b. Gate recessed silicon channel	(S) = source

(b)

Figure 1: Cross view of a 3D TCAD (Csuprem) process simulation of UTB (a) and GRC (b) devices having a channel thickness of 46 nm and 4.6 nm, respectively. The function and the process parameters of the numbered layers are given in Table 1.

3. Electrical Characterizations and Analysis

3.1. Experiment Setup and Conditions. Using the Semiconductor Characterization System (SCS-4200) from Keithley Ltd., the I-V measurements were first performed at room temperature (T = 300 K, dark conditions) in order to confirm the functionality of the measured transistors. The devices were inserted from the beginning on a cold finger support inside a Dewar specially designed for the experiments. Both I_{DS}-V_{DS} and I_{DS}-V_{GS} (g_m slope) characteristics were measured for each device, starting with the MOS standard I_{DS}-V_{GS} curves to check standard functionality. After the functionality screening step passed, the temperature was slowly taken down to 77 K. Stabilization time was required to assure the correct reading of the temperature in the vacuum chamber which was set to 2×10^{-7} bar. Since the analysis focused on the

Table 1: Process parameters for deposited layers of fabricated devices.

Layer number	Layer name	Layer acronym	Layer thickness (nm)	Function and properties
01	Bulk silicon	Bulk	500,000	Substrate p-type boron (10^{15} cm^{-3}) Resistivity: 14–22 Ω·cm orientation <100>
02	Buried oxide	BOX	70	Bulk insulator O^+ implantation energy: 120 keV (2.35 hours) Dose: 0.39 10^{18} O^+cm^{-2} Annealing: 1320°C (6.00 hours)
03a	Silicon on insulator	SOI	46	p-type boron (10^{15} cm^{-3}) regular transistor channel in UTB devices and nonreduced SOI in GRC devices (source/drain extensions)
03b	Gate recessed silicon	GRS	1.6–6.5 range	Thinned transistor channel in GRC devices
03c	Pad oxide	PAD OX	15	Relieve stress from silicon to nitride at high temperature
04	Gate oxide	GOX	26	Gate insulator
05	Polysilicon	Poly	220	Gate electrode
06	Nitride 2	Nit	30	Prevent further oxidation of the thin silicon layer during the implant's thermal annealing (GRC)
07	Field oxide	FOX	700	Active area insulator
08	Silox	SOX	350	Contact opening mask for source/drain and gate passivation
09	Polysilicon	Poly	220	Source/drain Polycontacts Source/drain doping obtained by phosphorous implant: dose $D = 2.5\,10^{15}$ cm^{-2}, energy $E = 30$ keV, and HTA high temperature annealing $T = 1000$°C (30 min)
10	Aluminum	Al	500	Source/drain metal contacts

gate voltage range, above the threshold voltage, and on the Y-function parameters extraction method, the respective linear transfer characteristics were deeply studied and compared in this paper.

3.2. Threshold Voltage and Mobility Extraction Using Y-Function. The I_{DS} versus V_{GS} transfer characteristics (ranging from 0 to +7 V) were measured in the linear domain, that is, for two low values of drain voltage (V_{DS}): 0.05 V and 0.1 V and above their respective threshold voltage V_T. In Figures 2(a) and 2(b), these characteristics are presented at linear scale for the UTB device (46 nm channel thick) at 300 K (room temperature) and at 77 K (liquid nitrogen), respectively. In Figures 2(c) and 2(d), the corresponding characteristics are presented for the GRC device (2.2 nm channel thick) at 300 K and 77 K, respectively. As observed in Figures 2(a) and 2(c), the GRC's drain current measured at 300 K (for V_{GS} = 7 V) is three orders of magnitude lower than those measured for UTB's at the same temperature. But at 77 K, as shown in Figures 2(b) and 2(d), this current ratio has almost reached five orders of magnitude. Such a huge current attenuation is not necessarily connected to a dumping of the electron mobility but can be related to the apparition of a huge series resistance during the channel thinning (gate recessed process). In order to discriminate the influence of the series resistance on the extraction of intrinsic device parameters, like threshold voltage and electron mobility, it is a common practice to use an extraction method based on the Y-function analysis. It is important to pay attention that Figures 2(d) and 3(d) (resp., I_{DS}-V_{GS} characteristics and Y-Function graphs) are presenting some fluctuation steps in their respective curves for GRC devices at $T = 77$ K.

The Y-method first introduced by Ghibaudo [1] has the interest to separate the respective contributions of the intrinsic channel conduction from the series resistance effect. However, this technique usually needs a set of devices with different channel lengths. As a novelty, we proposed, in a previous work [30], applying this method to our devices having a single channel length value by varying the drain voltage V_{DS} in the whole linear mode. In this case, we should take into account the $V_{DS}/2$ contribution in the potential of inversion layer ($V_{GS} - V_T$). Accordingly, the Y-function is expressed as follows:

$$Y \equiv \frac{I_{DS,lin}}{\sqrt{g_m}} = \sqrt{\beta V_{DS}}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) = a_Y + b_Y V_{GS}. \tag{1}$$

Assume

$$I_{DS,lin} \equiv \beta \frac{\left(V_{GS} - V_T - V_{DS}/2\right)}{1 + \theta_{1,0}\left(V_{GS} - V_T\right)} V_{DS}, \tag{2}$$

where

$$\beta = \frac{W}{L} C_{ox} \mu_0. \tag{3}$$

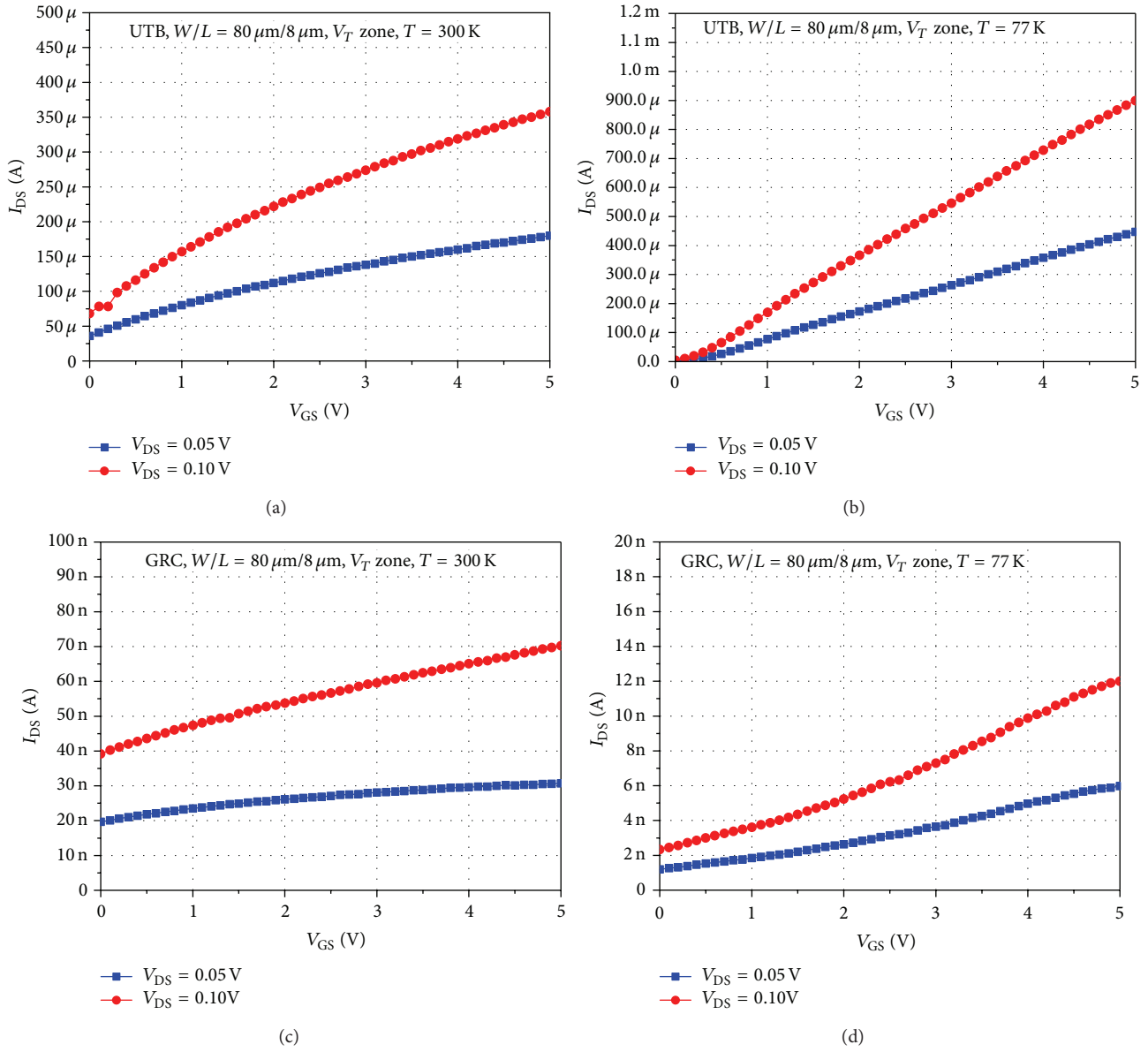


FIGURE 2: I_{DS}-V_{GS} characteristics measured above the threshold domain (linear domain) for UTB (t_{Si} = 46 nm) and GRC (t_{Si} = 2.2 nm), for two low V_{DS} values (0.05 V and 0.1 V): (a): UTB, W/L = 80 μm/8 μm and T = 300 K. (b): UTB, W/L = 80 μm/8 μm and T = 77 K. (c): GRC, W/L = 80 μm/8 μm and T = 300 K. (d): GRC, W/L = 80 μm/8 μm and T = 77 K.

And μ_0 is the low field electron mobility, while $\theta_{1,0}$ is the "intrinsic" mobility degradation factor. By using the effective mobility, μ_{eff} is given by the empirical relationship

$$\mu_{eff} \equiv \frac{\mu_0}{1 + \theta_{1,0}\left(V_{GS} - V_T\right)}. \quad (4)$$

Here we do not need to take into account the second degree degradation factor, unlike [5, 8], since the oxide equivalent thickness of our devices is large enough to avoid such term.

The Y-V_{GS} graphs can be straightforward derived from the I_{DS}-V_{GS} characteristics, as shown in Figures 3(a) and 3(b) for UTB at 300 K and 77 K, respectively. In Figures 3(c) and 3(d), Y-V_{GS} are presented for GRC at 300 K and 77 K, respectively. We can see there that, for positive V_{GS} values, the Y-functions are almost linear for UTBs but are significantly bended at higher V_{GS} values for GRC at 77 K. Moreover the slopes are V_{DS} dependent for UTB but almost independent for GRC.

Since the slope is not a pure constant of V_{GS}, in particular for GRC's devices, we will consider the maximum value of the Y-slope (Y'_{max}) as the b_Y parameter [30]. So, we can extract the threshold value V_T from the intercept of the tangent of the Y-function with the V_{GS} axis, according to the following:

$$V_T \equiv V_{T,Y'_{max}} = V_{GS}\left(b_Y\right) - \frac{Y_{max}}{Y'_{max}} - \frac{V_{DS}}{2} \quad \text{with } Y_{max} \equiv Y\left[V_{GS}\left(b_Y\right)\right]. \quad (5)$$

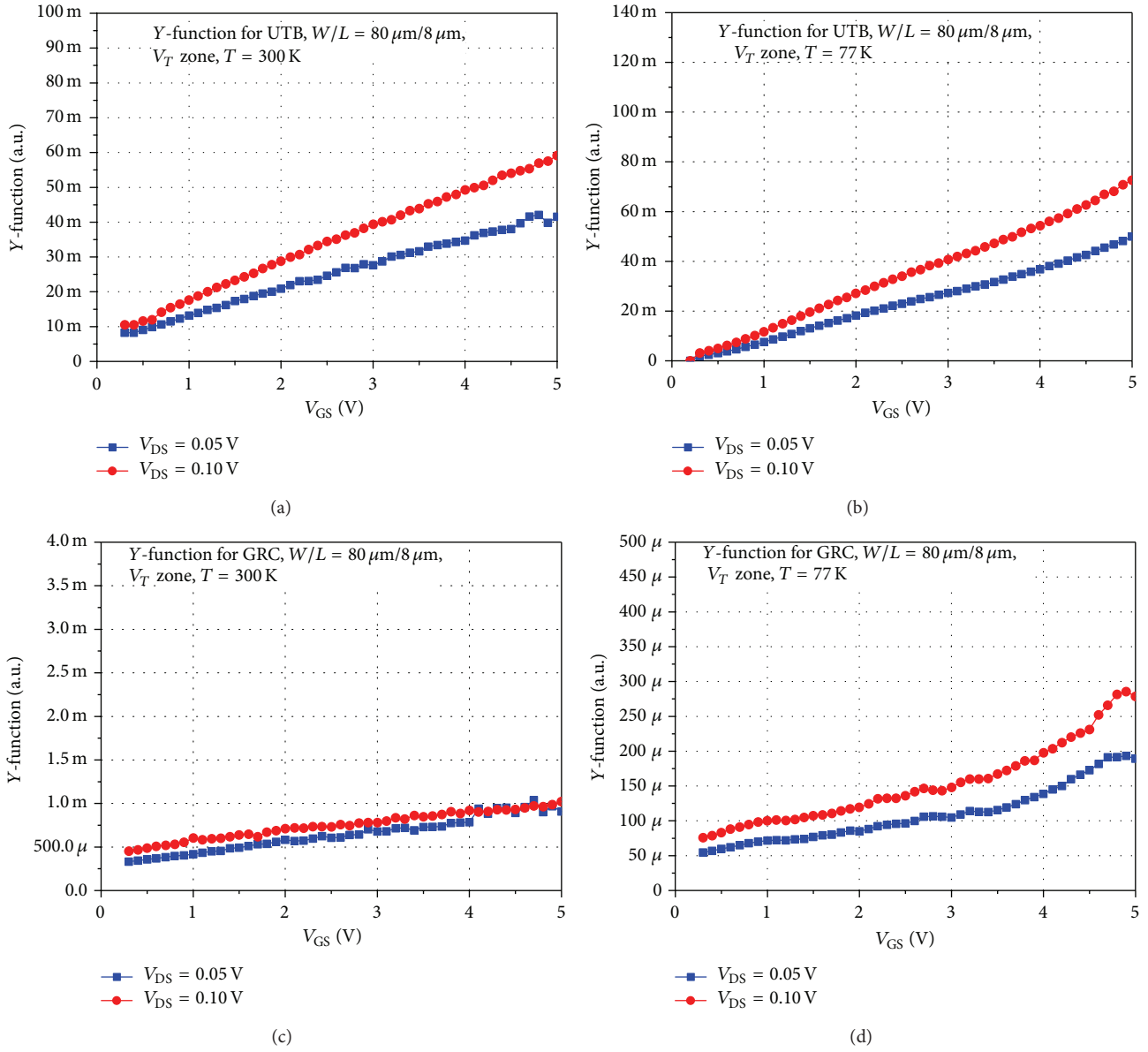


FIGURE 3: Y-functions measured above the threshold domain (linear domain) for UTB (t_{Si} = 46 nm) and GRC (t_{Si} = 2.2 nm), for two low V_{DS} values (0.05 V and 0.1 V): (a): UTB, W/L = 80 μm/8 μm and T = 300 K. (b): UTB, W/L = 80 μm/8 μm and T = 77 K. (c): GRC, W/L = 80 μm/8 μm and T = 300 K. (d): GRC, W/L = 80 μm/8 μm and T = 77 K.

The low field electron mobility can be also extracted from the slope parameter (b_Y) of the Y-function using the following equations:

$$\mu_0 = \beta\left(\frac{L}{WC_{ox}}\right), \tag{6}$$

where

$$\beta = \frac{b_Y^2}{V_{DS}}. \tag{7}$$

For GRC type devices, the front gate capacitance (C_{ox}) value was 138 nF/cm^2, for a 26 nm front gate oxide (GOX) thickness. For UTB the C_{ox} value was slightly lower (121 nF/cm^2) due to the 38 nm thick nitride layer capping the pad oxide in the gate region.

The extracted values of V_T and μ_0 obtained at V_{DS} = 0.05 V and V_{DS} = 0.1 V conditions are averaged and summarized in Table 2.

Note that both UTB and GRC are depletion-mode devices at 300 K (negative V_T for p-type channel). From Table 2, we can see that the UTB's threshold voltage and the low field electron mobility are strongly increased by decreasing the temperature from 300 K to 77 K. Conversely, for GRC's, the threshold voltage and the low field electron mobility are both

Table 2: Summarizing table of the threshold voltage V_T, the β factor, and the low field mobility extracted from the Y-function intersections and slopes and for UTB and GRC devices at 300 K and 77 K. A third row of UTB/GRC indicative ratios was added to emphasize the parameters difference between the two devices, built in the same conditions and process.

	$T = 300$ K			$T = 77$ K		
	V_T (V)	β (μS/V)	μ_0 (cm^2/Vs)	V_T (V)	β (μS/V)	μ_0 (cm^2/Vs)
UTB ($t_{Si} = 46$ nm)	−0.65	1470	1210	+0.26	2410	2000
GRC ($t_{Si} = 2.2$ nm)	−2.35	31	0.222	−2.60	0.007	0.005
Parameter ratio UTB/GRC	0.28	47.42	5,450	−0.10	344,286	400,000

Table 3: Summarizing table of R_{SD} and $\theta_{1,0}$ values extracted from the θ_1 versus β relationship. A third row of, this time, GRC/UTB indicative ratios was added to emphasize the parameters difference between the two devices and the huge R_{SD} ratio differences, built in the same conditions and process.

	$T = 300$ K			$T = 77$ K		
	R_{SD} (kΩ)	$\theta_{1,0}$ (V^{-1})	$R_{SD}\,\beta$ (V^{-1})	R_{SD} (kΩ)	$\theta_{1,0}$ (V^{-1})	$R_{SD}\,\beta$ (V^{-1})
UTB ($t_{si} = 46$ nm)	0.103	0.0215	0.151	0.046	−0.019	0.11
GRC ($t_{si} = 2.2$ nm)	1730	−0.176	0.530	8930	−0.146	0.06
Parameter ratio GRC/UTB	16,796	−8.19	3.51	194,130	7.68	0.54

decreased accordingly by decreasing the temperature from 300 K to 77 K.

If, for UTBS, the extracted μ_0 values are similar to those expected in silicon based devices, for GRC device, the corresponding μ_0 values are found very low and are inconsistent with the measured values of such kind of fully depleted SOI MOSFET's [33].

3.3. Series Resistance Extraction from θ_1 versus β Using X-Function for Variable V_{DS}. By introducing the series resistance R_{SD} in (2) and assuming $R_S = R_D = R_{SD}/2$, we get the classic expression

$$I_{DS,lin} = \beta \frac{(V_{GS} - V_T - V_{DS}/2)}{1 + \theta_1 (V_{GS} - V_T)} V_{DS}, \tag{8}$$

where θ_1 is the "extrinsic" mobility degradation factor including the series resistance according to

$$\theta_1 = \theta_{1,0} + R_{SD}\beta. \tag{9}$$

The mobility degradation factor θ_1 can be calculated using the X-function defined in [5]

$$X \equiv \frac{1}{\sqrt{g_m}} = \frac{1 + \theta_1 (V_{GS} - V_T)}{\sqrt{\beta V_{DS}}} = a_X + b_X V_{GS}. \tag{10}$$

Like Y-function, X is not a pure linear function of V_{GS} especially for GRC's devices. Consequently, we consider b_X as the maximum value of the X-function slope (X'_{max}). So, according to (10), the θ_1 values can be extracted as follows:

$$\theta_1 = b_X \sqrt{\beta V_{DS}} = b_X \cdot b_Y. \tag{11}$$

Since β is V_{DS} dependent, as seen from the previous Y-function analysis, we can plot θ_1 versus β according to (9) for the different V_{DS} values. In our case, R_{SD} is simply the slope of this plot, while $\theta_{1,0}$ is the intersection of the linear fit with the vertical (θ_1) axis. In case of fluctuations in the X'-V_{GS} graph, as observed for GRC's, the X'_{max} point is optimally chosen in order to get a coherent positive value of R_{SD}. The extracted values are summarized in Table 3.

It turns out that for the UTB device, the series resistance R_{SD} is decreased by a factor of 2 when decreasing the temperature from 300 K to 77 K while for GRC, R_{SD} is increased by a factor of 5. Moreover, the $\theta_{1,0}$ is found negative for UTB at 77 K and for GRC at both temperatures.

From the above equations, it is also possible to extract the analytical expression of R_{SD} as function of V_{GS} using the XY product as follows:

$$R_{SD} = \frac{V_{DS}}{Y^2}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)^2 \times \left[\left(\frac{XY}{V_{GS} - V_T - (V_{DS}/2)} - 1\right)\frac{1}{V_{GS} - V_T} - \theta_{1,0}\right]. \tag{12}$$

The calculated R_{SD} values modeled by (12) using the $\theta_{1,0}$ parameters values from Table 3 are shown in Figure 4 for UTB and GRC devices at 300 K and 77 K.

As a first observation, it appears from Figures 4(a) to 4(d) that small V_{DS} values (0.05 V and 0.1 V) are not influencing the series resistance behavior, since the curves remain almost matched at both 300 K and 77 K temperatures.

For UTB device, the R_{SD} series resistance is decreasing by a factor 5 by lowering temperature at moderate gate voltage overdrive (e.g., $R_{SD} = 100\ \Omega$ at $T = 300$ K versus $R_{SD} = 10\ \Omega$ at $T = 77$ K, for $V_{GS} - V_T = 3$ V). The opposite phenomenon is observed for GRC device ($R_{SD} = 1.75$ MΩ at $T = 300$ K versus $R_{SD} = 10$ MΩ at $T = 77$ K, for $V_{GS} - V_T = 3$ V). In all cases, the R_{SD} series resistance is found decreasing for moderated values of $V_{GS} - V_T$ (<4 V) while for higher $V_{GS} - V_T$ values, R_{SD} is found increasing.

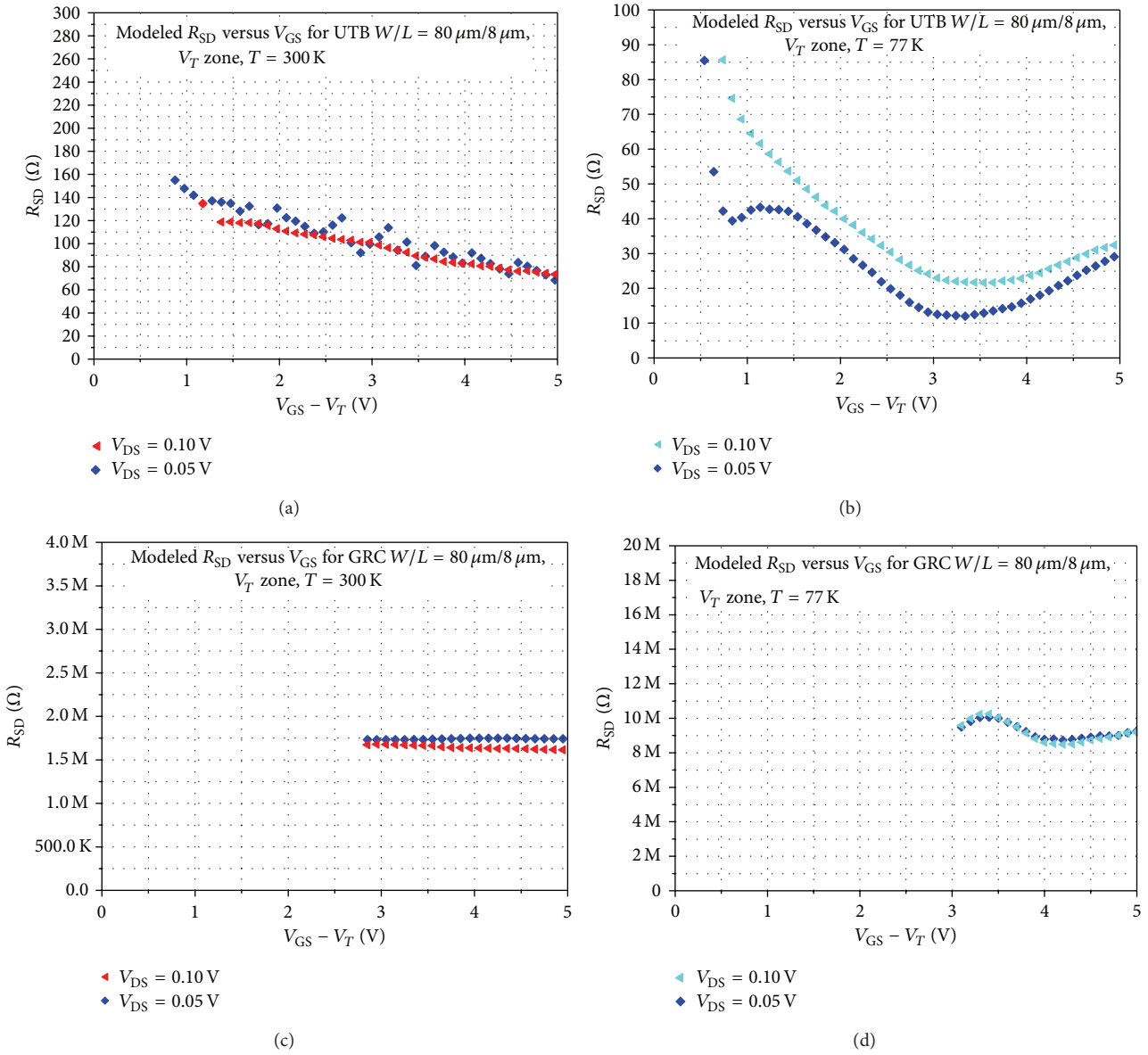


FIGURE 4: Modeled R_{SD} versus the gate voltage overdrive ($V_{GS} - V_T$), as extracted from the Y-function for UTB (t_{Si} = 46 nm) and for GRC (t_{Si} = 2.2 nm): (a): UTB, W/L = 80 μm/8 μm and T = 300 K. (b): UTB, W/L = 80 μm/8 μm and T = 77 K. (c): GRC, W/L = 80 μm/8 μm and T = 300 K. (d): GRC, W/L = 80 μm/8 μm and T = 77 K.

4. Interpretation and Discussion

4.1. Behavior of the Threshold Voltage at Low Temperature. According to Table 2, for UTB device the negative slope of V_T with temperature ($\Delta V_T/\Delta T$= −2.7 mV/K) can be related to the linear decrease of the Fermi potential with temperature as already observed in fully depleted (FD) and partially depleted (PD) SOI MOSFET [34]. However, for GRC, the threshold voltage is almost insensitive to temperature which is unexpected. In [34], the $\Delta V_T/\Delta T$ slope of FD was found lower than the PD on the channel thickness, meaning that for thinner channel the V_T is less sensitive to temperature as seen for our GRC device.

Previous works on ultrathin FD-SOI MOSFET devices at low temperatures have raised the explanation of the electrical behavior by quantum effects [33, 35]. For example, it was reported that for channel thickness of t_{Si} = 30 nm when the operating temperature was decreased from room to low temperatures, the threshold voltage V_T and the subthreshold slope increased. It was clearly reported that fluctuations of the drain current and the transconductance were due to quantum-mechanical phenomena found at operating temperature of 77 K [36]. Moreover, the threshold voltage increases steadily in SOI films thinner than t_{Si} = 6 nm, due to the occurrence of quantum effects. As mentioned above, in our case, the device channel thickness is t_{Si} = 2.2 nm, so

we can assume, as a first approach, such kind of mechanisms may be responsible for the observed V_T variations.

The fluctuation steps, observed in I_{DS}-V_{GS} characteristics (Figure 2(d)), are accentuated in Y-function curves (Figure 3(d)) since they are obtained from the derivative of the former characteristics. Such step phenomena were already reported as quantum effects for channel having t_{Si} = 30 nm [36]. The fluctuations of the I_{DS}-V_{GS} characteristics indicating some oscillations of I_{DS} and Y in the subthreshold current region are believed to correspond to a Coulomb blockade [19], because of the combination of a large undulation period, and the local roughness will result in coupled barriers inside a channel.

4.2. Behavior of the Low Field Mobility at Low Temperature. According to Table 1, we noticed that, for UTB's, the electron low field mobility μ_0 is close to the bulk silicon value at 300 K (1300 cm^2/Vs) but much lower than the bulk value at 77 K (7560 cm^2/Vs). The increase of μ_0 is consistent with the classic behavior of the carrier mobility in this range of temperature due to the freezing of the lattice phonon scattering in silicon [37].

However, for GRC device, the electron low field mobility μ_0 values are found abnormally low comparatively to published data in such devices for both temperatures [5, 8, 33]. Moreover, unlike UTB's, μ_0 is found decreasing when decreasing the temperature.

From Table 2, we see that the $\theta_{1,0}$ values are found surprisingly negative for UTB at 77 K but are still negligible relative to $R_{SD}\beta$, for GRC at both 300 K and 77 K. However, such surprising results have been observed in an early study about SOI MOSFET according to McLarty et al. [38]. One may argue that a second order dependence on V_{GS} may be responsible for the nonlinearity of the Y-function as mentioned in [38] and more recently by Cros et al. [5]. This approach was efficient for a very thin gate oxide (<10 nm) where interface scattering is a dominant issue such that the mobility is found to be more degraded at the top interface than at the bottom interface, indicating that defects are more numerous at the top channel region [39]. But in our case, due to the relative thick oxide layer of our devices (25 nm), the latter consideration is not relevant so we could limit our analysis to the first order dependence for moderate values of V_{GS}. Another explanation was reported in [35], for which the processing of source and drain regions may also be at the origin of additional scattering centers near the source and drain regions. All these observations lead us to conclude that the electron mobility extraction using Y-function is not physically coherent for UTB at 77 K nor for GRC at both temperatures.

4.3. Behavior of the Series Resistance at Low Temperature. It is well known that the field effect mobility of long-channel MOSFETs (10 μm) can be strongly affected by additional series resistance [16]. This is particularly important at low temperature for which the channel resistance is lowered by the enhancement of the mobility. Since R_{SD} and L_{eff} are both critical parameters for device modeling, many studies were published in the past decades for both room and cryogenics temperatures [24].

The series resistance dependence on gate voltage was originally observed for LDD devices [40] but also for non-LDD devices [41]. Simultaneously, for short channel devices, the electrical effective channel length (L_{eff}) is reduced, and found also gate voltage dependent. However for all our devices the channel is long enough (8 μm), so the short channel effects are *a priori* negligible in our study. Nevertheless, since the β parameter is found V_{DS} dependent, which is not expected from (6) for a long-channel device, it turns out that the device conduction may be in fact connected to a short channel effect.

From Table 3 and Figure 4, we observed an increase by a factor 2 of the UTB's series resistance R_{SD} when decreasing the temperature from 300 K to 77 K. This trend has been also observed for bulk n-MOSFETs [24]. Indeed, below 150 K, the freeze-out effect of the doping impurities leads to an increase of the parasitic series resistance as reported in [25]. This effect is particularly enhanced in LDD and depletion-mode devices [42].

The decrease of the low field mobility by lowering the temperature was recently reported in [36] for nano-CMOS devices having a sub-100 nm channel length. All these observations reinforce the interpretation that, for GRC's, the conduction may no longer be governed by the channel inversion but is screened by a huge series resistance depending on V_{GS} [26–30].

We may interpret the series resistance effect by considering the bottleneck regions at the edge of the GRC channel as parasitic short channel transistors that are controlled by a fringing field from the gate. Another reason for the increase of the series resistance may be increasing the dopant concentration in the drain/source extensions zones due to lateral diffusion from the source/drain occurring during the gate recessed process.

4.4. Limitations of Extraction Method at High V_{GS}. On one side, Emrani et al. reported a general Y-function as $Y = (I_{DS}^2/g_m)^{1/n}$, where n is an empirical coefficient depending on temperature. The reported values are $n = 2$ in the range of T = 200–300 K and $n = 3$ at T = 4.2 K (liquid helium) while $n = 2.4$ is the best value at 80 K [15, 17]. On the other side, Simoen et al. [24] used a similar analysis and found $n = 2.08$ for 77 K and $n = 1.92$ for T = 300 K for MOS devices having a high resistive silicon substrate. The change of n value is attributed to a change of the scattering process. Indeed, if phonon scattering dominates near room temperature, other mechanisms such as Coulomb scattering by interfaces charges and surface roughness scattering are dominant at low temperatures for low and high transverse field, respectively [33]. However, for highly resistive devices, the influence of the temperature on n value is small which suggests that the scattering mechanism is still dominated by phonon scattering.

In our case, for GRC's devices, the first order analysis (corresponding to $n = 2$) of the Y-function leads to a coherence discrepancy for the electron mobility and also for R_{SD} at high transverse field. However, at 300 K, it allows

discriminating the contribution of the mobility from the series resistance with a good degree of confidence. This leads to confirmation the predominant role of the gate voltage dependent series resistance at both temperatures.

5. Conclusion

Y-function method based on a first order analysis has been shown to be effective to interpret the radically opposite electrical behavior which was observed at low temperature between ultrathin body (UTB) and gate recessed channel (GRC) devices, sharing the same *W/L* ratio but having a channel thickness t_{Si} of 46 nm and 2.2 nm, respectively. When decreasing the temperature the apparent conductivity was increased in UTB; the opposite effect is observed for GRC. This phenomenon which is usually not observed for similar FD-SOI MOSFET devices can be explained by the presence of massive series resistance which is increasing when taking down the temperature due to a freeze-out of the dopants. We conclude that, for GRC device, the series resistance extraction is more physically coherent than the electron mobility one for moderate transverse field. Without the *Y*-function analysis we would have concluded an incoherent low value and behavior of the electron mobility for this device. Finally, this case study may be useful for the scientific community as guidance to interpret nonconventional electrical characteristics of nanoscale devices.

Conflict of Interests

The authors have no conflict of interests associated with this paper.

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