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Research Article

Usage and Limitation of Standard Mobility Models for TCAD Simulation of Nanoscaled FD-SOI MOSFETs

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TCAD tools have been largely improved in the last decades in order to support both process and device complementary simulations which are usually based on continuously developed models following the technology progress. In this paper, we compare between experimental and TCAD simulated results of two kinds of nanoscale devices: ultrathin body (UTB) and nanoscale Body (NSB) SOI-MOSFET devices, sharing the same W/L ratio but having a channel thickness ratio of 10 : 1 (46 nm and 4.6 nm, resp.). The experimental transfer *I-V* characteristics were found to be surprisingly different by several orders of magnitude. We analyzed this result by considering the severe mobility degradation and the influence of a large gate voltage dependent series resistance (R_{SD}). TCAD tools do not usually consider R_{SD} to be either channel thickness or gate voltage dependent. After observing a clear discrepancy between the mobility values extracted from our measurements and those modeled by the available TCAD models, we propose a new semiempirical approach to model the transfer characteristics.

1. Introduction

Nanoscale silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistor (MOSFET) based devices are the building blocks of up-to-date systems allowing ultrafast data processing. This is in accordance with efforts to develop new generation of ultrafast computers based on combined electronic and signal processing on one hand [1] and advanced generations of nanoscale devices (NSB) for communication systems [2] on the other hand. Furthermore, the excellent control of leakage current and short channel effects, achievable by means of UTB SOI-MOSFET architectures, makes them good candidates for ultimate nanometer scale. Consequently, the transport properties' study of thin semiconductor films has attracted considerable attention in the recent years.

In this perspective, the use of TCAD tools for predicting and optimizing such advanced semiconductor devices has increased recently [3, 4]. Since the nanotechnology's process and device evolution is quite rapid, there may appear some gaps among existing TCAD models. Indeed, TCAD tools use classic parametric models where some of them tend to become obsolete for nanoscale devices. For instance, it is well established that quantum effects and/or interface effects mainly govern the conduction of modern devices (e.g., ballistic transport effects or decreasing of the mobility by decreasing the channel thickness) [5]. Moreover, series resistance effects are of great importance for such devices and are the scope of intensive research activities [6–8] as well as the usage of the Y-function method in the last decades [9–12] to extract this parameter [13]. In this paper, we show how a semiempirical model based on gate voltage dependent series resistance established in a previous work [8] can be integrated in a TCAD simulator to match nonconventional electrical transfer characteristics of FD-SOI MOSFETs.

2. TCAD Process Simulation

The layers deposition process was simulated by a commercial 3D TCAD process simulator (Csuprem from Crosslight) according to the process conditions used to fabricate

Table 1: Process parameters for deposited layers of fabricated devices.

Layer #	Layer name	Layer acronym	Layer thickness [nm]	Function and properties
01	Bulk silicon	Bulk	500,000	Substrate p-type boron (10^{15} cm^{-3}) Resistivity: 14–22 Ω·cm Orientation ⟨100⟩
02	Buried oxide	BOX	70	Bulk insulator O^+ implantation energy: 120 keV (2.35 hours) Dose: 0.39 10^{18} O^+cm^{-2} Annealing: 1320°C (6.00 hours)
03a	Silicon-On-Insulator	SOI	46	p-type boron (10^{15} cm^{-3}) regular transistor channel in UTB devices and nonreduced SOI in GRC devices (source-drain extensions)
03b	Gate-recessed silicon	GRS	1.6–6.5 range	Thinned transistor channel in GRC devices
03c	Pad oxide	PAD OX	15	Relieve stress from silicon to nitride at high temperature
04	Gate oxide	GOX	26	Gate insulator
05	Polysilicon	Poly	220	Gate electrode
06	Nitride 2	Nit	30	Prevent further oxidation of the thin silicon layer during the implant's thermal annealing (GRC)
07	Field oxide	FOX	700	Active area insulator
08	Silox	SOX	350	Contact opening mask for source/drain and gate passivation
09	Polysilicon	Poly	220	Source/drain poly contacts Source/drain doping obtained by phosphorous implant: dose D = 2.5 10^{15} cm^{-2}, energy E = 30 keV, HTA high temperature annealing T = 1000°C, (30 min)
10	Aluminum	Al	500	Source/drain metal contacts

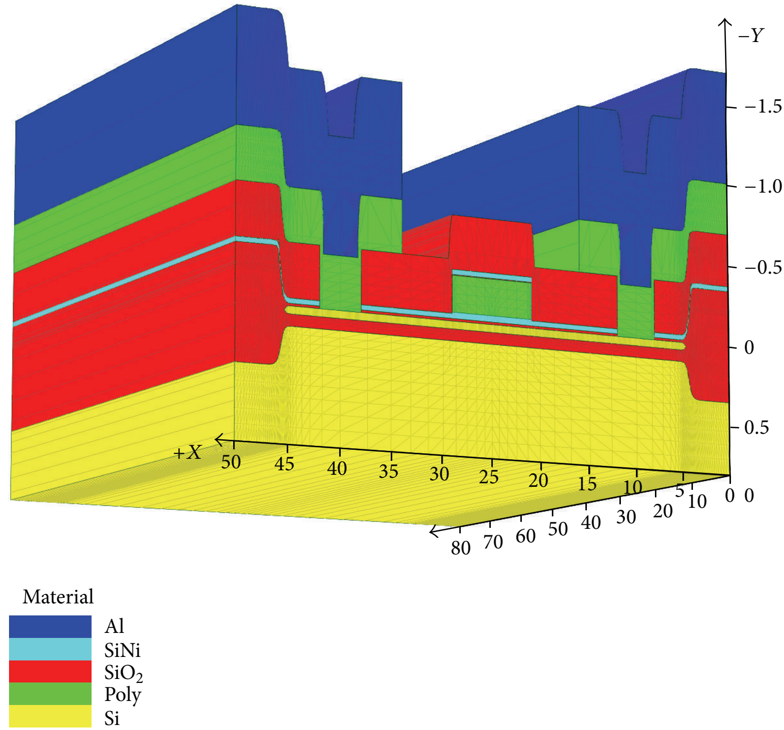
the devices as previously published [8]. In Figures 1(a) and 1(b) we present the simulated 3D structure of the ultrathin body (UTB) device, having a 46 nm thick body and channel and W/L ratio of 10 (80 μm/8 μm) and used as a reference device. In Figures 2(a) and 2(b), we show the simulated 3D structure of a ten-time reduced 4.6 nm thick channel obtained by the gate-recessed process, that is, the nanoscale body (NSB) device, sharing the same W and L values. As presented in Figures 1(a) and 2(a), the active region (source, gate, and drain terminals) is terminated by aluminum contacts (layer 10) in the vertical axis and limited by field oxide (layer 07) borders in the horizontal axis. The buried oxide (layer 02) is serving as a barrier between the bulk silicon (layer 01) and the gate-recessed silicon channel (layer 03).

Figure 2(b) represents a zoom-in of the gate-recessed channel, when the silicon layer was thinned from 46 nm to 4.6 nm. This points out advantage of the recessed process in which only the silicon channel is thinned while the source and drain regions and their respective extensions are remaining in their original (body) thickness. So the series resistance of the drain and of the source should not be affected *a priori* by the thinning process [14].

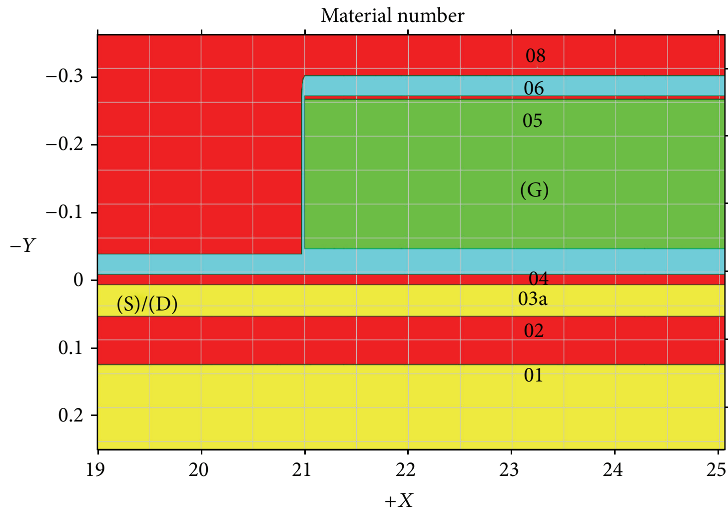
In addition to Figures 1 and 2, presenting a simulated TCAD cross-view of the device layers, a complementary list of the process parameters, most of which are used in the simulator, was presented in summarizing Table 1. Both the NSB and UTB devices were modeled in TCAD by applying almost the same process parameters used in their physical fabrications. However, the NSB process deviated from its actual microfabrication in the timing of annealing steps. Due to quite difficult control of the channel doping and thus of the threshold voltage in NSB devices, only a single annealing step was applied after ion implantation for a very short period (1-2 min, 1000°C) to fit the measured threshold voltage. It was observed that a slight change in the annealing time in the simulation could be enough to convert the channel region into excessively doped silicon due to the donors' diffusion from the drain and source sides. Furthermore, since dry oxidation of polysilicon is not available in the used simulation tool, a deposition (plus annealing for 46 nm) step was inserted.

3. Electrical Transfer Characteristics

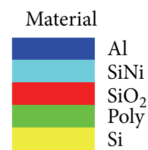
3.1. Measurements versus Simulations. I-V measurements (room temperature and dark conditions) were performed on both the UTB and the NSB's devices having a common channel width and length (W/L = 80 μm/8 μm = 10) but a channel thickness (t_{SI}) of 46 nm and 4.6 nm, respectively. The corresponding transfer characteristics, that is, drain currents (I_{DS}) versus gate voltage (V_{GS}) from −2 to +2 V, were measured in the linear domain (constant low V_{DS} = 0.1 V) and are presented in Figure 3. In addition we added the corresponding simulated characteristics (Apsys from Crosslight) using the default Canali or the so-called "beta"



(a)

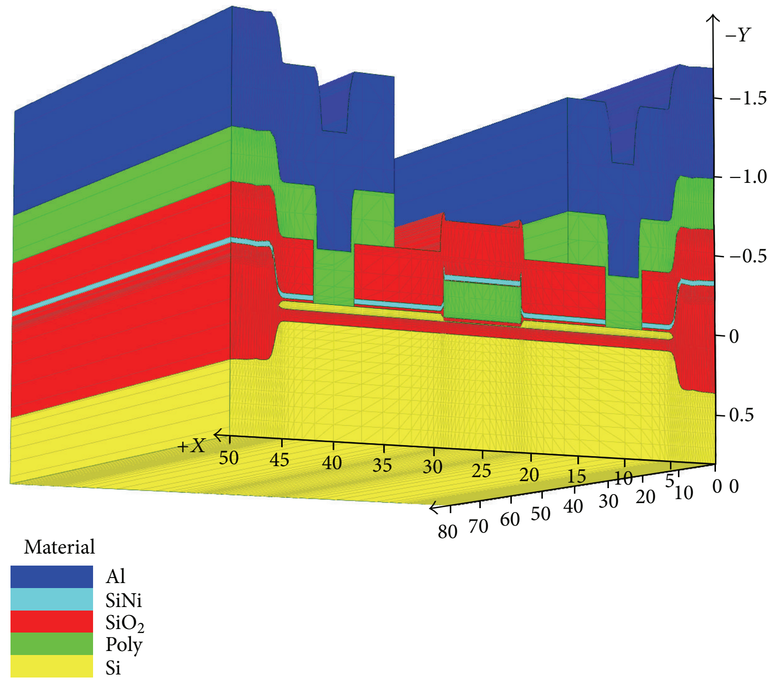


(10) Aluminum
(09) Polysilicon source/drain contact
(08) Silox (SOX)
(07) Field oxide
(06) Nitride
(05) Polysilicon
(04) Gate oxide (GOX)
(03a) Original silicon-on-insulator
(03b) Gate-recessed silicon channel
(03c) Pad oxide (PAD OX)
(02) Buried oxide (BOX)
(01) Bulk silicon
(G) Gate
(D) Drain
(S) Source

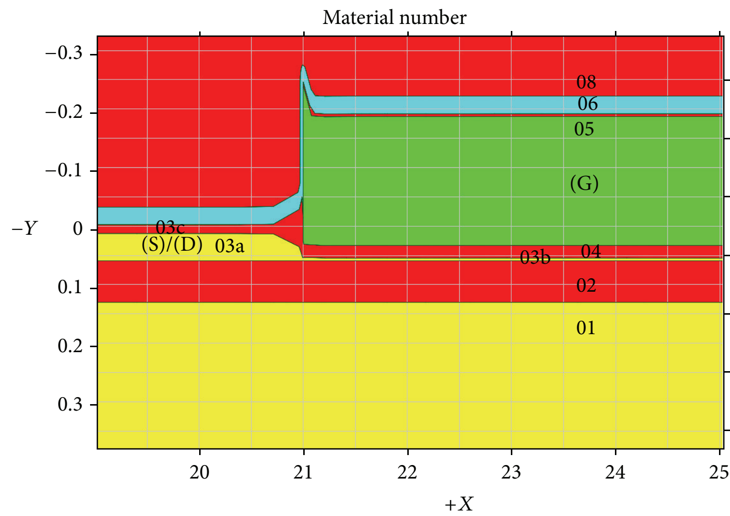


(b)

Figure 1: (a) 3D cross view and (b) 2D zoom-in of UTB (46 nm thick SOI channel) device, using TCAD process simulation. X, Y, and Z axes are in micron units



(a)



(10) Aluminum
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(D) Drain
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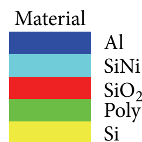

(b)

Figure 2: (a) 3D cross view and (b) 2D zoom-in of NSB device (4.6 nm thick SOI channel), using TCAD process simulation. X, Y, and Z axes are in micron units

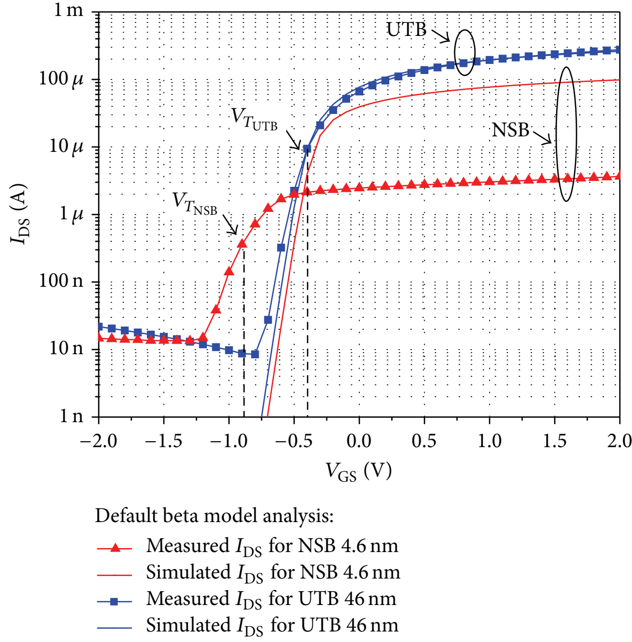

Figure 3: I_{DS}-V_{GS} transfer characteristics (semilog) measured at $V_{DS} = 0.1$ V for UTB and NSB device having a channel thickness (t_{SI}) of 46 nm and 4.6 nm, respectively, and same W/L ratio. The default beta mobility model used in the TCAD device simulator is added as an initial guess model.

model [15] for the electron mobility as described in the next paragraph.

By increasing V_{GS} from −2 V to about −1 V, I_{DS} slowly decreases, indicating a leakage phenomenon similar to the Gate Induced Drain Leakage (GIDL) observed for both classic and SOI-MOSFET devices [16]. The phenomenon is ignored in the simulation.

For V_{GS} varying from −1 V to −0.5 V, the observed increasing steep is related to the subthreshold regime. We note that the subthreshold slope is strongly degraded by decreasing the channel thickness and may be due to a poor interface quality and/or a parasitic gate capacitance induced by the gate-recessed process. In the I_{DS}-V_{GS} transfer curve, the threshold voltage (V_T) can be defined as the gate voltage for which the exponential extrapolation of subthreshold current deviates by 10% from the measured current [17]. This can be visualized by the highest point of the linear behavior in the semilog graph representation as shown in Figure 3. We preferred extracting V_T from the weak inversion region, since we argued that the strong inversion region, from which the V_T value is generally extracted, is already overwhelmed by the series resistance, for NSB device.

We note that the measured V_T value for NSB (−0.8 V) is lower than UTB's one (−0.4 V). However, for UTB's devices thinner than 10 nm typically, V_T is expected to increase by thinning the channel due to quantum effects as reported [18]. So, in our case, the V_T lowering could be rather related to a degradation of quality gate oxide that may occur during the thinning process.

3.2. Extraction of Field Dependent Mobility: Default Model versus Measurement. The TCAD device simulator (Apsys from Crosslight) uses a default field dependent mobility model, the so-called "beta" model [15], as described below for electron carrier:

$$\mu_n = \frac{\mu_{0n}}{\left(1 + \left(\mu_{0n} F / v_{sn}\right)^{\beta_n}\right)^{1/\beta_n}}, \tag{1}$$

where μ_{0n} is the low field electron mobility, F is the electrical field, v_{sn} is the electron velocity saturation, and β_n is an exponent parameter (fixed to one as a default value).

The beta model in (1) was used as an initial guess model with its defaults values. However, in order to have a better agreement with experimental result, an additional mobility reduction factor of 0.728 was used for the UTB device. This factor is reasonable since the electron mobility in SOI film is expected to be lower than in the bulk. Afterwards, the same electrical simulation without the reduction factor was simulated on the 4.6 nm thick NSB device. The simulation results are presented in Figure 3.

Since V_{DS} is fixed to 0.1 V, we can extract an *a priori* effective channel electron mobility using the following linear expression of the measured drain current:

$$\mu_n = \frac{I_{DS}}{(W/L)\, C_{ox} \left(V_{GS} - V_T\right) V_{DS}}. \tag{2}$$

This expression allows also extracting the mobility dependence of the electron mobility from the I_{DS}-V_{GS} TCAD simulations.

Figure 4 shows the dependence of the electron mobility relative to $V_{GS} - V_T$, as extracted from (2) for the NSB device and compared to UTB used for reference. We can notice a large and unexpected discrepancy between the mobility values extracted from simulation and measurement for NSB. In order to get a match for the NSB device, an outstanding reduction factor of 0.042 should be used in contrast to the 0.728 factor used for UTB. Consequently, unlike UTB, the default beta model has failed to reproduce our experimental results for NSB. Note that the split *C-V* technique, usually employed for mobility extraction, was examined in a previous study [8]. But, we found out that a large series resistance can deteriorate the *C-V* characteristics consistently with our experimental results so the channel mobility cannot be discriminated by this technique for such NSB devices.

4. Methodology for TCAD Simulations of the NSB Transfer Characteristics

4.1. Limits of TCAD Standard Simulation Models. As a first approach, the transfer characteristics of the devices were simulated by existing mobility models which are available in the TCAD toolbox.

In Figure 5, a fitting of the mobility between the simulated NSB device and experimental result was presented. Using the same default beta model given in (1) and by introducing a prefactor of 0.042, obtained from the ratio between the simulated mobility and measured mobility values of the NSB

TABLE 2: Parameter(s) value(s) of the respective standard electron mobility models. Changed value(s) correspond to a nonphysical behavior of the simulated transfer characteristics (i.e., null transconductance).

Electron mobility model	Beta (=1)	Intel 1		Intel 2		Lombardi (cgs units)			
Parameter(s)	Prefactor	E_{crit} (MV/m)	β	E_{univ} (MV/m)	α	B (10^7)	α (10^5)	β	δ (10^{14})
Default value(s)	1	4.2	0.5	57.1	1.02	4.75	1.74	0.125	5.82
Changed value(s)	0.042	4.5	1	4.0	1	4.75	1.74	0.125	0.01

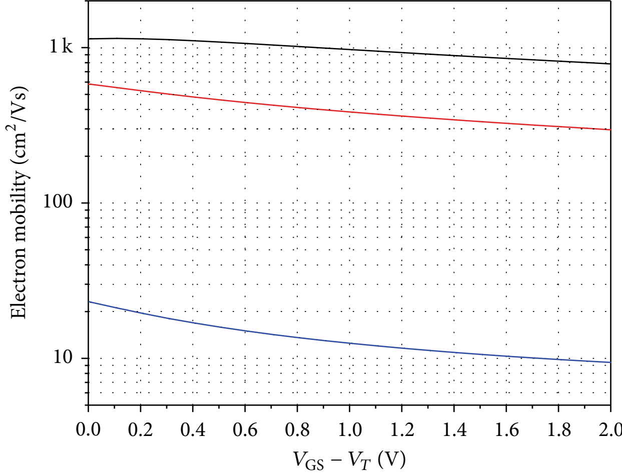

FIGURE 4: The effective electron mobility versus $V_{GS}-V_T$ relationship (semilog) extracted from the simulated transfer characteristics using the default beta model for UTB and NSB devices. For comparison the electron mobility extracted from the measurement for NSB device. V_{DS} is fixed to 0.1 V.

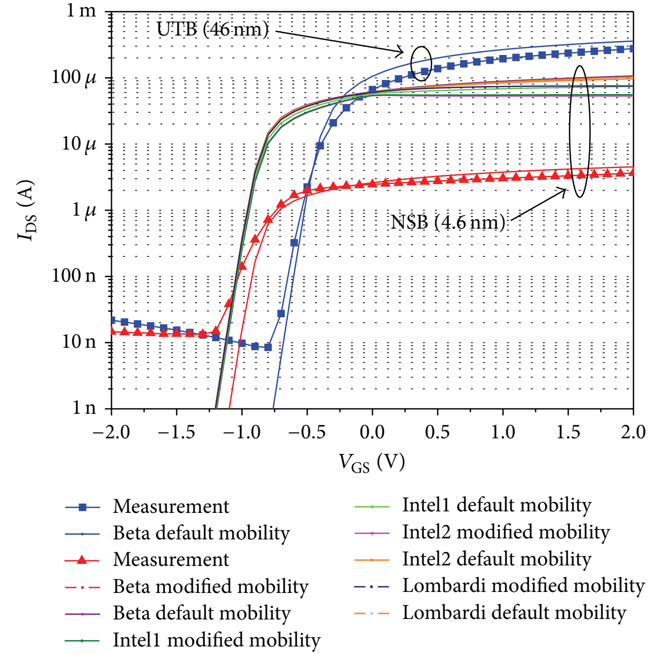

FIGURE 5: I_{DS}-V_{GS} (semilog) for experimental and simulation data. The presented NSB's I_{DS}-V_{GS} are based on all the available field dependent mobility models in TCAD device simulator. Default and changed parameters are presented in Table 2. V_{DS} is fixed to 0.1 V.

device (see Figure 4), it is possible to get good agreement with the experimental result of the 4.6 nm device for gate voltages below −0.5 V (beta modified mobility curve). Above −0.5 V, the I_{DS}-V_{GS} characteristics start to deviate from the experimental data indicating a discrepancy of the beta model. It is important to note that a prefactor was preferably used instead of manipulating the model parameters V_{sat} and β in (1).

Other existing models of mobility reduction, due to transverse field (perpendicular to the MOSFET channel), have been implemented as follows and plotted in Figure 5.

(1) The model "Intel1" based on pisces-2ET manual (Stanford University) [19] defines a factor to reduce the mobility under the channel:

$$r_{perp} = \frac{\mu}{\mu_0} = \left(1 + \frac{E_{perp}}{E_{crit}}\right)^{-\beta}, \tag{3}$$

where E_{perp} is the field perpendicular to the SiO_2/Si interface and μ_0 is bulk mobility value for electron in silicon at 300 K (1500 $cm^2 \cdot V^{-1} \cdot s^{-1}$). E_{crit} and β are the critical field and the exponent factor, respectively, indicated in Table 2.

(2) The model "Intel2" also based on pisces-2ET manual (Stanford University) defines another kind of factor to reduce the mobility under the channel according to the so-called "universal mobility curve" as follows:

$$r_{perp} = \frac{\mu}{\mu_0} = \left[1 + \left(\frac{E_{perp}}{E_{univ}}\right)^{\alpha}\right]^{-1}. \tag{4}$$

(3) A more refined model called Lombardi's model [20] proposes to integrate the contributions to mobility from different mechanisms as follows:

$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_{srf}} + \frac{1}{\mu_0}, \tag{5}$$

where μ_0 is this time of the mobility due to longitudinal field/hot-carrier effect. The other terms are due

to acoustic phonons and surface roughness defined, respectively, by

$$\mu_{ac} = \frac{B}{E_{perp}} + \frac{\alpha N^{\beta}}{\left(T_L E_{perp}{}^{1/3}\right)}, \quad (6)$$

$$\mu_{srf} = \frac{\delta}{E_{perp}{}^{2}}, \quad (7)$$

where T_L, B, and N are, respectively, the lattice temperature, velocity equivalent factor, and the average doping concentration ($10^{17}\ \mathrm{cm}^{-3}$). At room temperature, for very thin channel, the surface roughness is the dominant back-scattering mechanism (see [1, chapter 7]). So we only modified the δ parameter of the μ_{srf} component in Lombardi's model.

The mentioned models were modified to fit the NSB experimental characteristics till getting a nonphysical behavior (i.e., null transconductance, except the beta model). The corresponding parameters are shown in Table 2.

The transfer characteristics simulated using all the above models (default and modified) are added in Figure 5 for NSB device. However, except the beta model, the modified models are still presenting a discrepancy of more than one order of magnitude compared to the measurement. But even in the modified beta model the prefactor should be changed by a small factor leading to very low electron mobility for such kind of devices (less than $10\ \mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$). These results lead us to insert the series resistance influence in the transport model of the NSB device.

4.2. Application of R_{SD} versus V_{GS} Model to NSB Device. In order to describe the NSB measured transfer characteristic by the influence of a series resistance, we used the gate voltage and body thickness dependent series resistance model, presented in [8] which is considered as the access resistance ($= V_{DS}/I_{DS}$). Consider

$$R_{SD} = \frac{R^{*}_{SD0} e^{-t_{si}/t_0}}{1 + \theta^{*} V_{GS}/t_{si}}, \quad (8)$$

with $R^{*}_{SD0} = 4.54\ \mathrm{M\Omega}$, $t_0 = 1.03\ \mathrm{nm}$, and $\theta^{*} = 1.1\ \mathrm{nm{\cdot}V^{-1}}$.

A resistance extraction was made for $t_{SI} = 4.6\ \mathrm{nm}$ and gate voltages between −0.5 and 2V and shown in Figure 6.

4.3. Influence of R_{SD} on the Simulated Transfer Characteristics. The I_{DS}-V_{GS} was simulated using the field dependent beta model without the reduction mobility factor of 0.042. The series resistance can be included in the TCAD device simulator as an external lumped element but for a fixed value of V_{GS}. Thus we simulated I_{DS}-V_{GS} characteristics for each extracted resistance values in the range of −0.5 V to 2 V with 0.5 V steps (six different values according to Figure 6). The influence of the R_{SD} voltage dependence on I_{DS}-V_{GS} can be simulated by a postprocessing of the above simulated characteristics which is shown in Figure 7. Indeed, for a given I_{DS}-V_{GS} curve corresponding to a R_{SD} given for a particular V_{GS}, for example, −0.5 V, the current value is sampled at this particular voltage V_{GS}. The process is then repeated for each I_{DS}-V_{GS} curve at the V_{GS} value corresponding to the next R_{SD} step value. The reconstructed I_{DS}-V_{GS} characteristic from the sampled I_{DS} values is shown as the graph with triangle symbols in Figure 7.

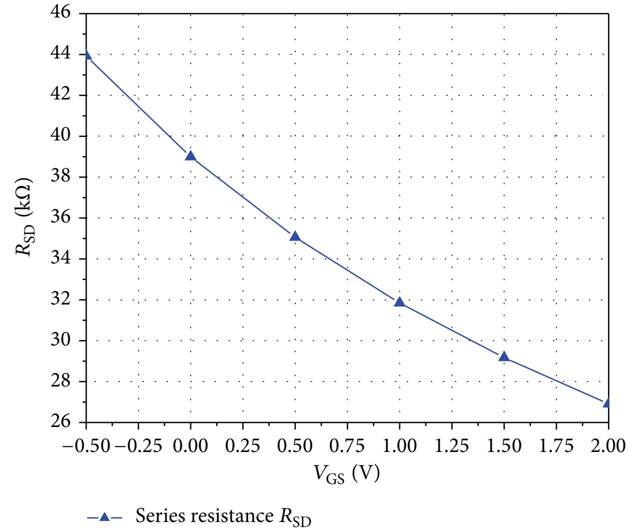

Figure 6: R_{SD} versus V_{GS} relation for NSB with 4.6 nm channel thick given by (8).

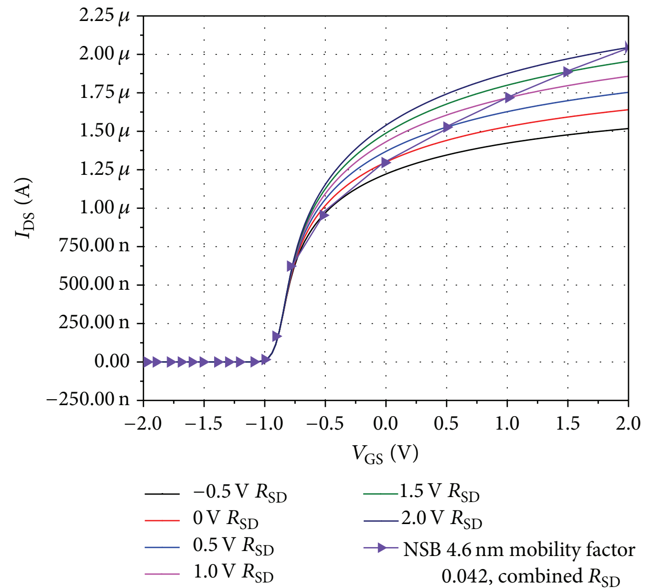

Figure 7: The variation of simulated I_{DS}-V_{GS} for each extracted resistance values in the range of −0.5 V to 2 V with 0.5 V steps. V_{DS} is fixed to 0.1 V.

In Figure 8, we compare our reconstructed characteristic from Figure 7 (now called $I_{DS,sim,RSD}$) to the measured one and to the simulated one from the beta model with the reduction mobility factor of 0.042 only ($I_{DS,sim}$). While the latter is higher than the measured characteristic, it appears that reconstructed one is now lower. Mobility reduction and

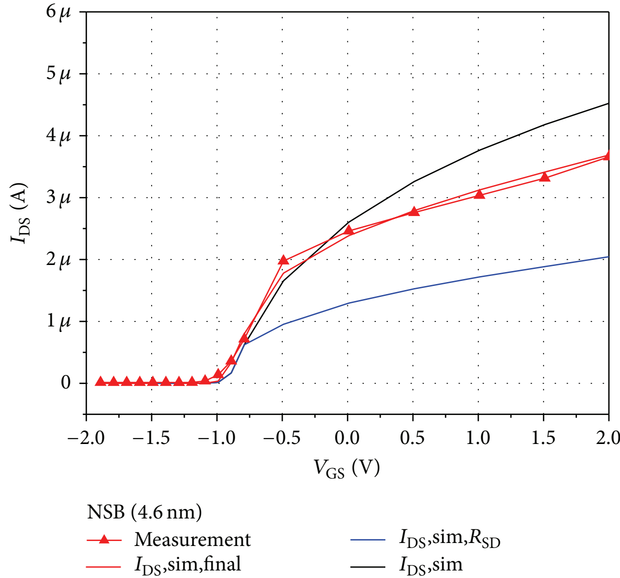

FIGURE 8: Simulated I_{DS}-V_{GS} data including the resistance in series to the drain terminal compared to the measured one for NBS device. An exponent value of 0.93 in (9) gave the best fit to measurement. V_{DS} is fixed to 0.1 V.

series resistance effect are in competition to reduce the drain current but each of them is dominating in a particular range of V_{GS} values (below −0.5 V and above −0.5 V, resp.). Consequently we suggest unifying both simulated characteristics to simulate the final current $I_{DS,sim,final}$ according the following equation inspired from Matthiessen's mobility-like law:

$$I_{DS,sim,final} = \left(\frac{I_{DS,sim} I_{DS,sim,RSD}}{I_{DS,sim} + I_{DS,sim,RSD}} \right)^n . \quad (9)$$

It was found that an exponent value of $n = 0.93$ gave the best fit to the experimental characteristics, as it is presented in Figure 8.

5. Conclusion

Nanoscale SOI-MOSFET devices were fabricated using a selective recessed gate thinning process to get channel thicknesses scaling from 46 nm down to 4.6 nm. We show that the anomalous degradation of electrical characteristics of the latter can be modeled by a gate controlled series resistance rather than merely by a mobility model. Using TCAD tools, the devices' transfer characteristics were simulated using the series resistance model combined with a factorized mobility model. Based on simulation results, it could be better understood that for low gate voltage the degraded electron mobility may be the dominant factor while at high gate voltage the series resistance becomes the dominant factor. Among various tested mobility models we have found out that the best fit is obtained when combining the modified beta mobility model with the gate voltage dependent series model. We suggest that this semiempirical modeling approach may be useful as a TCAD embedded tool to model the behavior of other nanodevices for which series resistance and/or mobility degradation is of a great concern.

Conflict of Interests

The authors have no conflict of interests associated with this paper.

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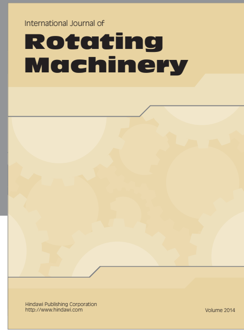
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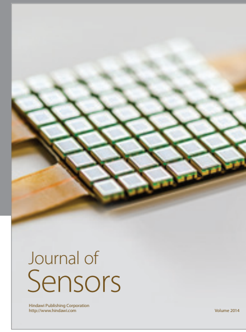
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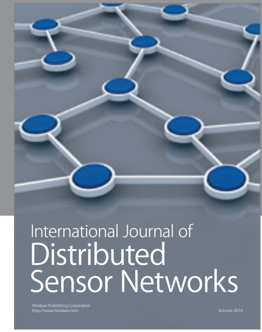
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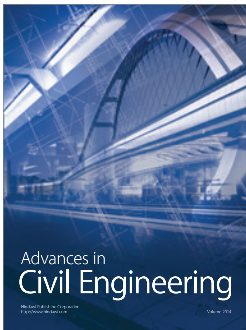
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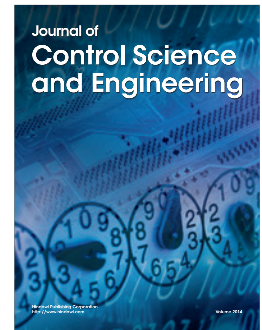
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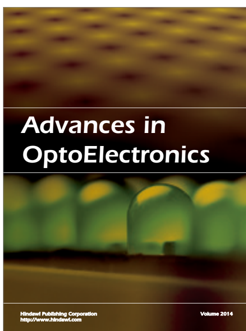
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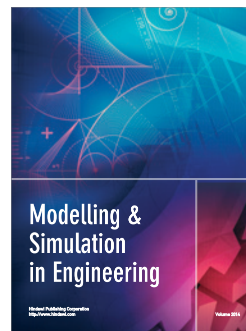
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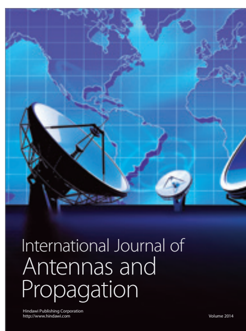
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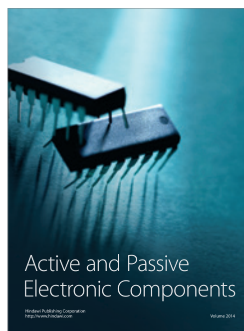
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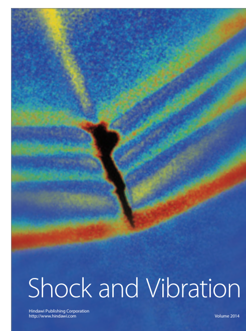
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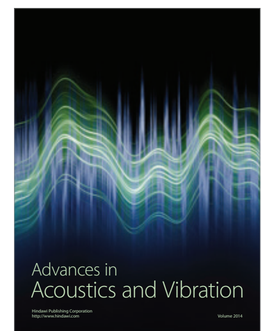
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