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Research Article

Anomalous DIBL Effect in Fully Depleted SOI MOSFETs Using Nanoscale Gate-Recessed Channel Process

Avi Karsenty[1] and Avraham Chelly[2]

[1]*Applied Physics/Electro-Optics Department, Faculty of Engineering, Lev Academic Center, 21 Havaad Haleumi Street, 9116001 Jerusalem, Israel*
[2]*Advanced Semiconductor Devices Lab, Faculty of Engineering, Bar-Ilan University, 52900 Ramat Gan, Israel*

Correspondence should be addressed to Avi Karsenty; karsenty@jct.ac.il

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Nanoscale Gate-Recessed Channel (GRC) Fully Depleted- (FD-) SOI MOSFET device with a silicon channel thickness (t_{Si}) as low as 2.2 nm was first tested at room temperature for functionality check and then tested at low temperature (77 K) for I-V characterizations. In spite of its FD-SOI nanoscale thickness and long channel feature, the device has surprisingly exhibited a Drain-Induced Barrier Lowering (DIBL) effect at RT. However, this effect was suppressed at 77 K. If the apparition of such anomalous effect can be explained by a parasitic short channel transistor located at the edges of the channel, its suppression is explained by the decrease of the potential barrier between the drain and the channel when lowering the temperature.

1. Introduction

The Drain-Induced Barrier Lowering (DIBL) effect is a well-known phenomenon, which was reported in different types of nanoscale devices, such as in classical short-channel MOSFET devices [1] and recently in long-channel Carbon Nano Tubes (CNT) devices [2].

The DIBL effect was mainly reported in short channel structures. The classical described root cause is that the channel formation is not entirely done by the gate, but now the drain and source also affect the channel formation. As the channel length decreases, the depletion regions of the source and drain come closer together and make the threshold voltage (V_T) a function of the length of the channel. This is called V_T roll-off. V_T also becomes function of drain to source voltage V_{DS}. As we increase V_{DS}, the depletion regions increase in size and a considerable amount of charge is depleted by V_{DS}. The gate voltage required to form the channel is then lowered, and thus, V_T decreases with an increase in V_{DS}. This effect is called Drain-Induced Barrier Lowering.

In this paper, we report the evidence of an anomalous DIBL effect in nanoscale n-type FD-SOI MOSFET with a Gate-Recessed Channel (GRC) thickness of 2.2 nm and a long channel W/L ratio of 80/3 [μm]. Moreover, if the effect was anomalously observed at room temperature (RT) of 300 K, it completely disappeared at low temperature (LT) of 77 K. A COMSOL Multiphysics simulation picture of the device channel is shown in Figure 1. Further details about such kind of devices can be found in previous published work [3]. The initial SOI thickness before gate recess processing of the gate was 50 nm. The buried oxide (BOX) thickness is 70 nm. The gate oxide (GOX) thickness is 26 nm.

2. Experimental Results and Analysis

2.1. Room Temperature Measurements. The transfer (I_{DS}-V_{GS}) characteristics of the n-type FD-SOI MOSFET were measured at room temperature (300 K) and shown in Figure 2 in a semilog scale for several V_{DS} voltages (1, 2, 3, and 4 V).

For each V_{DS} value, the threshold voltage is extracted from the end of the weak inversion domain of the transfer characteristic for a given threshold current fixed here at 1 μA. The extracted values range stands between −1 V and −0.5 V and is linearly decreasing (in relative value) with V_{DS}, indicating Drain-Induced Barrier Lowering (DIBL) effect as shown in Figure 3.

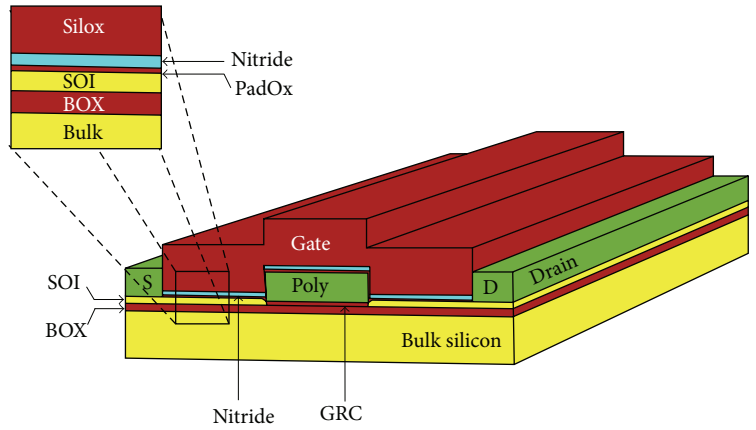

FIGURE 1: COMSOL 3D view of the GRC device is presented, showing a channel thickness of 2.2 nm. Scale $X : Y$ ratio is 100 : 1.

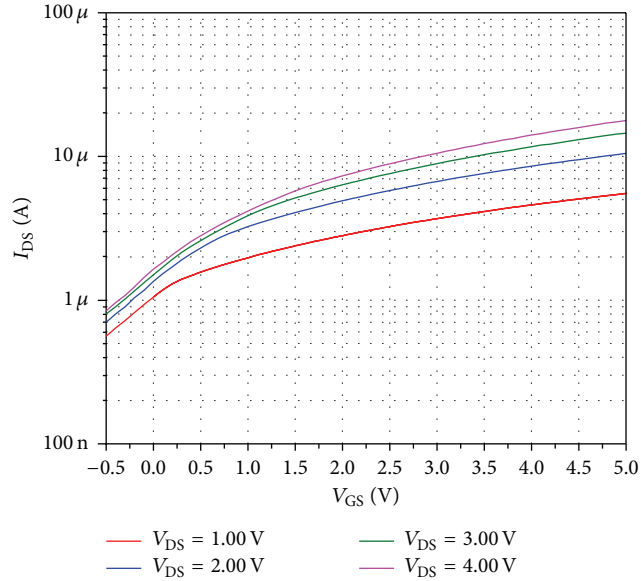

FIGURE 2: Transfer characteristics I_{DS} versus V_{GS} for GRC device with specifications: t_{Si} = 2.2 nm and W/L = 80 μm/3 μm, T = 300 K.

The intercept value at zero V_{DS} is 0.02 V, indicating that the device is almost depletion type (normally on). The DIBL coefficient σ as extracted from the slope of a linear fit of the Figure 3 is −104 mV/V. Such a DIBL effect is at a first glance surprising here since the length of the channel is relatively high (L = 3 μm) and the channel is ultrathin (t_{Si} = 2.2 nm) with a relatively small gate oxide thickness (t_{ox} = 26 nm). Indeed, these conditions should prevent such effect as expected for FD-SOI MOSFETs [4, 5]. Indeed, the design rule for the channel length to avoid Short Channel Effects (SCE) like DIBL in a planar SOI-MOSFET is given by the following equation:

$$L \gg \lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}} = 13\,\text{nm}. \quad (1)$$

For a FD-SOI MOSFET [6], a correction factor should be applied to the previous equation which turns to

$$\lambda_{FD} = \lambda \sqrt{\frac{C_{fbb}}{\eta C_{box}}}, \quad (2)$$

where

$$\frac{1}{C_{fbb}} = \frac{1}{C_{box}} + \frac{1}{C_{fox}} + \frac{1}{C_b} \quad (3)$$

C_{box} is the buried oxide capacitance (ε_{ox}/t_{box}), C_b is the channel body capacitance (ε_{Si}/t_{Si}), and C_{fox} is the front gate capacitance (ε_{ox}/t_{ox}). η is the factor which depends on the substrate doping value and silicon thickness and is taken as 1 for very thin body channel [7]. According to our device's parameters λ_{FD} is now 11 nm which is not a significant change relatively to the planar SOI MOSFET.

2.2. Low Temperature (77 K) Measurements. The same transfer characteristics I_{DS}-V_{GS} for several V_{DS} voltages (1, 2, 3, and 4 V) were measured at 77 K and are shown in Figure 4 in a semilog scale. The drain current is reduced to about 60 times relatively to RT.

The extracted threshold voltage (V_T) for a threshold current of 10 nA is now almost independent of V_{DS} and is fixed to about −0.1 V +/− 0.1 V, meaning that the DIBL effect

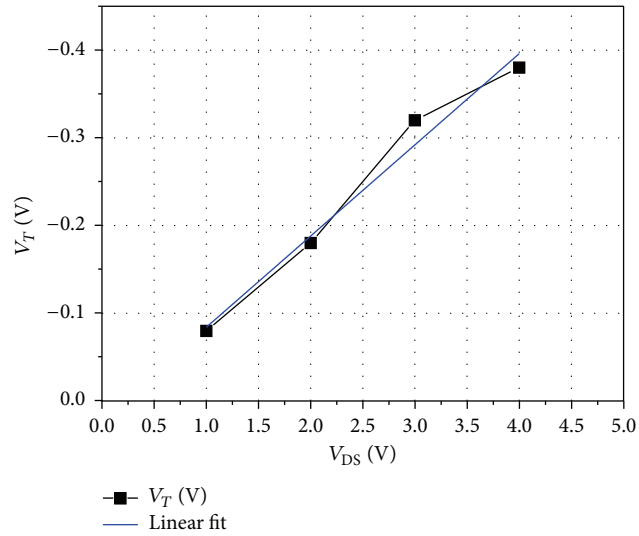

FIGURE 3: Linear variation of V_T extracted from Figure 2 as a function of V_{DS} showing the DIBL effect at 300 K.

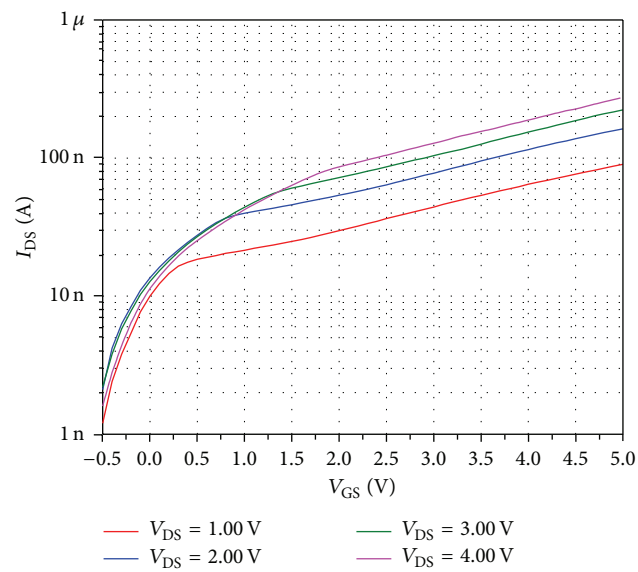

FIGURE 4: Transfer characteristics I_{DS} versus V_{GS} for GRC device with following specifications: t_{Si} = 2.2 nm and W/L = 80 μm/3 μm, T = 77 K.

is suppressed by lowering the temperature. It turns also out that V_T is weakly decreased by lowering the temperature from 300 K to 77 K. This result is also surprising since it is expected that V_T is increased, like the Fermi potential should, by lowering the temperature for n-FD-SOI MOSFET according to [5].

By confining the channel to very thin silicon, we should expect a quantization of the threshold voltage. Indeed, when the channel becomes very thin, V_T will increase due to the quantum shift of the ground state energy which is inversely proportional to the square of the Si thickness like a 1D quantum well. It has been shown [8] that the uncertainty of the threshold voltage (σ_{V_T}) due to quantum fluctuations is given by

$$\sigma_{V_T} = -\frac{\hbar^2\pi^2}{em^* t_{Si}^3}\sigma_{t_{Si}}, \tag{4}$$

where $\sigma_{t_{Si}}$ is the channel thickness uncertainty (taken as 10% of t_{Si}, i.e., 0.2 nm), e is the elementary charge, and m^* is the effective mass of the first subband. In our case, σ_{V_T} is found to be as low as 15 mV which is well below the experimental error.

3. Interpretation

We propose to interpret the previous experimental observations at 300 K and 77 K as follows.

3.1. Room Temperature. For a FD SOI MOSFET device the DIBL coefficient σ can be modeled by the following equation [6, 7]:

$$\sigma = \frac{dV_T}{dV_{DS}} = \frac{C_{bb}}{C_{fbb}}\left(e^{-L_{eff}/2\lambda_{FD}} + 2e^{-L_{eff}/2\lambda_{FD}}\right) \tag{5}$$

with

$$\frac{1}{C_{\text{bb}}} = \frac{1}{C_{\text{box}}} + \frac{1}{C_b}. \quad (6)$$

According to our device's parameters, $C_{\text{bb}}/C_{\text{fbb}} = 1.37$ and by solving the previous equation numerically, we can compute the value of the effective channel length ($L_{\text{eff}} = 81$ nm) of the device corresponding to the extracted value of ($\sigma = 104$ mV/V).

Since the field can penetrate the channel from drain and source through the buried oxide (BOX) and substrate, another term should be added to the DIBL coefficient σ defined in (5). This is called drain-induced virtual substrate biasing (DIVSB) [7] and is given by

$$\text{DIVSB} = \frac{C_{\text{BD}}(0)\, C_b}{C_{\text{fox}}\left(C_{\text{BD}}(0) + C_b\right)}, \quad (7)$$

where $C_{\text{DB}}(0)$ is the drain to body capacitance taken at the middle of the channel. Since the body channel is very thin (2.2 nm) the C_b term is dominating such that the DIVSB is close to the $C_{\text{DB}}(0)/C_{\text{fox}}$ ratio. $C_{\text{DB}}(0)$ is given by the following [7]:

$$C_{\text{BD}}(0) = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}\left(e^{\pi L/2t_{\text{box}}} - 1\right)}. \quad (8)$$

If we take into account the additional DIVSB term to calculate the new effective channel length, we would get a value of 83 nm which is not a significant change relatively to the former value of 81 nm. Indeed, for our long channel device, $L/t_{\text{box}} = 3000/70$, so $C_{\text{DB}}(0) \sim 0$ and then DIVSB ~ 0.

We can conclude that this device behaves like a SOI-MOSFET sharing an effective channel length of about 80 nm. This can be described like a parasitic transistor located in the vicinity of the channel edges below the gate which overwhelms the behavior of the expected long channel SOI-MOSFET device.

3.2. Low Temperature. On one hand, the decrease of the current at low temperature may be due to a freezing effect of the doping charge that in turn increases the series resistances located at the drain and source to channel contacts as reported in a similar device [3].

On the other hand, it is well known that operating at low temperatures reduces SCE like DIBL does [9]. Indeed, in order to sustain a given subthreshold current level, which is proportional to $e^{-q\Delta\varphi/kT}$, the potential barrier $\Delta\varphi$ between the source and the surface channel is lowered by decreasing the temperature. The potential barrier will then be less sensitive to the lateral electric field into the channel, and charge sharing effects near the surface will be reduced at low temperature. Moreover, this may explain our experimental decreasing of V_T by lowering the temperature.

Finally, if we consider the influence of quantum confinement, as well as the temperature dependence of the effective density of states for channel thickness thinner than 10 nm [10], it has been shown that SCE should be enhanced at low temperature in opposition to the classic behavior mentioned above. So, this may confirm that the observed SCE is not connected to the quantum well confinement of the channel but rather to a classic short channel parasitic n-SOI MOSFET having at least 10 nm thickness.

4. Conclusion

Anomalous DIBL effect at 300 K and its suppression at 77 K are observed for ultrathinned Fully-Depleted Silicon-On-Insulator (FD-SOI) MOSFETs fabricated by GRC process. These trade-off phenomena are interpreted by the apparition of a dominating short channel transistor near the edges of the recessed channel and by the lowering of the potential barrier when decreasing the temperature. Such phenomena may occur in other low dimensional devices where source and drain contacts are separated from the channel by an extension region at both sides.

Conflict of Interests

The authors have no conflict of interests associated with this paper.

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