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Research Article

On the Evaluation of Gate Dielectrics for 4H-SiC Based Power MOSFETs

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This work deals with the assessment of gate dielectric for 4H-SiC MOSFETs using technology based two-dimensional numerical computer simulations. Results are studied for variety of gate dielectric candidates with varying thicknesses using well-known Fowler-Nordheim tunneling model. Compared to conventional SiO_2 as a gate dielectric for 4H-SiC MOSFETs, high-k gate dielectric such as HfO_2 reduces significantly the amount of electric field in the gate dielectric with equal gate dielectric thickness and hence the overall gate current density. High-k gate dielectric further reduces the shift in the threshold voltage with varying dielectric thicknesses, thus leading to better process margin and stable device operating behavior. For fixed dielectric thickness, a total shift in the threshold voltage of about 2.5 V has been observed with increasing dielectric constant from SiO_2 ($k = 3.9$) to HfO_2 ($k = 25$). This further results in higher transconductance of the device with the increase of the dielectric constant from SiO_2 to HfO_2. Furthermore, 4H-SiC MOSFETs are found to be more sensitive to the shift in the threshold voltage with conventional SiO_2 as gate dielectric than high-k dielectric with the presence of interface state charge density that is typically observed at the interface of dielectric and 4H-SiC MOS surface.

1. Introduction

Power semiconductors provide basic building block in almost all energy conversion, transmission, and distribution networks used today. From system design point of view, semiconductor devices that enable reduced power losses, provide higher power density, facilitate compact converter design, and simultaneously bring lower overall system cost will be considered key technological booster for very high power applications. With power electronics reliability consideration in mind, semiconductor devices [1–10] are also evaluated for high power applications that demand harsh environment [3, 4, 9]. Recently, silicon carbide (SiC) material has gained substantial interest as a promising candidate for high power and high temperature applications. Compared to conventional Si material (used today for standard CMOS and for variety of high power applications ranging from 25 to 125°C), silicon carbide is a wide bandgap material (i.e., 3 times than that of Si) having larger thermal conductivity values (i.e., 3 times than that of Si) and larger breakdown field strength (i.e., 10 times than that of Si) and offers larger carrier saturation velocity (i.e., 2 times than that of Si). Because of these unique features, SiC material is well blessed for high power devices [10–20] for applications ranging from −75 up to 550°C [4].

Silicon carbide based semiconductor devices such as Schottky diodes [3], junction field effect transistors (JFETs) [8, 9], bipolar junction transistors (BJTs) [4–7], metal oxide semiconductor field effect transistors (MOSFETs) [11–15], insulated gate field effect transistors (IGBTs) [16–20], and integrated gate commutated thyristors (IGCTs) [10] are explored today as potential candidates to meet the growing demand from the point of view of power system compactness that offer increased power density and simultaneously reduced overall system losses. While significant progress at material and device level research has been made and resulted in commercialization of some of these devices, reliability concern has been raised either in the passivation process for BJTs/JFETs [7, 8] or in gate dielectric process for MOSFETs/IGBTs [11–20] that may present one limiting factor for reliable performance of these devices in real applications. Note that most of these devices use silicon dioxide (SiO_2) as a passivation layer protecting the device surface or as gate

dielectric process. While SiC can be thermally oxidized to yield SiO_2 over its surface, a fundamental inherent drawback of SiO_2 is its low dielectric constant, which is about 2.5 times lower than that of the SiC material and also possesses poor interface properties at the SiO_2/SiC junction. This leads to proportionally a larger electric field enhancement in the dielectric medium compared to that in the semiconductor layer underneath, which is a reason why new dielectrics with dielectric constant at least similar to that of the SiC material and with lower interface state densities are required for device applications. Note that this inequality of dielectric constant often requires device operation at an electric field far below the SiC material breakdown field in order to avoid premature SiO_2 breakdown at the device surface. The performance of these SiO_2/SiC interfaces for MOSFETs (and for BJTs as well) has been improved by various oxidation [21, 22] or nitridation methods [21, 22], but their realistic commercialization potential still remains limited by a low channel mobility due to a high interface state density near the conduction band. Generally speaking, the density of interface states (D_{it}) at the SiO_2/SiC interface is at least two to three orders of magnitude higher ($\sim 10^{12}$ eV^{-1} cm^{-2}) [23–26] compared to the relatively matured Si/SiO_2 interface.

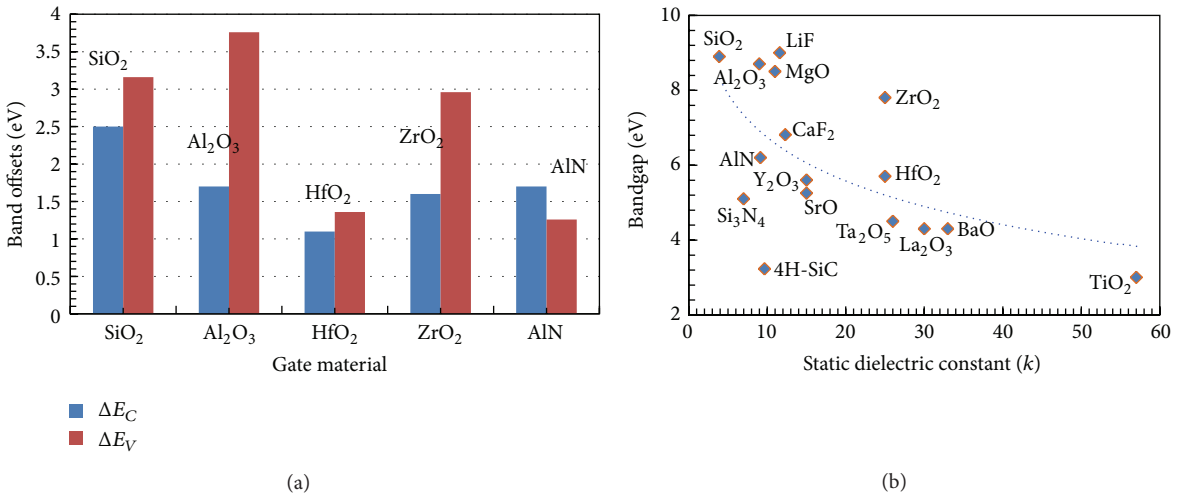
To overcome the abovementioned problems associated with SiO_2 on SiC, potential of various high-k gate dielectrics (e.g., Al_2O_3, HfO_2, AlN, La_2O_3, Y_2O_3, Al_2O_3, and Ta_2O_5) [27–43] is being explored recently for SiC MOS technology. Among them, Al_2O_3 is getting more attention as potential substitute for SiO_2 primarily due to its excellent lattice matched with SiC, its compatible high-k value with 4H-SiC, good thermal stability, reasonably high conduction band offset between 4H-SiC and Al_2O_3, and relatively large dielectric bandgap. Similarly, HfO_2 is considered another interesting candidate for 4H-SiC MOS devices due to its high-k value. However, its bandgap is relatively small compared to SiO_2 or Al_2O_3 gate dielectric. Utilizing high-k value dielectric but with problem of its low bandgap, this issue is being addressed by inserting a sandwiched layer of SiO_2between HfO_2 and 4H-SiC [35, 43, 44] or between Al_2O_3 and 4H-SiC [36, 38, 40, 41]. On the other side, a significant reduction in leakage current density has been observed in high-k La_2O_3 structure (i.e., smaller bandgap than that of SiO_2) when a 6 nm thick thermal nitrided SiO_2 has been inserted between La_2O_3 and SiC [45]. Recent device performance of using high-k gate dielectric for 4H-SiC based MOSFETs [38–41] shows overall good progress for future SiC device commercialization.

Similar to conventional low power devices using high-k gate dielectric over Si, one of the major challenges is the significantly lower channel mobility for the SiC-MOSFETs due to high interface state density and interface surface roughness through scattering and trapping effects for the carriers at SiO_2/SiC interface. This surface roughness also poses threat to the gate oxide reliability and further leads to instability of the threshold voltage. While for matured SiO_2/Si interface channel mobility lies close to the universal mobility curve, mobility for high-k gate dielectric interface with Si lies well below the universal curve and the real cause is not well understood yet [25]. Channel mobility values of SiC MOSFETs with thermally grown SiO_2 as gate dielectric present unacceptably low value of 10 cm^2/V·s due to high density of interface traps [12, 13]. Postoxidation annealing of the gate oxide under NO/N_2O (nitric/nitrous oxide) [14] and $POCl_3$ [15] environment helps to further improve this value to 50 [32] and 89 cm^2/V·s [15], respectively. A record peak channel mobility of 150 cm^2/V·s has also been reported after performing oxidation process in the presence of alumina [11] for SiO_2/SiC interface based MOSFETs. More recently, the improvement of channel mobility over 100 cm^2/V·s using combined "Sb + NO" process which is associated with the dual mechanisms of counterdoping by Sb (i.e., antimony) and interface trap passivation by NO has been reported [46] for 4H-SiC MOSFETs. Ultrahigh channel mobility has been demonstrated for 4H-SiC-MOSFETs with Al_2O_3 gate insulators fabricated at low temperatures by metal-organic chemical-vapor deposition [38]. Relatively high field effect channel mobility of 64 cm^2/V·s is obtained when Al_2O_3 gate insulator is deposited at 190°C. Furthermore, extremely high field effect mobility of 284 cm^2/V·s was obtained for a MOSFET fabricated with an ultrathin thermally grown SiO_x layer inserted between the Al_2O_3 and SiC [38]. Yet, in another investigation, the same group [38, 40] has demonstrated a remarkable increase in the channel mobility by inserting a thin SiO_2 layer (1-2 nm) between Al_2O_3 and SiC [41]. A maximum channel mobility in stacked dielectric of Al_2O_3/SiO_2/SiC based MOSFETs as high as 300 cm^2/V·s was reported using low deposition temperature of the gate-insulator film. Note that three positive outcomes as reported in the scientific literature [35–43] are generally expected using thin SiO_2 layer between high-k material and SiC surface underneath; namely, (i) thin layer of SiO_2 acts as a barrier layer against unwanted chemical reaction with the SiC substrate during high-k growth, (ii) interface state density should be lower than that of growing high-k material directly over SiC surface, and (iii) inserted SiO_2 layer would further reduce the effect of Coulomb scattering from the fixed charges present in the high-k film. All in all, these preliminary findings using high-k stacked dielectric [35–43] present a fair advancement in SiC MOSFET technology development through reduction in the interface state density (D_{it}) compared to pure SiO_2/SiC interface.

A list of various dielectrics [23–26, 44, 45] and their physical properties is illustrated in Table 1. Figure 1 shows the analytical trend of the bandgap energy as a function of the dielectric constant of the material [23–25, 44, 45]. Note that the energy bandgap of dielectric material has a direct correlation with the gate leakage current through the conduction band edge offset values where a wider bandgap energy of dielectric material means a better chance for getting larger conduction (ΔE_C) or valence band (ΔE_V) offsets at the interface of semiconductor and the gate dielectric. Interestingly, lower conduction band offsets are predicted with respect to dielectric material due to smaller bandgap difference at the interface of dielectric and SiC compared to Si material counterpart as shown in experimentally extracted values from the literature [23, 24, 44] in Table 1. It is therefore objective of this work to investigate various dielectrics that can be employed as a potential candidate for 4H-SiC based

Table 1: List of physical properties of various dielectric materials reported in the literature.

Material	Dielectric constant (k)	Bandgap E_g (eV)	ΔE_C (eV) with respect to Si	ΔE_C (eV) with respect to 4H-SiC	Structure	Preparation method
SiO_2	3.9	8.9	3.2	2.2–2.7	Amorphous	Thermal, PECVD
Si_3N_4	7.0	5.1	2.0	—	Amorphous	Thermal, LPCVD, MOCVD
SiON	4.0–7.0	5.0–9.0 (O/N ratio)	2.8	—	Amorphous	Thermal, PECVD
Al_2O_3	9.0	8.7	2.8	1.7	Amorphous	Sputtering, ALCVD
HfO_2	25	5.7	1.5–1.7	0.54 and 0.7–1.6	Mono, tetra, cubic	Sputtering, ALCVD
ZrO_2	25	7.8	1.4	1.6	Mono, tetra, cubic	ALCVD
Ta_2O_5	26	4.5	1–1.5	—	Orthorhombic	MOCVD
Y_2O_3	15.0	5.6	2.3	—	Cubic	—
La_2O_3	30	4.3	2.3	—	Cubic	—
AlN	9.14	6.2	2.2	1.7	Wurtzite	MOCVD



(a) (b)

Figure 1: Conduction band (ΔE_C) and valence band (ΔE_V) offsets of various dielectrics with respect to 4H-SiC material (a) and bandgap energy (E_g) as a function of dielectric constant (k) of various materials reported in the literature (b).

MOSFETs. Influence of dielectric constants, dielectric thicknesses, and interface state densities has been studied using two-dimensional numerical computer simulation.

2. Device Simulation Setup

A schematic cross sectional view of the simulated 4H-SiC based MOSFET device along with the net doping profile is shown in Figure 2. For simplicity, only left half of the device with horizontal dimension of 4 μm is simulated with a channel length of 0.8 μm. A drift layer thickness of 25 μm with a doping concentration 5×10^{14} cm^{-3} is used to get a hypothetical device of blocking voltage of at least 1700 V. Device simulation was executed by considering bandgap narrowing model [47], Auger recombination model [47], Shockley-Read-Hall (SRH) recombination [47], doping and temperature dependent field mobility models [47], and incomplete ionization model [47]. In addition, all the simulations were carried out using Fermi Dirac statistics. The used physical models (e.g., bandgap, incomplete ionization, mobility model, and carrier lifetime) and their parameters in this work have earlier been applied for 4H-SiC devices [6, 19, 20, 28]. The total number of mesh points was 40,000 while mesh resolution at the surface interfaces and p-n junction areas was 0.2-0.3 nm. The material parameters used in present simulations are listed in Tables 2 and 3 and have earlier been used and verified in previous simulation papers for 4H-SiC BJT [5–7] and 4H-SiC IGBT [19, 20] devices. The carrier lifetime in different regions of the device was simulated

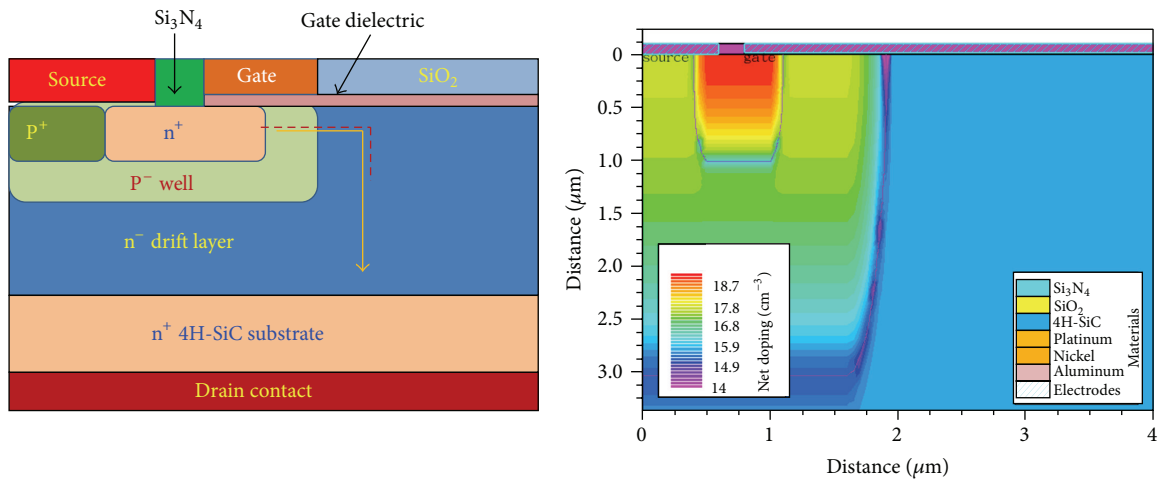


Figure 2: A schematic cross section of simulated device layer structure (a) and corresponding net doping profile showing top portion of 4H-SiC based MOSFET (b).

Table 2: Parameters used in 4H-SiC based MOSFET device simulation.

Eg_{300} (eV)	3.24	Bandgap at 300 K
Eg_{alpha} (eV/K)	4.15×10^{-4}	Parameter of bandgap model
Eg_{beta} (eV/K)	−131	Parameter of bandgap model
Permittivity	9.66	Permittivity
Affinity (χ)	4.2	Affinity
A_{UGN} (cm^6/s)	5×10^{-32}	Auger recombination parameter for electrons
A_{UGP} (cm^6/s)	2×10^{-32}	Auger recombination parameter for holes
Ea_b (eV)	0.2	Acceptor energy level
Ed_b (eV)	0.1	Donor energy level
Gv_b (eV)	4	Degeneracy factor for valence band
Gc_b (eV)	2	Degeneracy factor for conduction band
LT.TAUN	5	Lifetime model parameter for electrons
LT.TAUP	5	Lifetime model parameter for holes
N_{srhn} (cm^{-3})	3×10^{17}	SRH concentration-dependent lifetime for electrons
N_{srhp} (cm^{-3})	3×10^{17}	SRH concentration-dependent lifetime for holes
A_{RICHN} ($A/K^2\,cm^2$)	110	Effective Richardson constant for electrons
A_{RICHP} ($A/K^2\,cm^2$)	30	Effective Richardson constant for holes

by considering doping and temperature dependent carrier lifetime model [6, 20]:

$$\tau_{n,p} = \frac{\tau_{max,n,p}(T/300)^{1.72}}{1 + \left(N/\left(3 \times 10^{17}\right)\right)^{0.3}}. \quad (1)$$

A wide spread in the band offset values of various dielectric materials with respect to 4H-SiC has been reported in the literature [21–27, 44, 45]. For few potential high-k dielectric materials (e.g., see Table 1), the band offset values with respect to 4H-SiC material are still unknown. In present simulation, the electron affinity values were adjusted to get the right conduction band offsets of respective dielectric material equivalent to its experimentally extracted value with respect to 4H-SiC. For example, experimentally extracted values of ΔE_C of 2.5, 1.7, 1.1, 1.6, and 1.7 eV are used in present simulations for SiO_2, Al_2O_3, HfO_2, ZrO_2, and AlN material, respectively, that correspond to 44, 31, 45, 35, and 57%, respectively, of the bandgap difference of the respective dielectric with respect to 4H-SiC. Since ΔE_C of few dielectrics (e.g., Si_3N_4, Y_2O_3, and La_2O_3) is still unknown, 50% of the bandgap difference has been associated with conduction band, which is almost similar but closer to other known dielectric materials (e.g., SiO_2, HfO_2).

Note that time dependent dielectric breakdown (TDDB) in power semiconductor devices is considered a potential reliability concern for dielectric layers. Since Si and SiC based MOS devices generally use SiO_2 as a gate dielectric, the resultant barrier height and conduction band offset difference between SiC and SiO_2 is fairly smaller than that

Table 3: Mobility parameters used in 4H-SiC based MOSFET device simulation.

μ_{1n}.caug	40	$cm^2/V{\cdot}s$
μ_{2n}.caug	950	$cm^2/V{\cdot}s$
ncrn.caug	2×10^{17}	cm^{-3}
δ_n.caug	0.73	Arbitrary
γ_n.caug	−0.76	Arbitrary
α_n.caug	0	Arbitrary
β_n.caug	−2.4	Arbitrary
μ_{1p}.caug	53.3	$cm^2/V{\cdot}s$
μ_{2p}.caug	105.4	$cm^2/V{\cdot}s$
N_{critp}.caug	2.2×10^{18}	cm^{-3}
δ_p.caug	0.7	Arbitrary
γ_p.caug	0	Arbitrary
α_p.caug	0	Arbitrary
β_p.caug	−2.1	Arbitrary
v_{satn}	2×10^7	cm^2/s
v_{satp}	2×10^7	cm^2/s
β_n	2	—
β_p	1	—

of Si counterpart [29–32]. This leads to higher tunneling current in 4H-SiC/SiO_2 based MOS system than that in Si/SiO_2based MOS devices. For thick gate oxides (>5.0 nm), Fowler-Nordheim (FN) tunneling mechanism has been suggested to contribute to dielectric breakdown, particularly at high electric fields. Since FN tunneling has earlier been used to characterize SiC based MOS capacitors [23, 29, 30, 32, 45] with thick dielectric layers (5–50 nm), the present work therefore takes into account FN tunneling model for various dielectric assessment. Direct tunneling through the dielectric has therefore been ruled out in this work since it dominates for very thin dielectrics (<3 nm) where the tunneling current increases exponentially with reduction in the oxide thickness. The Fowler-Nordheim current density equation that represents the tunneling current through the gate dielectric is expressed as

$$J_{FN} = F_{AN} \cdot E^2 \cdot \exp\left[-\frac{F_{BN}}{E}\right],$$
$$J_{FH} = F_{AH} \cdot E^2 \cdot \exp\left[-\frac{F_{BH}}{E}\right], \quad (2)$$

where E specifies the magnitude of the electric field in the gate dielectric. F_{AN} and F_{BN} are 1.8×10^{-7} and 1.92×10^8, respectively, and are adjustable modeling parameters for electrons. Similarly, F_{AH} and F_{BH} are 1.83×10^{-7} and 1.91×10^8, respectively, and are modeling parameters for holes. Principally, $F_{AN}(F_{AH})$ and $F_{BN}(F_{BH})$ depend on the tunneling barrier height (i.e., $F_{AN}/F_{AH} \propto 1/\phi_b$ and $F_{BN}/F_{BH} \propto {\phi_b}^{3/2}$) and effective mass of the tunneling electrons (holes) [31] and where the barrier height is defined as the difference between the electron affinities of the metal/semiconductor and the dielectric.

3. Results and Discussion

Figure 3 illustrates the conduction band energy diagram (a), current voltage characteristics of SiC MOSFET (b), electric field at the interface, and gate current density at various gate biases. While dielectric constant of HfO_2 is larger than that of SiO_2 (see Table 1), a narrow bandgap of HFO_2 results in smaller conduction band offsets with respect to SiC material (Figure 3(a)). With these small conduction band offset values, the probability of carriers tunneling through the dielectric is increased significantly and hence it may limit the purpose of using this high-k material. Tanner et al. [23] have earlier reported a conduction band offset of 0.7–0.9 eV at the HfO_2/4H-SiC interface that results in insufficient barrier height causing unacceptably high leakage current values. A high leakage current density as a result of small conduction band offset and increased density of surface trap at HfO_2/SiC interface has been reported [34] and could have an impact on the electron transport properties of the MOSFET. Note that, for low power electronics, HfO_2 is a promising gate oxide material for Si-MOSFETs due to its high dielectric constant. However, its small bandgap value of 5.7 eV presents prohibitive feelings for 4H-SiC based MOSFET/IGBT devices. On the other side, a significant reduction in the electric field is induced in the dielectric material as a result of its higher dielectric constant values. The low band offsets at the dielectric/SiC interface have recently been addressed by introducing an ultrathin SiO_2interfacial layer between SiC and high-k HfO_2 dielectrics [35, 44] for SiC based MOS structures. A barrier height of 1.5 eV has been extracted from the Schottky emission characteristics, which is higher than the reported value for HfO_2 on SiC surface without additional interfacial SiO_2. Thus, presence of an interfacial SiO_2 layer increases band offsets to reduce the leakage current characteristics. While gate leakage current has been reduced significantly with sandwiched SiO_2 [44], further optimization of this new layer stack is required to get a clean and abrupt interface morphology with minimization of formation of intermixing layer at the interface. Note that simulation of new dielectric layer stack with additional SiO_2 has been ignored here primarily because band alignment values are not available for the whole layer stack of HfO_2/SiO_2/4H-SiC [35]. This may in fact be the objective of future work where new dielectric combinations are assessed for surface passivation and as gate dielectric material for SiC based MOSFETs/IGBTs. With fixed drain-source bias, gate current density increases with the increase of gate bias. Current voltage characteristics at different gate-source biases of simulated MOSFET show reduction in the drain current in saturation region and increase in the ON-resistance (i.e., R_{ON} is defined as a slope of the I-V characteristics in the linear region of device operation for a given gate bias above threshold: see Figure 3(b)) with temperature, consistent with the experimental findings of 4H-SiC based MOSFETs [12–14], and hence allow paralleling of the MOSFET devices for high power applications. Increase in the ON-resistance with temperature is attributed mainly to decrease in the bulk carrier mobility for thick drift layer MOSFETs.

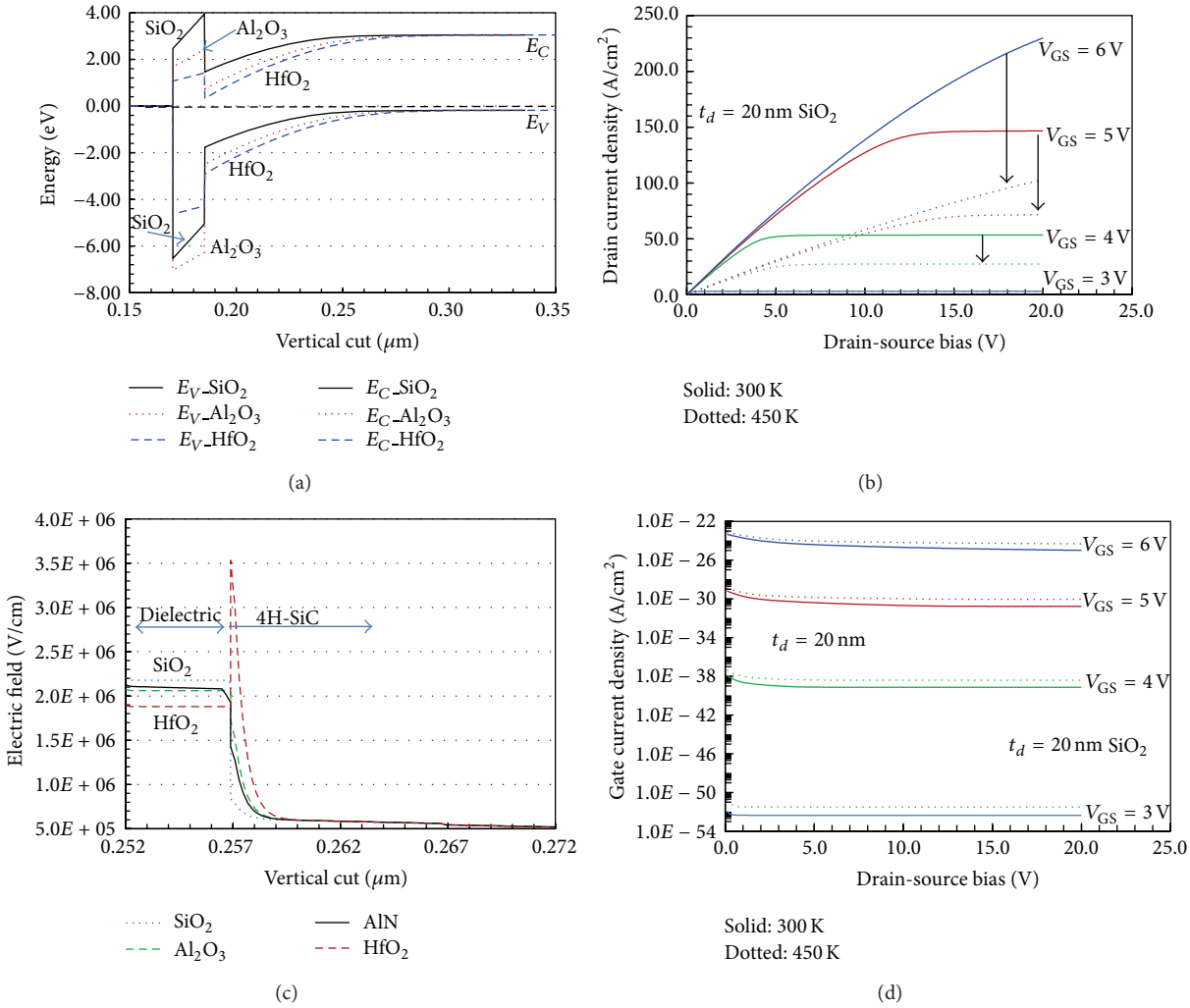


FIGURE 3: Conduction and valence band energy diagram (a), current-voltage characteristics at different temperatures for 20 nm thick SiO_2 (b), electric field at the semiconductor-dielectric interface for various dielectrics (c), and gate current density at different gate-source biases for 20 nm SiO_2 gate dielectric (d).

For fixed dielectric thicknesses of 5 nm each, gate current density is plotted in Figure 4 as a function of gate-source bias at constant drain-source voltage of 10 V for various dielectric materials. With varying gate bias at constant drain-source bias, the MOSFET goes from accumulation (negative bias) to depletion and then to inversion region (positive gate bias) as expected. In the range from 6 to 12 MV/cm, the gate current density decreases with the increase of dielectric constant of the respective material. For example, current density of 3.9×10^{-4} (1.3×10^{-8}), 1.3×10^{-4} (2.5×10^{-9}), 1.2 x 10^{-5} (6.8×10^{-10}) and 1.1 x 10^{-5} (1.3×10^{-10}) A/cm^2 for SiO_2, Al_2O_3, AlN and HfO_2, respectively is obtained at 10 (7) MV/cm with equal dielectric thickness. While dielectric constant of HfO_2 is larger than that of other high-k dielectrics (e.g., Al_2O_3, AlN), this advantage is fairly negated due to smaller bandgap and hence smaller conduction band offset of HfO_2 with 4H-SiC. Simulations predict that materials (AlN, Y_2O_3) with moderate/high dielectric constant along with smaller bandgaps tend to suffer from higher leakage current at negative bias (accumulation) as a result of smaller valence band offsets. This has earlier been experimentally witnessed for TiO_2 (E_g = 3.5 eV) material that has shown significantly higher gate leakage current density in accumulation region in comparison to A_2O_3 (E_g = 8.7 eV) material for 4H-SiC based MOS capacitors [27].

AlN and Al_2O_3 are two promising compatible (almost similar dielectric constant with 4H-SiC) candidates as gate dielectric with 4H-SiC materials. However, lower bandgap of AlN (6.2 eV) in comparison with Al_2O_3 (8.7 eV) or SiO_2 (8.9 eV) might be disappointing for 4H-SiC devices, but a lattice mismatch to SiC of only 1% along with almost the same thermal expansion coefficient of up to 1000°C and a high dielectric constant are more encouraging parameters. Similar to HfO_2 and Al_2O_3 [35, 36, 44] as discussed earlier, a thin SiO_2 as a buffer layer has been inserted [33] between SiC and AlN as additional barrier layer to prevent electron injection from semiconductor to dielectric, which may further decrease leakage current. Figure 5 illustrates the gate

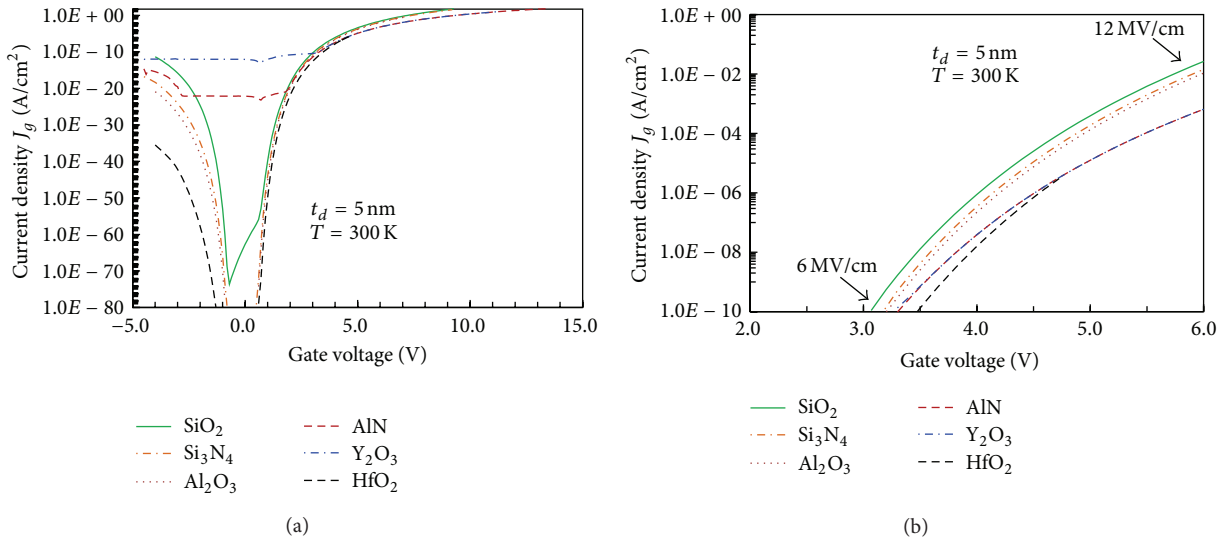


FIGURE 4: Gate current density as a function of gate bias for various gate dielectrics of thickness 5 nm, each at 300 K (a). Zoomed-in view over limited gate bias range is also shown with an electric field span of 6 to 12 MV/cm (b).

current density for SiO_2 and Al_2O_3 dielectrics with various thicknesses at 300 K. Gate current density decreases with increasing dielectric thicknesses as expected. Compared to SiO_2, a lower gate current density is achieved for Al_2O_3 material for equal gate dielectric thickness. Al_2O_3 material belongs to the family of wide bandgap (8.7 eV) and possesses a potential barrier of 2.8 eV and 1.7 eV with Si and 4H-SiC conduction band, respectively. Although conduction band offsets with 4H-SiC material are smaller than that of Si, this value is high enough to effectively suppress the carrier injection at interface. A gate current density of $2.0e-3(1.7e-3)$ and $3.5e-3(3.0e-3)$ is obtained for Al_2O_3 and SiO_2 respectively, at 10 MV/cm field assuming 20 (10) nm thick gate dielectric. Similarly, a gate current density of $3.0e-13(1.7e-13)$ and $5.0e-13(5.6e-13)$ is predicted for Al_2O_3 and SiO_2, respectively, at 5 MV/cm field with 20 (10) nm thick gate dielectric. A gate leakage current density of 10^{-3} A/cm^2 at 8 MV/cm of 4H-SiC MOS capacitor has been obtained for amorphous Al_2O_3 film grown on 4H-SiC surface by atomic layer deposition technique [23]. A barrier height of 1.58 eV has been extracted using Fowler-Nordheim tunneling model for Al_2O_3/4H-SiC interface. The amorphous Al_2O_3 films [23] further show superior leakage current density characteristics compared with many other high-k materials and stacks (i.e., Ta_2Si, SiO_2/TiO_2, Gd_2O_3, SiO_2/HfO_2, AlN, and Si_3N_4) investigated on 4H-SiC surface.

Drain-source current density and threshold voltage (i.e., the value of the gate-to-source voltage V_{GS} needed to create or induce the conducting channel to cause surface inversion) of simulated 4H-SiC MOSFET device are illustrated in Figure 6 for various gate dielectrics. The value of the threshold voltage for MOSFET device is generally dependent on some physical parameters of the device structure such as the gate material, the thickness and type of dielectric layer, substrate doping concentration, oxide-interface fixed charge concentration (or density), and channel length and channel width. For a given gate dielectric material, threshold voltage of a 4HSiC-MOSFET increases linearly with the dielectric thickness as expected. However, the amount of variation in threshold voltage is suppressed using high-k dielectric material (e.g., Al_2O_3, HfO_2) with fixed other physical parameters of the device structure, an aspect that is favorable from device manufacturability point of view. On the other side, threshold voltage decreases with the increase of dielectric constant of a gate material for a fixed gate dielectric thickness indicating that a trade-off is required with the substrate doping to adjust the threshold voltage to higher value for a SiC based MOSFET power device. For example, a total shift in the threshold voltage of about 2.5 V has been observed with variation in gate dielectric material from SiO_2 to HfO_2 (see Figure 6(a)). This further resulted in the increase in the transconductance of the device with the increase of the dielectric constant from SiO_2 to HfO_2. For example, a maximum device transconductance of 87, 69, 68, 64, and 45 μS/μm has been observed for HfO_2, AlN, Al_2O_3, Si_3N_4, and SiO_2, respectively. MOSFET device transconductance is simply defined as $(W \cdot \mu_n \cdot C_{ox} \cdot V_{DS})/L$, where W is the gate width, L is the gate length, μ_n is the channel mobility of electrons, and $C_{ox}(\approx \varepsilon_r/t_{ox})$ is the dielectric capacitance of the respective material. Considering μ_n and other parameters to be constant in our simulations, changing dielectric constant only helps to improve the maximum device transconductance as observed in our numerical simulations and also is found out to be consistent with the experimental findings [42]. Higher transconductance might help to improve the switching capability of the power device. Note that threshold voltages of Si_3N_4, Y_2O_3, and AlN are clustered with each other as a result of smaller difference in the bandgap (and hence conduction band discontinuity) of these materials for fixed dielectric thickness. Generally speaking for a given channel length of a MOSFET, as the physical thickness of the gate dielectric material increases, the number of electric

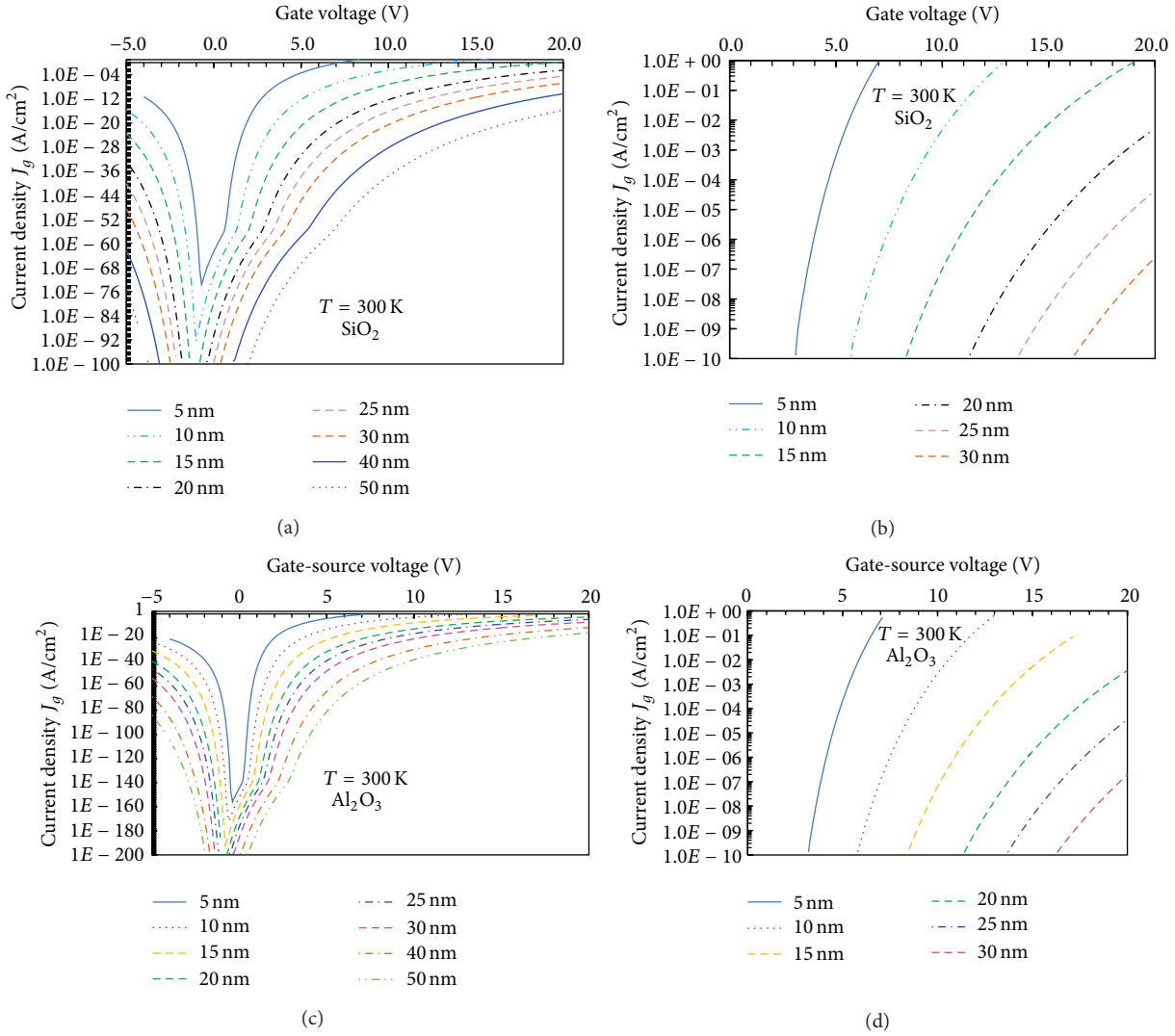


FIGURE 5: Gate current density at 300 K for different gate dielectric thicknesses using SiO_2 as a gate dielectric ((a), (b)) and Al_2O_3 as a gate dielectric ((c), (d)). Zoomed-in view is also shown for SiO_2 (b) and Al_2O_3 (d) at higher gate current densities.

field lines originating from the bottom of the gate electrode and terminating on the source and possible drain regions increases. These field lines form an electric field from source to channel region and thereby decrease the potential barrier height between the channel and the source. A lower potential barrier height here reflects a lower threshold voltage of a device for a constant channel length. Note that a potential distribution along the channel surface is strongly dependent on gate dielectric permittivities that in fact define the amount of variation in the potential barrier height. The high-k dielectrics allow reducing gate leakage current while keeping a very low electrical equivalent oxide thickness, an aspect that is especially critical for Si based low power electronics. For high power electronics using SiC based MOSFETs where the conduction band discontinuity of gate dielectric is relatively small compared to Si counterpart, a thick gate dielectric of the order of 20–30 nm (i.e., maximum of 6.5–10 MV/cm considering 20 V bias at the gate; commercial SiC-MOSFETs today use 4-5 MV/cm with 20 V gate bias and 40–50 nm SiO_2 gate dielectric) is far sufficient to simultaneously fix the threshold voltage to large positive value with reduced gate leakage current density for high-k gate material.

One reliability concern for 4H-SiC MOSFETs is the quality and reliability of the gate-dielectric interface that has severely been affected by the presence of traps and carrier energy interface states. The origin of these states is primarily linked with the imperfect nature of 4H-SiC dielectric interfaces due to presence of carbon clusters and dangling Si and C bonds. Consequently, the channel electrons scatter with these energy states and get trapped there, hence increasing the channel resistance. The location and density of interface states within the bandgap affect not only the channel electron mobility but also the FN tunneling currents at the SiC dielectric interface. Note that the threshold voltage may also be affected by the so-called fast surface states at the semiconductor-dielectric interface and by fixed charges

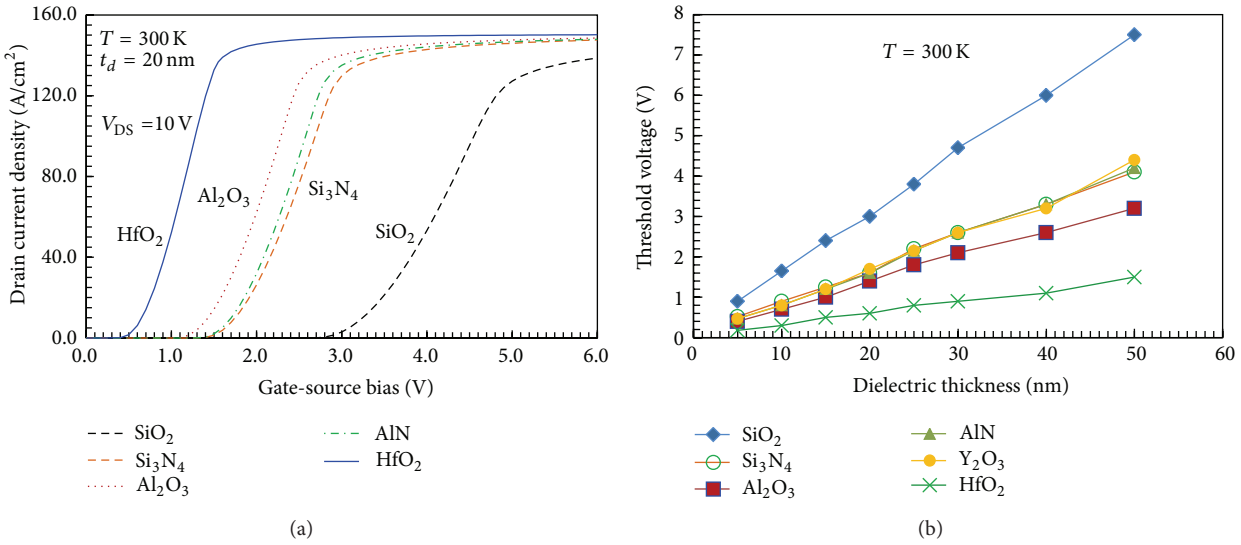


FIGURE 6: Drain current density as a function of gate-source bias for various gate dielectrics using 20 nm thick dielectric material (a) and threshold voltage shift as a function of dielectric thickness for various gate dielectrics (b). Threshold voltages of Si_3N_4, Y_2O_3, and AlN are clustered with each other as a result of smaller difference in the bandgap of these materials. Simulations have been performed for 20 nm thick gate dielectric at 300 K.

in the insulator layer of the gate. As earlier said, the density of charged interface states in 4H-SiC/SiO_2 structures is 2-3 order of magnitude higher than that at Si/SiO_2 MOS interface. While this may not be a significant concern with modern day Si based fabrication technology, depending on the type and growth mechanism of dielectric film on 4H-SiC MOSFET surface, these energy states of the order of 1.0×10^{11}–5.0×10^{12} cm^{-2} are routinely measured in real devices [23–26]. The threshold voltage of nonideal MOS capacitor is simply defined as

$$V_{TH} = \varphi_{ms} + 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}, \quad (3)$$

where φ_{ms} is the metal-semiconductor work function difference, ϕ_F is the Fermi potential, Q_B is the depletion charge due to ionized impurities, C_{ox} is the oxide capacitance, and Q_{ox} is the total oxide charge which is zero for ideal MOS capacitor. Note that Q_{ox} is the sum of interface trapped charge (Q_{int}: these may be positive or negative and located at the interface), fixed oxide charge (Q_f: these may be positive or negative and located very close to the interface), oxide trapped charge (Q_{ot}: these may be positive or negative due to hole and electron trapped in the bulk of the gate oxide), and mobile ionic charge (Q_m: origin is due to presence of ionic impurities in the oxide film but far from the interface) and its overall impact causes a voltage drop across the oxide. Depending on the growth mechanism and interface material, the polarity of this fixed oxide charge induces a shift in the voltage (i.e., V_{TH} decreases if Q_{ox} is positive or vice versa). Considering arbitrary growth conditions, positive and negative interface state charge density have been introduced here at 4H-SiC/SiO_2(positive), 4H-SiC/HfO_2(positive), and 4H-SiC/Al_2O_3 (negative) to study their influence on drain-source current. Earlier experimental findings report that depositing Al_2O_3 or HfO_2 on 4H-SiC [23, 34–36] drastically shifts the flat band voltage to positive voltages, meaning that negative charges are generated either at the interface or near the interface and/or in the bulk of the insulating layer. Thus effective fixed oxide charge of the MOS capacitor is considered negative for pure Al_2O_3 and HfO_2 on 4H-SiC [23, 34–36, 43] surface and positive for another dielectric such as pure SiO_2 on SiC [35, 37]. More interestingly, stacking gate dielectric of HfO_2/SiO_2/SiC [35] and Al_2O_3/SiO_2/SiC [36] scheme also reveals negative effective oxide charges at the respective interfaces for SiC MOS capacitors. Figure 7 illustrates the influence of these interface state densities on drain-source characteristics. Positive interface density induces a negative shift in the threshold (i.e., V_{TH} decreases) while negative interface density increases the threshold voltage of the device. Furthermore, using a high-k dielectric material, threshold voltage variation is shrunk for a given dielectric thickness predicted by the numerical simulation.

4. Conclusions

Influence of various possible dielectric materials on 4H-SiC MOSFETs has been studied in this work. For fixed dielectric thickness, numerical device simulation predicts a smaller shift in the threshold voltage for high-k dielectrics. Similarly, a smaller shift in the threshold voltage is expected for high-k dielectric material with variation in the interface charge densities. Compared to conventional SiO_2 as gate dielectric used today in SiC MOSFETs, high k-gate dielectric reduces significantly the amount of electric field in the gate dielectric with equal gate dielectric thickness and hence

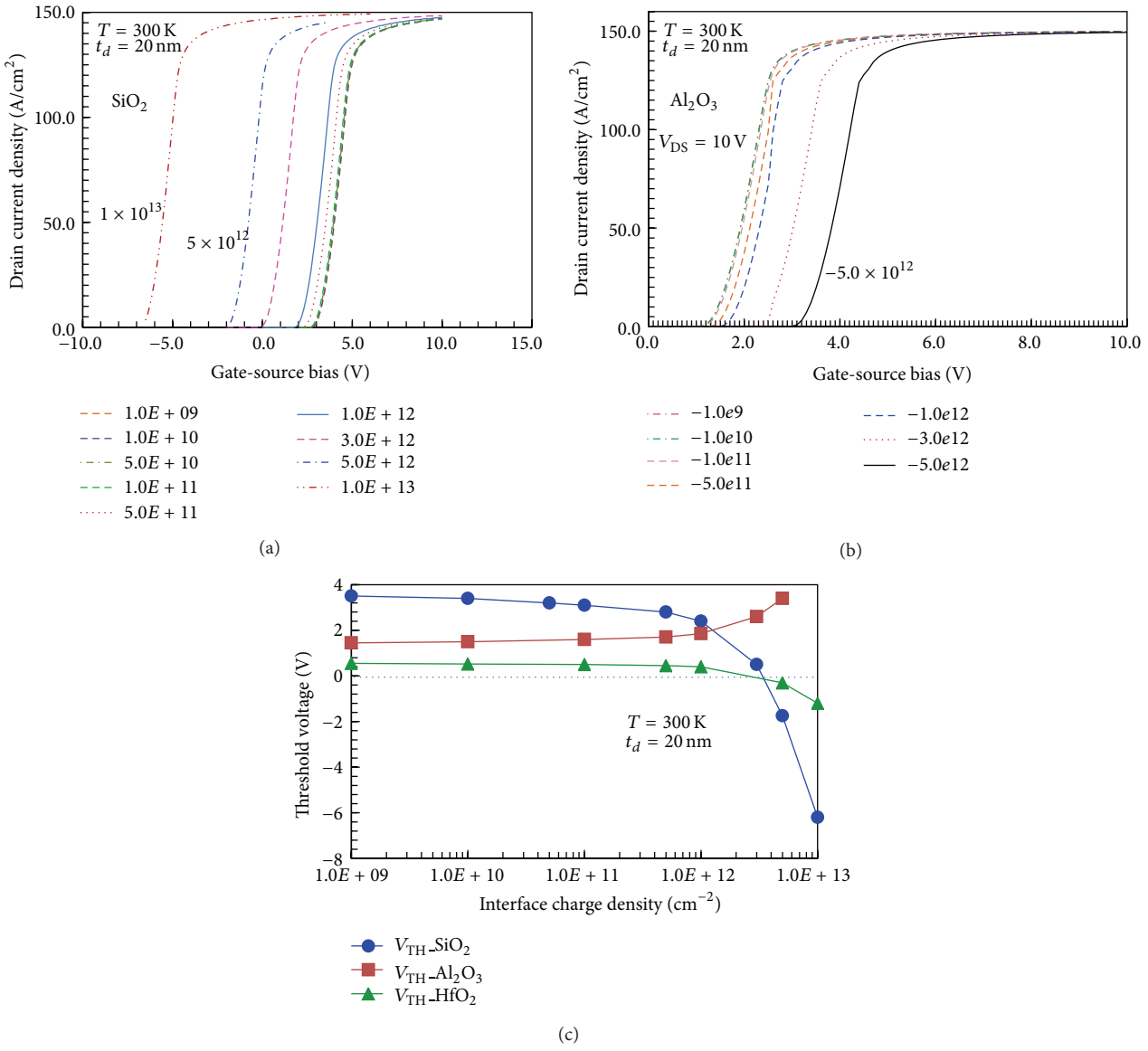


Figure 7: Drain current density as a function of gate-source bias for various interface state densities using SiO_2 as a gate dielectric (a) and Al_2O_3 as a gate dielectric (b). Threshold voltage shift is also shown for various gate dielectrics as a function of interface state densities (c). Simulations have been performed for 20 nm thick gate dielectric at 300 K.

the overall gate current density. To realize full potential of high-k dielectric over 4H-SiC MOSFET surface, a clean and abrupt dielectric/semiconductor interface morphology is prerequisite for reliable device operation. The numerical data presented in this work will not only provide a useful guideline to device and circuit designer but also support technology development when different dielectric options are considered.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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