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Research Article

Trigger Pulse Generator Using Proposed Buffered Delay Model and Its Application

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This paper proposes a circuit capable of incorporating buffered delays in the order of picoseconds. To study our proposed circuit in the profound way, we have also explored our proposed circuit using emerging technologies such as FinFET and CNFET. Comparisons between these technologies have been made in terms of different parameters such as duration of incorporated delays (pulse width) and its variability with supply voltages. Further, this paper also proposes a trigger pulse generator by utilizing proposed buffered delay circuit as its basic element. Parametric results obtained for the proposed trigger pulse generator match different application specific requirements. These applications are also mentioned in this paper. The proposed trigger pulse generator requires very low supply voltage (700 mV) and also proves its effectiveness in terms of tunability of pulse width of the generated pulses. The modeling of the circuit has been done using Verilog and the simulation results are extensively verified using SPICE.

1. Introduction

In the present electronics world, certain applications require a circuit that offers precise delay for providing synchronization [1]. It is also essential to maintain the signal strength and information stored in the signal while propagating it through the delay circuits [2]. With the advent of the new technologies, the delays such as propagation delays and delta delays have been scaled down to be in the order of picoseconds [3]. Thus, an accurate and precise buffered delay incorporating circuit is required to fulfill these necessities. Seeing the importance of buffered delay circuits, this paper proposes a precise buffered delay circuit capable of introducing delays in the order of picoseconds (pulse duration) without degrading the signal strength. Thus, the proposed buffered delay circuit can provide synchronization with very accurate measure and acceptable output signal strength.

To provide in-depth analysis of the proposed circuit, we have also realized the proposed circuit by utilizing emerging technologies such as FinFETs and CNFETs. Comparisons have been made in terms of delay time (minimum pulse duration) incorporated by the proposed circuit, while realizing it with different technologies. Further, variability analysis of the proposed circuit level model of buffered delay circuit has also been carried out in this paper.

In the conventional approach of generating trigger pulses, we are generally using RC circuits whose output waveforms are affected by the time constant [4]. Figure 1 shows the effect of time constant of the RC trigger circuit. For generating trigger pulses as shown in Figure 1(c), we need very small time constant for RC circuit which is a challenging task to achieve. These conventional trigger pulse generators are also very bulky to be incorporated in the nanoregime circuits [5]. Hence, this paper also proposes a trigger pulse generator circuit by utilizing the proposed buffered delay circuit as an elementary unit. Further, different applications' specific parameters of the proposed trigger pulse generator are also mentioned in this paper.

The rest of the paper is organized as follows. Section 2 shows the circuit level model of proposed buffered delay circuit. Comparative study of proposed circuit realized with different technologies has been made in Section 3. Section 4 presents the circuit level model of proposed trigger pulse generator. Simulation results and discussions are mentioned

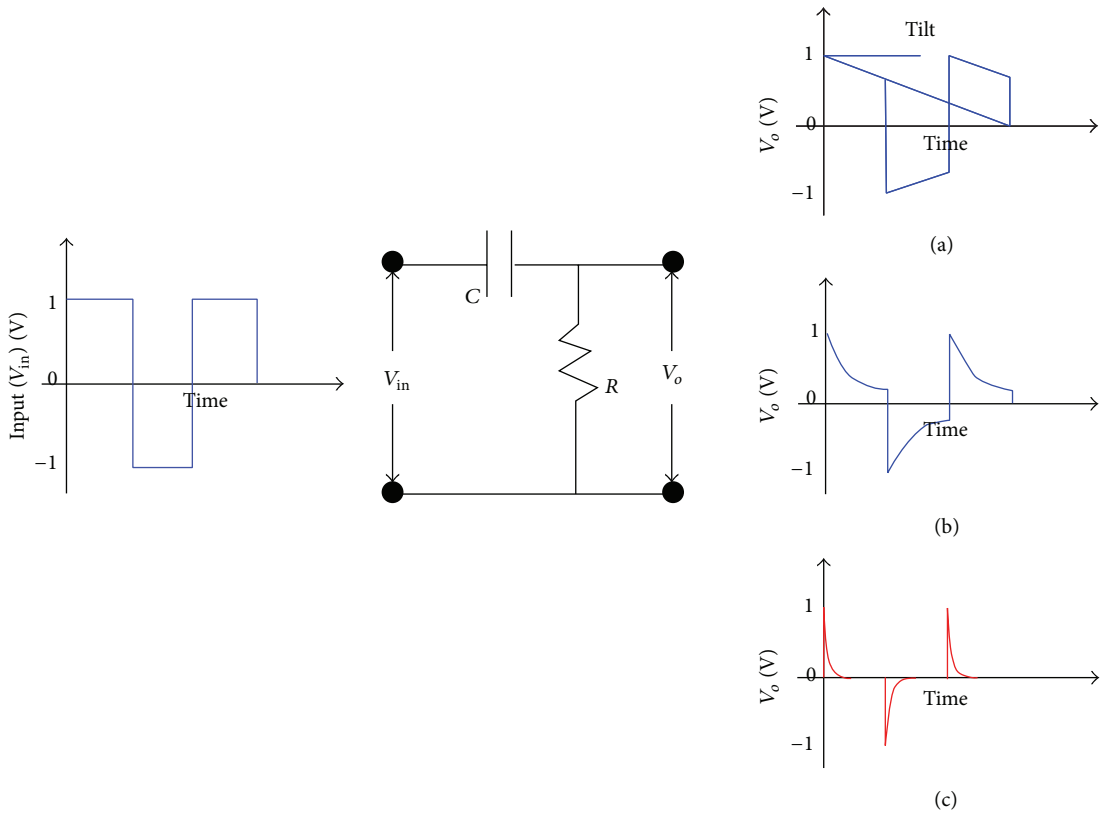

FIGURE 1: Effect of time constant of the RC circuit in the output waveforms: (a) high value of time constant, (b) medium value of time constant, and (c) very low value of time constant.

in Section 5. Applications of the proposed trigger pulse generator are given in Section 6. Finally, concluding remarks are made in Section 7.

2. Proposed Buffered Delay Circuit

A buffered delay circuit is an arrangement of electronic components which takes a signal as an input and introduces a time difference (delay). Additionally, it minimizes the rise time and fall time effects, thus leading to a buffered signal with introduced delay as an output signal. The duration of delay introduced by these circuits may range from few picoseconds to several hundred milliseconds. The circuit level model of proposed buffered delay circuit is shown in Figure 2. It can be observed from the circuit that MOS transistors are connected in a push-pull topology. MOS transistors (MP1–MP3 and MN1–MN3) and (MP4–MP6 and MN4–MN6) are connected in such a way that the output of the first pair of connection is providing input to the next network.

For the proposed MOSFET based buffered delay circuit, if logic state "1" is input to the inverter composed of transistors MN1/MP1, then high logic turns on transistor MN1 and, thus, node 2 is connected to logic state "0" (GND) (see Figure 2). Logic "0" at node 2 turns on transistor MP4 and node 4 holds logic state "1" (V_{DD}). This further turns on transistors MN2 and MN3. Now, node 2 and node 3 connect to logic state "0" (GND) through MN2. As node 3 is directly connected to inverters composed of MN5/MP5, it provides inverted logic of node 3, that is, logic "1" at the output terminal (OUT) of the proposed circuit as shown in Figure 2. Similarly, for logic state "0" at the input terminal (IN), it turns on transistor MP1 which connects logic "1" (V_{DD}) to node 1. High logic at node 1 turns on transistor MN4 which connects node 5 to logic state "0." Low logic at node 5 turns on transistor MP2 and connects node 1 and node 3. As node 3 is directly connected to input terminal of the inverter composed of transistors MN5/MP5, it provides inverted logic of node 3, that is, logic "0" at the output terminal (OUT) of the proposed circuit as shown in Figure 2. Thus, output logic state/signal, same as input state/signal, is achieved at the output of the proposed circuit. Meanwhile, some delay is introduced between the input and output signal. The delay introduced by the proposed delay circuit is achieved as a result of time (delay) taken by the signal while propagating from one node to another as explained above.

Cascaded inverter arrangement is incorporated in the proposed design to introduce delay in the signal. A pair of cascaded inverters can work as a delay element and incorporates delay equal to the propagation delays of the two inverters. The propagation delay incorporated by the inverter depends upon the charging and discharging of the load capacitance. However, approximate expression is derived by computing average value of current equal to the saturation

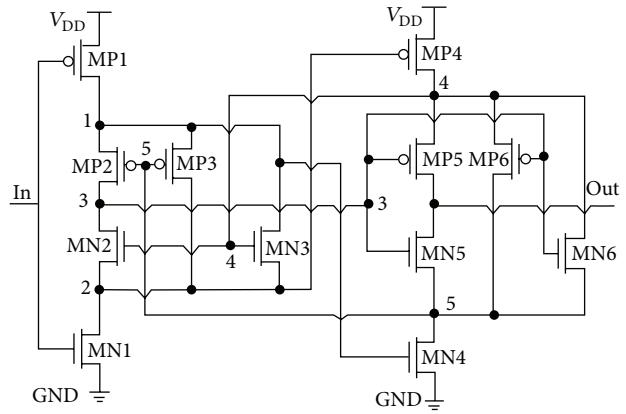

Figure 2: Circuit level model of proposed buffered delay circuit.

current of the NMOS and PMOS transistors which is given as [6]

$$I_{AVG} = \frac{k_P}{2}\left(V_{GS} - \left|V_{T_p}\right|\right)^2 = \frac{k_P}{2}\left(V_{DD} - \left|V_{T_p}\right|\right)^2 \approx \frac{k_P}{2}{V_{DD}}^2. \quad (1)$$

As $V_{DD} \gg |V_{T_p}|$ and V_{TN}, the above equation is used to determine the propagation delay (t_P) as

$$t_P = \frac{1}{2}\left(t_{PLH} + t_{PHL}\right) = \frac{C_L}{2V_{DD}}\left(\frac{1}{k_P} + \frac{1}{k_N}\right), \quad (2)$$

where t_{PHL} and t_{PLH} are the propagation delays for high to low and low to high transitions of the propagation signal. Equation (2) shows the propagation delay expression for the cascaded inverter. In the proposed design, inverters composed of MN1/MP1 and MN5/MP5 are cascaded. The input provided at the input terminal of inverter MN5/MP5 propagates through push-pull arrangement as shown in Figure 2. Based upon the requirement, node 3 connects to either high logic state "1" (V_{DD}) via transistors MP1/MP2 or low logic "0" (GND) via transistors MN1/MN2. The output of inverter MN1/MP1 (node 3) is finally cascaded with the inverter MN5/MP5. Meanwhile, the delay achieved during propagation of input signal through the cascaded network architecture of the proposed delay circuit is the desired delay introduced in the signal obtained at the output node. While making abrupt transition (V_{DD} (logic state "1") to GND (logic state "0")), the effect of rise time (t_R) and fall time (t_F) > t_{PHL}/t_{PLH} can be expressed as

$$t_{R/F} = 2\sqrt{{t^2}_{PHL/PLH(actual)} - {t^2}_{PHL/PLH(step)}}, \quad (3)$$

where $t_{PHL/PLH(actual)}$ represents the actual propagation delay of the input signal while making transition from high to low and low to high logic state, respectively. Similarly, $t_{PHL/PLH(step)}$ represents the propagation delay of the proposed circuit while making transition from high to low or low to high logic state, respectively. Using (2) and (3), t_R (from 10% of V_{DD} to 90% of V_{DD}) and t_F (from 90% of V_{DD} to 10% of V_{DD}) can be expressed as [6]

$$t_{R/F} = \frac{0.9V_{DD}C_L}{|I_{AVG}|} \approx \frac{0.9C_L}{V_{DD}}\left(\frac{1}{k_P} + \frac{1}{k_N}\right). \quad (4)$$

The effect of $t_{R/F}$ is minimized in the proposed circuit as $t_{PHL/PLH(step)}$ traces $t_{PHL/PLH(actual)}$ while signal propagates through the push-pull arrangement of the transistor connected network. Also, transistors MP3/MN3 and MP6/MN6 used in the proposed circuit (see Figure 2) connect node 1 to node 2 and node 4 to node 5, respectively, to minimize the $t_{R/F}$ effect by synchronizing the signal at both nodes.

Thus, the topology is providing interdependent network to generate the output, which is also responsible for maintaining the fixed bias points for the different transistors. As the bias points are not changing with the process, there is less chance of mismatch of the bias points of the transistors which also increases the stability of the generated output by the proposed design. Hence, the circuit is robust and immune to the external disturbances [7]. This has been also shown by the variability analysis of different technologies in Section 5.

3. Realization of Proposed Circuit Using Emerging Technologies

To provide in-depth analysis of the proposed MOS circuit level model of the buffered delay circuit, we have realized the proposed circuit using the emerging technologies, such as FinFET and CNFET. With the technology evolution, these devices have been evidenced as promising candidates to enhance the properties of the circuit with the technology scaling [8]. This section also shows the comparative study of the proposed circuit level model using these technologies.

3.1. Basic Structure of FinFET and Its Characteristics. FinFET is an emerging technology which is proving to be a deserving candidate to replace the present CMOS technology [9]. The basic structure of FinFET is shown in Figure 3. The circuit level model shown in Figure 2 has been realized using FinFETs which is shown in Figure 4.

As the double gate structure is capable of providing the improved gate control as compared to the single gate structure, it enhances the device properties [10]. FinFET is the cutting-edge technology that effectively eliminates the problems of short channel effects [11]. Hence, we have included this technology to realize the proposed buffered delay circuit. In order to see the effect of this technology on the characteristics of proposed circuit level model, we have made comparisons in terms of the pulse width and its variability with the supply voltages. Hence, this section demonstrates a FinFET based buffered delay circuit to examine the effect of technology change on the characteristics of proposed buffered delay circuit.

From Figure 4, it can be observed that the MOS transistors have been replaced with the FinFETs while keeping all other connections unaltered. Thus, the FinFET realization of the proposed circuit possesses the additional features of

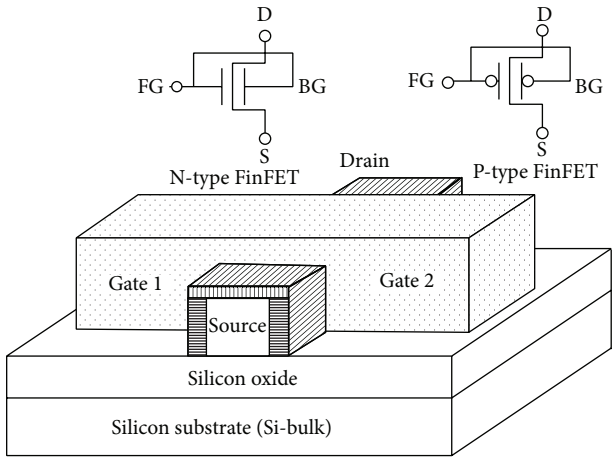

Figure 3: Basic structure of FinFET (double gate structure).

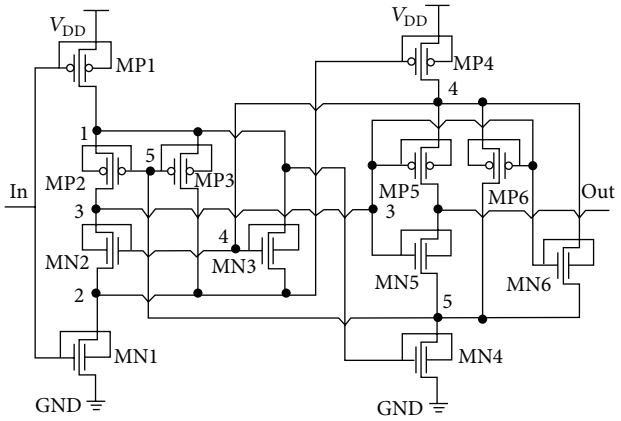

Figure 4: FinFET based realization of the proposed buffered delay model.

FinFET technology. The output waveform of the FinFET based buffered delay circuit for step signal as an input is shown in Section 4 (Figure 7).

3.2. CNFET Structure and Its Characteristics. We need some promising devices which can replace the traditional CMOS, as CMOS is reaching its scaling limits. With the advent of the carbon nanotube (CNT) based field effect transistor (CNFET) technology, it is desirable to integrate the proposed circuit with this new technology which can offer additional advantages [9]. CNFET is one of the promising candidates which have proven their worth in terms of speed and power as compared to MOS transistors in the nanoscale regime [12]. Technology scaling does not affect the robustness of the circuits against PVT (process, voltage, and temperature) variations adversely. The basic structure of CNFET is shown in Figure 5. The CNFET shows higher device performance, even in case of device nonidealities [13, 14]. Circuit level model realized using CNFETs is shown in Figure 6 and its corresponding output waveform of the buffered delay circuit is shown in Section 4 (Figure 7).

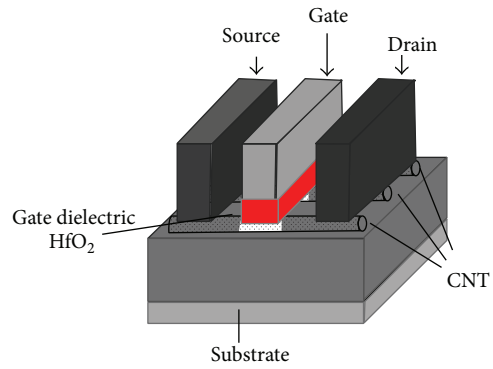

Figure 5: Basic structure of CNFET.

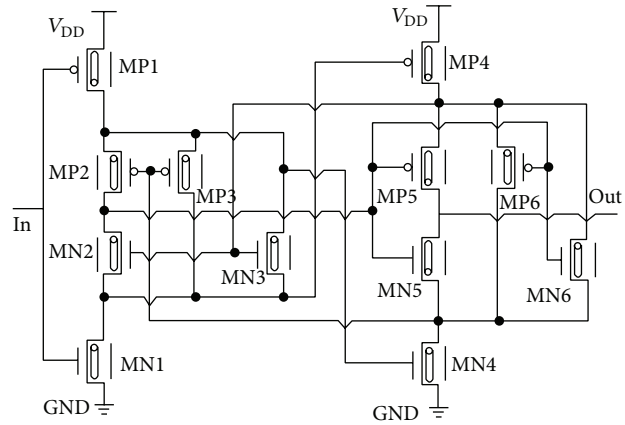

Figure 6: Realization of proposed buffered delay model using CNFETs.

3.3. Comparative Study of Proposed Buffered Delay Circuit Using Different Technologies. Apart from the MOS based proposed buffered delay circuit, this work also makes a comparative study between different technologies by realizing the proposed circuit with these emerging devices. The output waveforms of proposed buffered delay circuit realized using MOSFETs, FinFETs, and CNFETs, respectively, are shown in Section 4 (Figure 7). The output waveforms demonstrate that the buffered signals with additional delay in order of picoseconds are achieved from the proposed circuit level model. Capability to provide buffered output waveform by the proposed buffered delay circuit has been analyzed in this work by providing variable rise time and fall time to the input signal. Measurements using SPICE simulator for rise time (10% to 90% of its value) and fall time (90% to 10% of its value) show that there is 99% reduction (in case of CNFET realization) in the rising edge and fall edge. For example, for a signal having 1 nm rise time and fall time, the output waveform obtained from the proposed buffered circuit is having only 0.01 ns rise time and fall time. These results justify the term buffered signal used for the proposed circuit. The reduction in rise time and fall time of the buffered signal can be achieved up to ≈10 ps and 12.3 ps (in case of CNFET realization). Thus, output of the proposed buffered delay circuit is a delayed version of the input waveform which

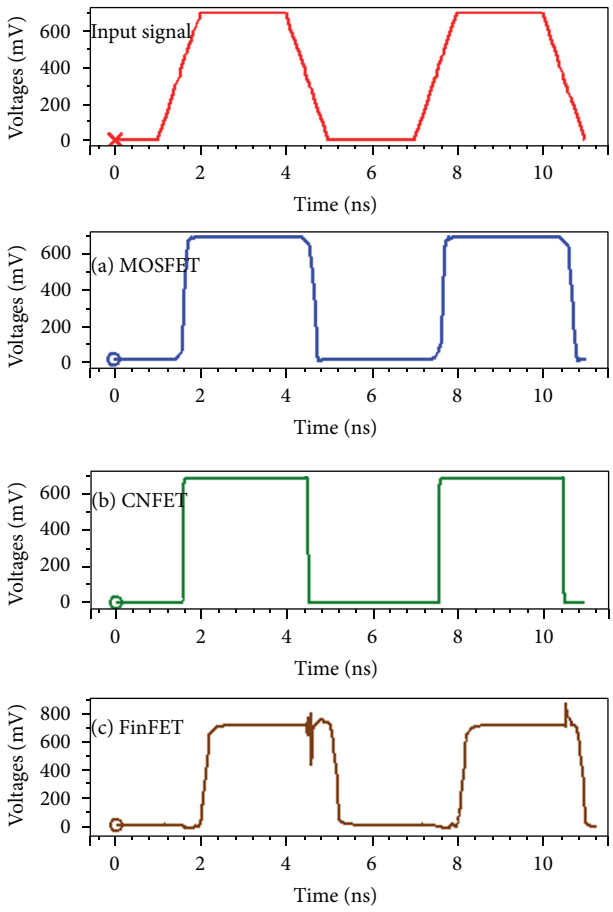

FIGURE 7: Buffered delay output waveform of proposed circuit realized using (a) MOSFETs, (b) CNFETs, and (c) FinFETs.

is also advantageous in terms of minimizing the effects of the rise time and fall time of the input signal. Comparisons among different technology devices have been drawn in terms of the minimum delays that can be introduced and their variability, when realized with different technology devices, with respect to variation in the supply voltages. These results have also been tabulated (Table 1) and their corresponding plots (Figures 11 and 12) have been shown in the following section.

4. Proposed Trigger Pulse Generator

In this section, we have extended the work mentioned in Section 2 by utilizing the basic proposed buffered delay circuit to act as a trigger pulse generator. As many electronics circuits such as 555 timer circuit and SCR firing circuit need trigger pulses to initiate their operations [15, 16], this necessitates trigger pulses generation of very precise control over the pulse width at low supply voltage such 700 mV [17]. Because of these requirements, this work also proposes a trigger pulse generator circuit using the buffered delay circuit proposed in Section 2, employing an additional XOR circuit.

The basic concept utilized to develop the proposed trigger pulse generator using the proposed buffered delay

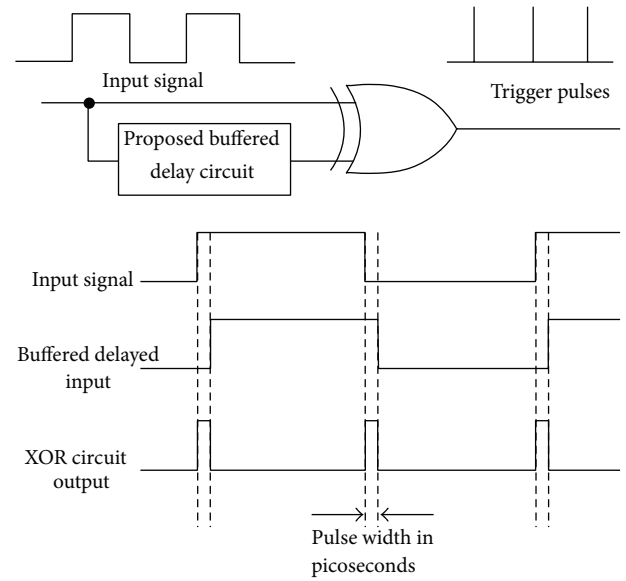

FIGURE 8: Principle of generation of trigger pulses from the proposed buffered delay circuit.

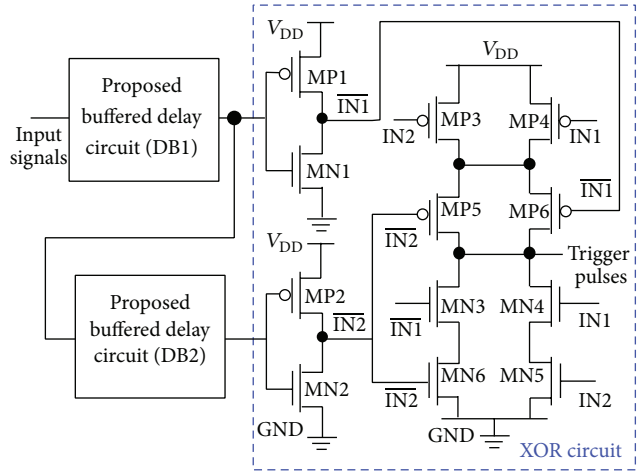

FIGURE 9: Proposed trigger pulse generator.

circuit model is shown in Figure 8. Similar theory has been utilized to generate trigger pulses by using the proposed buffered delay model and an XOR circuit (see Figure 9). From Figure 8, it can be observed that the input pulse is passed from the proposed buffered delay circuit to obtain a delayed version of the input waveform with abrupt switching from low to high and high to low, that is, with minimized rise time and fall time effects of the input signal. Actual signal and its buffered delayed version are XORed to provide impulse trigger pulses (see Figure 8). As our proposed buffered delay circuit is capable of providing delays in order of picoseconds, our proposed trigger pulse generator is also capable of generating trigger pulses with the pulse width in the order of picoseconds.

Figure 9 shows the block diagram of the proposed trigger pulse generator capable of generating trigger pulses of time

Table 1: Comparison between MOSFET, FinFET, and CNFET based on proposed buffered delay circuit.

V_{DD} (mV)	Mean values of delay (s) $\times 10^{-10}$			Delay variability (a.u.) (σ/μ)		
	MOSFET	FinFET	CNFET	MOSFET	FinFET	CNFET
630	2.336	6.118	0.971	0.195	0.167	0.109
665	1.940	5.923	0.926	0.204	0.153	0.119
700	1.632	5.705	0.886	0.208	0.128	0.126
735	1.399	5.599	0.840	0.215	0.142	0.129
770	1.214	5.470	0.780	0.236	0.140	0.135

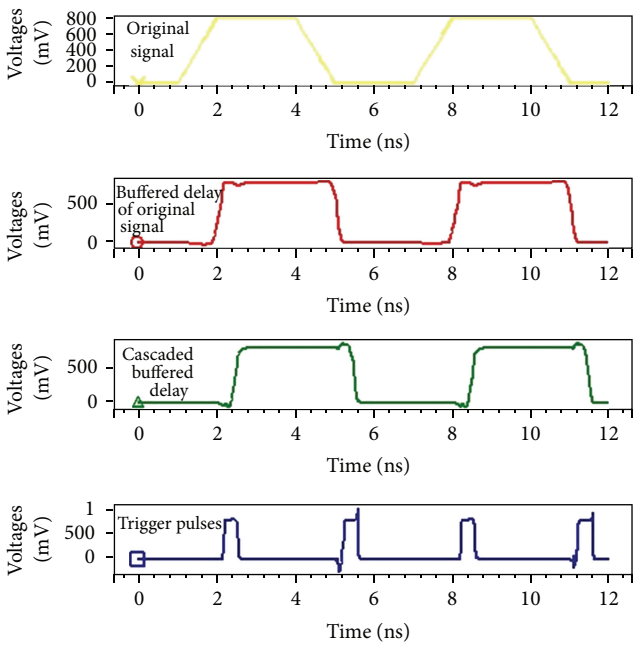

Figure 10: Output waveform of the trigger pulse generator.

duration (pulse width) in the order of picoseconds with negligible effects of rise time and fall time of the input signal.

Here, we have utilized two buffered delay circuits (DB1 and DB2), so that both inputs to the XOR circuit should not be affected with the rise time and fall time delay of the input signal (clock signal). The input signal from a conventional clock is first provided to DB1, and then the buffered output of DB1 (IN1) serves as input of DB2 to generate buffered delay output waveform (IN2) with respect to output IN1. Now, both IN1 and IN2 are buffered waveforms with difference of few picoseconds between them. The precise delay between these waveforms (IN1 and IN2) can be XORed to get trigger pulses. Figure 10 shows the trigger pulses obtained after XORing the output achieved from the two different buffered delay circuits. The relative time difference between the two buffered pulses can be varied to get the trigger pulses for desired pulse duration. This variation ranges from few picoseconds to several milliseconds. The ease in the tunability of the generated pulses' width evidences the effectiveness of the proposed circuit. Thus, the proposed buffered delay circuit is capable of generating trigger pulses of precise pulse duration, whose pulse duration can also be altered as per the requirements by adjusting the relative delay between the two XORed signals.

5. Simulation Results and Discussion

The proposed buffered delay circuit has been modeled using SPICE simulator and results have been extensively verified. We have utilized 16 nm technology node (PTM, developed by the Nanoscale Integration and Modeling (NIMO) Group at Arizona State University (ASU) [18] to substantiate the proposed MOS and FinFET based design). The proposed CNFET based design of buffered delay circuit has been simulated using experimentally validated Stanford University 32 nm CNFET model [12], which can be scaled down to 10 nm channel length and 4 nm channel width. This work shows a comparative study between different technologies to find out the best suited device that can be used to model the proposed buffered delay circuit capable of introducing minimum delays. Figure 11 shows the variation in the delay (pulse width) that can be introduced by proposed buffered delay circuit, utilizing different technologies and its variation with the supply voltages. Corresponding values of these comparisons for the different supply voltages have been also shown in Table 1. It can be observed from Figure 11 that CNFET realization of the proposed buffered delay circuit is capable of incorporating minimum and highly precise delay in the order of picoseconds (delay of 88.6 ps between two pulses) at nominal supply of 700 mV. Further, this work also investigates the proposed buffered delay model in terms of variability of the introduced delay against the variation in the supply voltages. The device parameters such as channel length (L), gate width (W), channel doping concentration (n/p), oxide thickness (t_{ox}), threshold voltage (V_t), carrier mobility (μ_o), and supply voltage (V_{DD}), with variations up to 10%, have been implemented. Monte Carlo simulations for 1000 samples of the proposed circuit realized with MOSFET, FinFET, and CNFET have been performed for higher accuracy. Variability of introduced delay against the supply voltages for different technologies has been tabulated in Table 1 and its corresponding plots have also been shown in Figure 12. The distribution plots that show the introduced delay by the proposed buffer delay circuit realized using MOSFETs, FinFETs, and CNFETs, respectively, for 5000 Monte Carlo simulations at 0.7 V and $T = 27^{\circ}$C have been shown in Figures 13, 14, and 15. It can be observed from Figure 12 that CNFET based design shows least variability in the introduced delay against variations in the supply voltage,

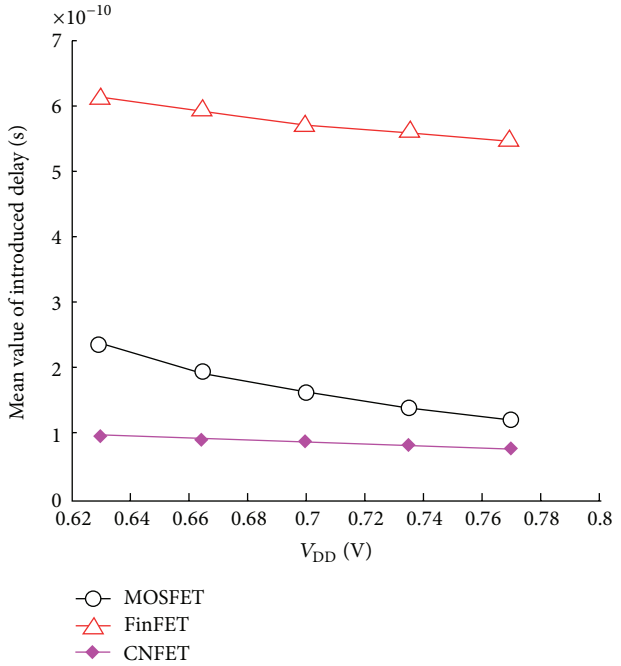

FIGURE 11: Delay (pulse width) introduced by proposed buffered delay model utilizing different technologies and its variations with the supply voltages.

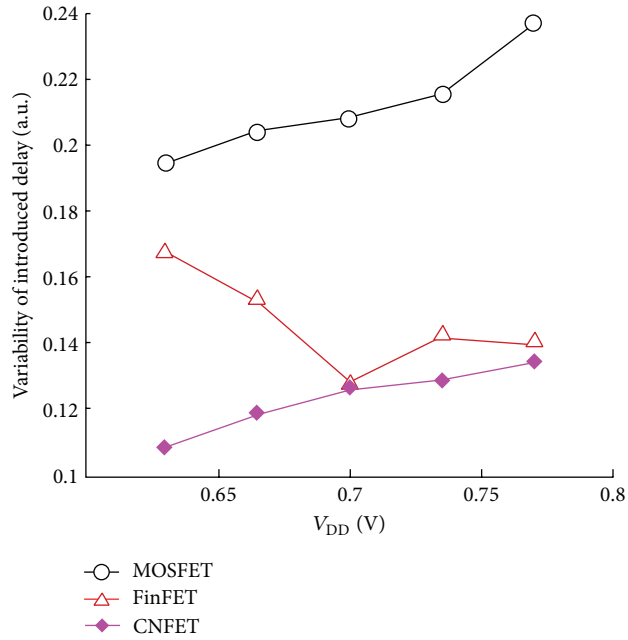

FIGURE 12: Variability analysis of the introduced delay by the proposed buffered delay circuit for various supply voltages.

while MOS implementation of the proposed circuit exhibits more variations. Thus, alteration in technology can be done to boost the performance of the proposed buffered delay circuit. The simulation results illustrate that the CNFET based proposed buffered delay circuit is capable of incorporating more precise delays and is also immune to variations due to the supply voltage as compared to MOS and FinFET based designs. As it is more advantageous to use the MOS transistors in place of CNFETs or FinFETs, due to increased cost and advanced technology requirements to develop these devices, we can utilize the MOS transistors to realize the proposed buffered delay circuit if the delays to be introduced (pulse width) are in range of 163.2 ps at nominal voltage supply of 700 mV. Otherwise, we can use CNFETs for more precise requirements.

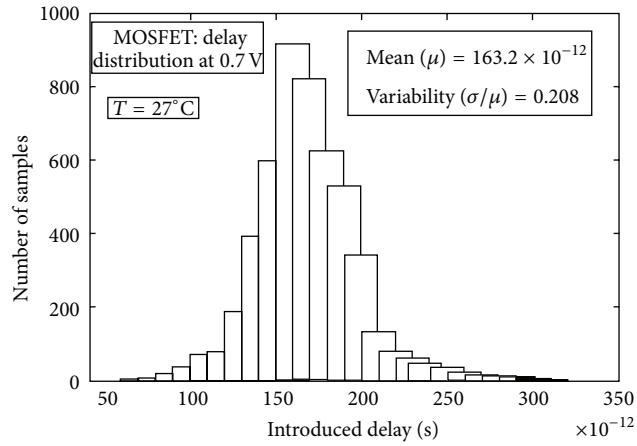

FIGURE 13: Introduced delay distribution plot of the MOSFET based proposed buffer delay circuit.

6. Application of Proposed Trigger Circuit

The proposed trigger pulse generator circuit finds its applications in the circuits requiring trigger pulses of very short durations. Conventional methods for generation of such ultrathin pulses include step recovery diode (SRD), nonlinear transmission line (NLTL), and RC circuit employing very small time constants [19, 20]. As compared to these traditional methods, which are capable of incorporating delays in the range of ns, the proposed buffered delay circuit proves to be more efficient [21]. SRD trigger pulse generators are economical but typically require several volts of input drive level and have a considerably high level of random jitter which leads to undesirable variations under PVT fluctuations [22]. As mentioned in Section 1, trigger pulses can also be generated using RC circuit employing very small time constants. But such traditional methods are not that much efficient and require a large circuit arrangement which is not feasible in the current technology trends [5].

Therefore, the trigger pulse generator circuit proposed in this work overcomes several demerits of the prevailing trigger pulse generator mechanism and also finds its application as a microwave pulse generator as the generated output pulses are in the order of picoseconds. Moreover, the buffer circuit produces a better shaped waveform, cutting down rise and fall time, eliminating one major source of delay while switching. This refined waveform when passed through the different buffered delay circuit provides abrupt switching and, thus, minimizes the rise time and fall time effects. The two

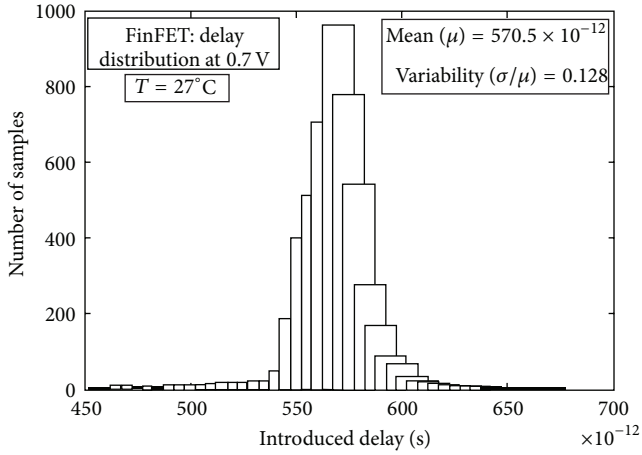

Figure 14: Introduced delay distribution plot of the FinFET based proposed buffer delay circuit.

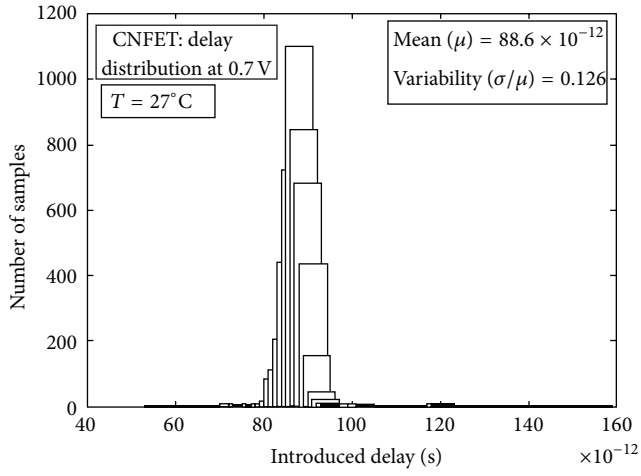

Figure 15: Introduced delay distribution plot of the CNFET based proposed buffer delay circuit.

different buffered waveforms, having different period with very small interval time gap between them, can be XORed to get triggering pulses. Thus, these pulses are actually the delay (measure of pulse duration) in the output waveforms of the proposed buffered delay model. The resolution of the trigger pulses is dependent on the preciseness of the delay incorporated by the proposed buffered delay circuit. The simulation results given in Section 5 show that, for very high and precise generation of trigger pulses, we can realize our proposed circuit using CNFETs. The different application specific parameters of the proposed trigger pulse generator are shown in Table 2. Based upon these parameters, the proposed trigger pulse generator can be used as a firing circuit for silicon controlled rectifier (SCR). Such microwave pulses also find application in military communication applications, thermoacoustic imaging applications, and low power microwave transceiver ICs [23, 24].

Table 2: Different parameter of SCR and proposed trigger pulse generator.

Parameters	SCR ratings	Proposed trigger circuit
Gate current (I_G)	30 mA	25 μA–40 mA
Drive voltage	1-2 V	700–1500 mV
Trigger pulse duration	5–20 μs	88.6 ps (min)
dI_G/dt	≥2 A/μs	≈11.36 A/μs (CNFET)
Pulse rise time (t_r)	≤1 μs	≤10 ns (CNFET)

7. Conclusion

This paper proposes an efficient and compact design of buffered delay circuit capable of incorporating delays in the order of picoseconds (88.6 ps at supply voltage of 700 mV). The proposed buffered delay circuit has been also realized using the different technologies such as FinFET and CNFET, to see the variation in the delay incorporated by the proposed circuit due to influence of these emerging technologies. The simulation results illustrate that the CNFET based proposed buffered delay circuit is capable of incorporating more precise delays and is also immune to variations due to the supply voltage as compared to MOS and FinFET based designs. Further, this work also proposes a trigger pulse generator using the proposed buffered delay circuit and an additional XOR circuit. Overcoming the demerits of conventional methods of trigger pulse generation, our proposed design is also capable of generating highly precise trigger pulses with flexibility to control pulse durations (delay) which can be controlled by providing additional delays between two XORed signals. The effectiveness of the proposed trigger pulse generator has been proved by generating trigger pulses in the order of picoseconds. The push-pull arrangement avoids serious mismatch issues, thus minimizing the effects caused due to process variations. The proposed pulse generator can be used to trigger different circuits whose requirements match the results obtained in this paper.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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