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Research Article

A Novel Inverter Topology for Single-Phase Transformerless PV System

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Transformerless photovoltaic (PV) power system is very promising due to its low cost, small size, and high efficiency. One of its most important issues is how to prevent the common mode leakage current. In order to solve the problem, a new inverter is proposed in this paper. The system common mode model is established, and the four operation modes of the inverter are analyzed. It reveals that the common mode voltage can be kept constant, and consequently the leakage current can be suppressed. Finally, the experimental tests are conducted. The experimental results verify the effectiveness of the proposed solution.

1. Introduction

The transformerless PV inverter has the prominent advantages of the small size, low cost, and high efficiency [1]. And more and more commercial transformerless PV inverters have been developed in recent years. However, there is no galvanic isolation between the input and output sides of the transformerless inverter, so it is prone to common mode leakage current problems [2]. The common mode leakage current not only affects the electromagnetic compatibility of the inverter [3], but also leads to the potential human safety problems [4].

In order to solve this problem, Sunways Company developed HERIC inverter [5]. SMA Company developed H5 inverter [6]. Xiao and Xie presented a leakage current analytical model [7] and then developed the new optimized H5 [8], and split-inductor neutral point clamped inverters [9]. Cavalcanti et al. developed the space vector modulation techniques for three-phase two-level [10] and three-level [11] inverters. Guo et al. developed the carrier modulation techniques for three-phase inverters [12]. Yang et al. [13], Zhang et al. [14], and San et al. [15] developed the improved H6 inverter. And there is an increasing attention to develop the new inverter for transformerless PV applications.

The main contribution of this paper is to develop a new single-phase transformerless PV inverter. Compared with HERIC in [5], only one auxiliary switch and gating driver are needed in the proposal. While in HERIC, two auxiliary switches are needed. Also, two auxiliary gating drivers should be designed for two auxiliary switches. Therefore, the proposal is more cost-effective and reliable, due to less auxiliary switches and gating drivers are used. On the other hand, three semiconductors conduct current during modes 2 and 4. While in Heric, two semiconductors conducts current during modes 2 and 4. Therefore, the main difference is that one additional diode loss. With the development of the commercially available Sic diode, the diode loss will be very small. So this difference due to one additional diode loss would be small. Finally, the theoretical analysis and experimental results validate the proposed solution.

2. Proposed Topology

Figure 1 illustrates the schematic diagram of the proposed single-phase inverter. It consists of five switches and four diodes. C_{PV} is the parasitic capacitance between PV array and ground. The capacitance value depends on many conditions such as the PV panel frame structure, weather conditions, and humidity, and it is generally up to 50–150 nF/kW. V_g is the grid voltage, and V_d is the dc bus voltage. L_a and L_b are filter inductors, respectively.

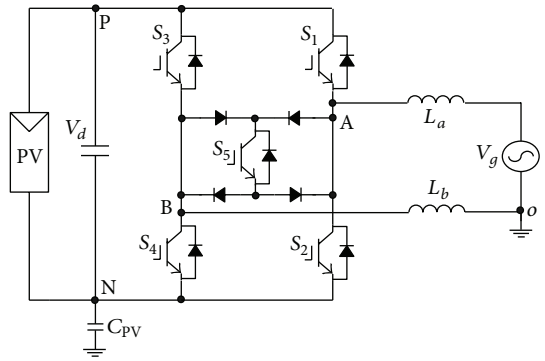


Figure 1: Schematic diagram of proposed inverter.

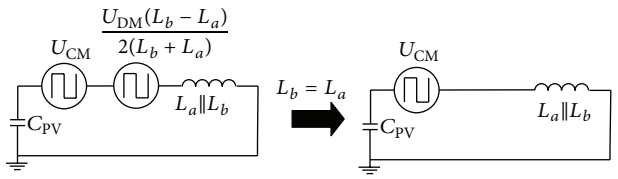


Figure 2: System common mode model.

The common mode voltage and differential mode voltage are defined as

$$U_{CM} = \frac{U_{AN} + U_{BN}}{2}, \qquad U_{DM} = U_{AN} - U_{BN}. \tag{1}$$

From (1), the following voltage equations can be obtained:

$$U_{AN} = U_{CM} + \frac{U_{DM}}{2}, \qquad U_{BN} = U_{CM} - \frac{U_{DM}}{2}. \tag{2}$$

Figure 2 shows the system common mode model. It can be observed that the differential mode voltage has the effect on the system common mode current if $L_b \neq L_a$. Therefore, the filter inductance of L_a should be designed the same value as that of L_b; that is, $L_a = L_b$. So the differential mode voltage will not contribute the common mode current, as shown in Figure 2 [15]. Note that the common mode current is mainly due to the high frequency switching components. Therefore, the effect of grid voltage on the common mode voltage is neglected, because its frequency is much lower than the switching frequency [2].

On the other hand, from Figure 2, it can be observed that the common mode leakage current will be eliminated on condition that the common mode voltage U_{CM} can be kept constant all the time. The reason is that the common mode leakage current, which passes through C_{PV}, depends on $C_{PV}(dU_{C_{PV}}/dt)$. When the common mode voltage U_{CM} is constant, the voltage across C_{PV} is constant as well. That is $dU_{C_{PV}}/dt = 0$. Therefore, the common mode leakage current can be eliminated if the common mode voltage U_{CM} is constant. In order to achieve this goal, the following will present the operation principle.

Table 1: Four operation modes and common mode voltage.

	S_1	S_2	S_3	S_4	S_5	U_{AN}	U_{BN}	U_{CM}
Mode 1	1	0	0	1	0	V_d	0	$V_d/2$
Mode 2	0	0	0	0	1	$V_d/2$	$V_d/2$	$V_d/2$
Mode 3	0	1	1	0	0	0	V_d	$V_d/2$
Mode 4	0	0	0	0	1	$V_d/2$	$V_d/2$	$V_d/2$

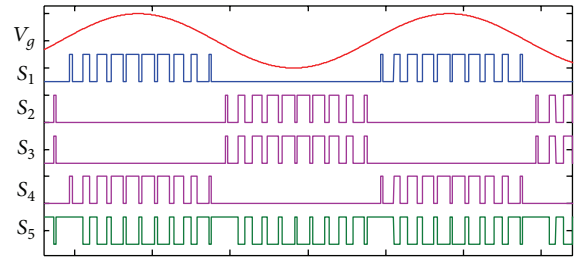


Figure 3: Switching state of the proposed inverter.

The proposed inverter operates in four modes, as shown in Figure 3 and Table 1.

In Mode 1, the switches S_1 and S_4 turn on, and other switches turn off. The differential mode voltage U_{AB} is equal to the dc bus voltage of V_d, while the common mode voltage can be expressed as

$$U_{CM} = \frac{1}{2}(U_{AN} + U_{BN}) = \frac{1}{2}(V_d + 0) = \frac{V_d}{2}. \tag{3}$$

In Mode 2, only the switch S_5 turns on, and other switches turn off. The current flows through S_5 and diodes. In this case, the differential mode voltage U_{AB} is 0, while the common mode voltage remains unchanged as

$$U_{CM} = \frac{1}{2}(U_{AN} + U_{BN}) = \frac{1}{2}\left(\frac{V_d}{2} + \frac{V_d}{2}\right) = \frac{V_d}{2}. \tag{4}$$

In Mode 3, the switches S_2 and S_3 turn on, and other switches turn off. The differential mode voltage U_{AB} is $-V_d$, while the common mode voltage can be expressed as

$$U_{CM} = \frac{1}{2}(U_{AN} + U_{BN}) = \frac{1}{2}(0 + V_d) = \frac{V_d}{2}. \tag{5}$$

In Mode 4, only the switch S_5 turns on, and other switches turn off. The current flows through S_5 and diodes. In this case, the differential mode voltage U_{AB} is 0, while the common mode voltage remains unchanged as

$$U_{CM} = \frac{1}{2}(U_{AN} + U_{BN}) = \frac{1}{2}\left(\frac{V_d}{2} + \frac{V_d}{2}\right) = \frac{V_d}{2}. \tag{6}$$

From the above theoretical analysis, it can be observed that the common mode voltage remains constant during the whole operation cycle. Consequently, the common mode leakage current can be significantly suppressed, according to theoretical analysis of Figure 2.

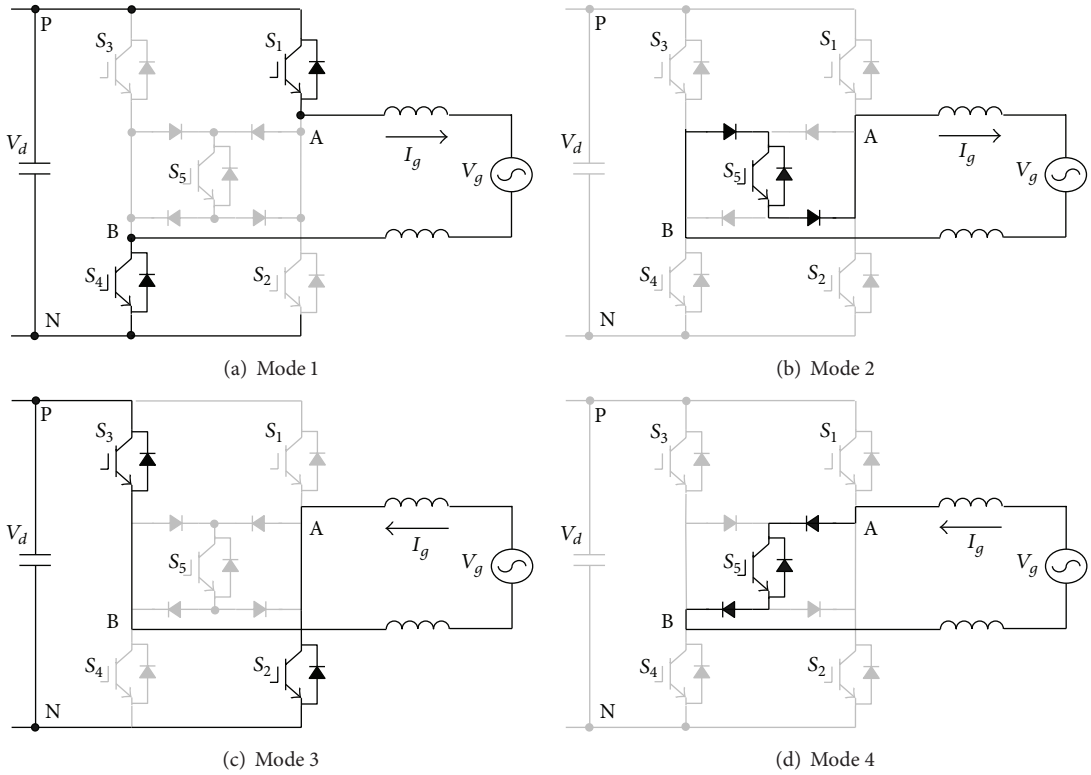


Figure 4: Operation modes of the proposed.

The system design in terms of passive and active components is presented as follows. The rated system power is 1.5 kW, dc bus voltage V_d is 400 V, grid voltage V_g is 220 Vac, grid frequency is 50 Hz, and inverter switching frequency is 10 kHz.

First of all, the active components such as the switches are designed in terms of the operating voltage, on-state current. The rated voltage and current stresses of switches (S_1, S_2, S_3, S_4, S_5) and diodes are 400 V and 10 A, respectively. Therefore, the IRG4IBC30S IGBT from International Rectifier is selected for five switches (S_1, S_2, S_3, S_4, S_5). Its collector-to-emitter breakdown voltage is 600 V, and the continuous collector currents are 23.5 A and 13 A, respectively, in case of $T_C = 25^\circ$C and $T_C = 100^\circ$C. The diode is FR20J02GN-ND from GeneSiC Semiconductor.

Another design consideration is the filter inductor. Its inductance can be calculated according to the commonly used design criterion, in which the maximum current ripple magnitude is less than 10% of the rated current. The filter inductor current ripple can be calculated from Figure 4 as follows.

In mode 1, the inductor current increases:

$$V_d - V_g = V_d - V_m \sin \omega t = \left(L_a + L_b\right) \frac{\Delta I_1}{T_1}, \tag{7}$$

where V_m and ω is the amplitude and angular frequency of the grid voltage and T_1 is the time interval of mode 1.

In mode 2, the inductor current decreases:

$$-V_m \sin \omega t = \left(L_a + L_b\right) \frac{\Delta I_2}{T_2}, \tag{8}$$

where T_2 is the time interval of mode 2, $T_1 + T_2 = T_s$, and T_s is the switching cycle.

In steady state, $|\Delta I_1| = |\Delta I_2|$. So $(V_d - V_m \sin \omega t)T_1 = (V_m \sin \omega t)T_2$. Considering $T_1 = T_s - T_2$, we can obtain

$$T_2 = \frac{\left(V_d - V_m \sin \omega t\right)}{V_d} T_s. \tag{9}$$

Substituting (9) into (8), the inductor current ripple can be calculated as follows:

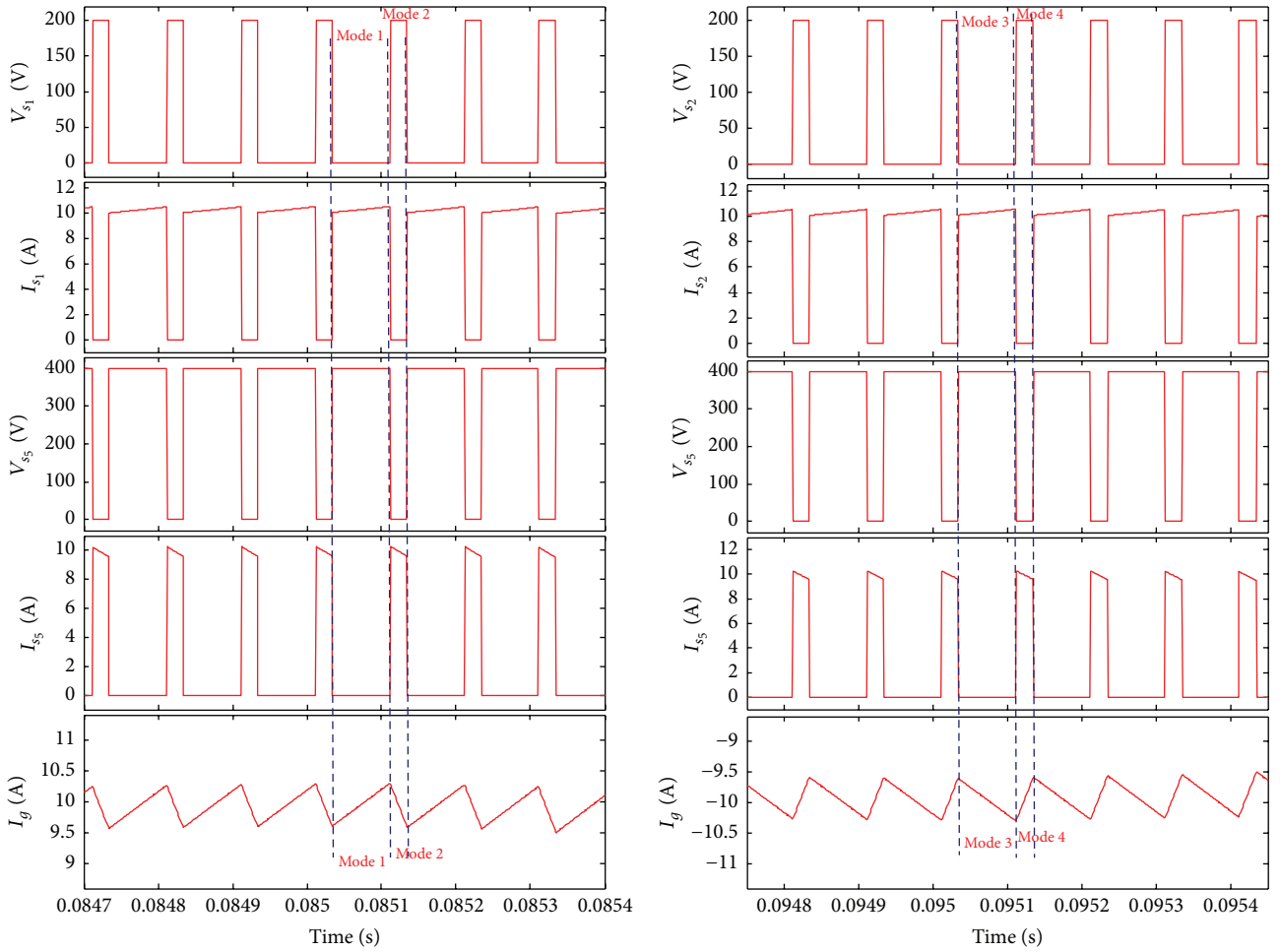
$$\begin{aligned} \left|\Delta I_2\right| &= \left| \frac{-V_m \sin \omega t}{L_a + L_b} T_2 \right| \\ &= \frac{V_m \sin \omega t}{L_a + L_b} \frac{\left(V_d - V_m \sin \omega t\right)}{V_d} T_s. \end{aligned} \tag{10}$$

The current ripple reaches its maximum value when $V_m \sin \omega t = V_d/2$. In this case, the maximum current ripple is

$$\Delta I_{\max} = \frac{V_d}{4\left(L_a + L_b\right)} T_s. \tag{11}$$

In this paper, V_d is 400 V, T_s is 100 us, the rated current is 10 A, and the maximum current ripple should be less than 1 A; therefore, the filter inductor should be designed as follows:

$$L_a + L_b = \frac{V_d}{4\Delta I_{\max}} T_s \geq 0.01\text{H}. \tag{12}$$



(a) Operation mode 1 and mode 2

(b) Operation mode 3 and mode 4

FIGURE 5: Simulation results showing the operation of the converter.

3. Simulation and Experimental Results

In order to further verify the effectiveness of the proposed inverter, the performance test is conducted in MATLAB/Simulink. The components and parameters are listed as follows: system rated power is 1.5 kW, dc bus voltage V_d is 400 V, grid voltage V_g is 220 Vac, grid frequency is 50 Hz, switching frequency is 10 kHz, filter inductor is $L_a = L_b = 5$ mH, and parasitic capacitor is $C_{\mathrm{PV}} = 150$ nF. The leakage current is obtained by measuring the current through the parasitic capacitor [10].

Figure 5 shows the operation of the proposed converter. The simulation results of the operation mode 1 and mode 2 are shown in Figure 5(a). In agreement with the theoretical analysis in Figure 4(a), when the switches S_1 and S_4 turn on, the collector-to-emitter voltage V_{s_1} of S_1 is approximately zero, and its current I_{s_1} increases with a slope of $(V_d - V_m \sin \omega t)/(L_a + L_b)$. The simulation result waveforms of S_4 are the same as those of S_1 in mode 1 and thus not duplicated here for simplicity.

In mode 2, only the switch S_5 turns on, the collector-to-emitter voltage V_{s_5} of S_5 changes from 400 V (in mode 1) to zero (in mode 2), and its current I_{s_5} decreases with a slope of $-V_m \sin \omega t/(L_a + L_b)$.

The last figure in Figure 5(a) shows the filter inductor current, it can be observed that the inductor current I_g charges (in mode 1) and discharges (in mode 2) during a switching cycle, and the current ripple is less than 1 A, which is in good agreement with the design consideration in Section 2.

The simulation results of the operation mode 3 and mode 4 are shown in Figure 5(b). In agreement with the theoretical analysis in Figure 4(c), when the switches S_2 and S_3 turn on, the collector-to-emitter voltage V_{s_2} of S_2 is approximately zero, and its current I_{s_2} increases in mode 3. In mode 4, only the switch S_5 turns on, the collector-to-emitter voltage V_{s_5} of S_5 changes from 400 V (in mode 3) to zero (in mode 4), and its current I_{s_5} decreases. The last figure in Figure 5(a) shows the filter inductor current, it can be observed that the inductor current I_g charges and discharges during a switching cycle, and the current ripple is less than 1 A, which is in good agreement with the design consideration in Section 2.

Figure 6 shows the simulation results of output waveforms in the time and frequency domains. It can be observed

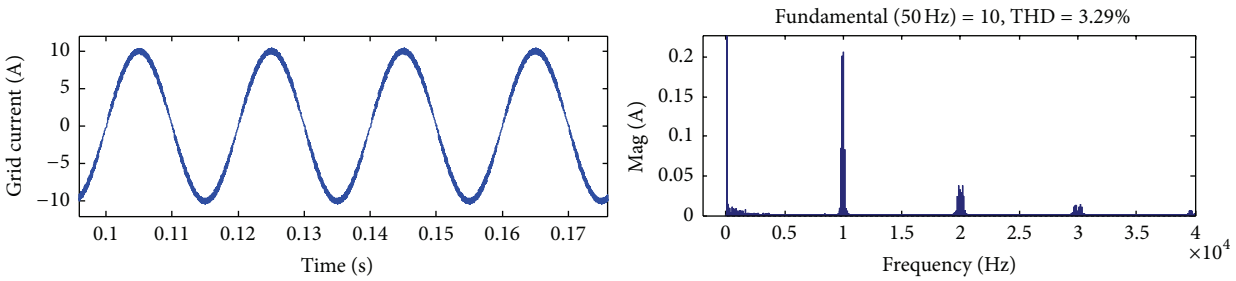
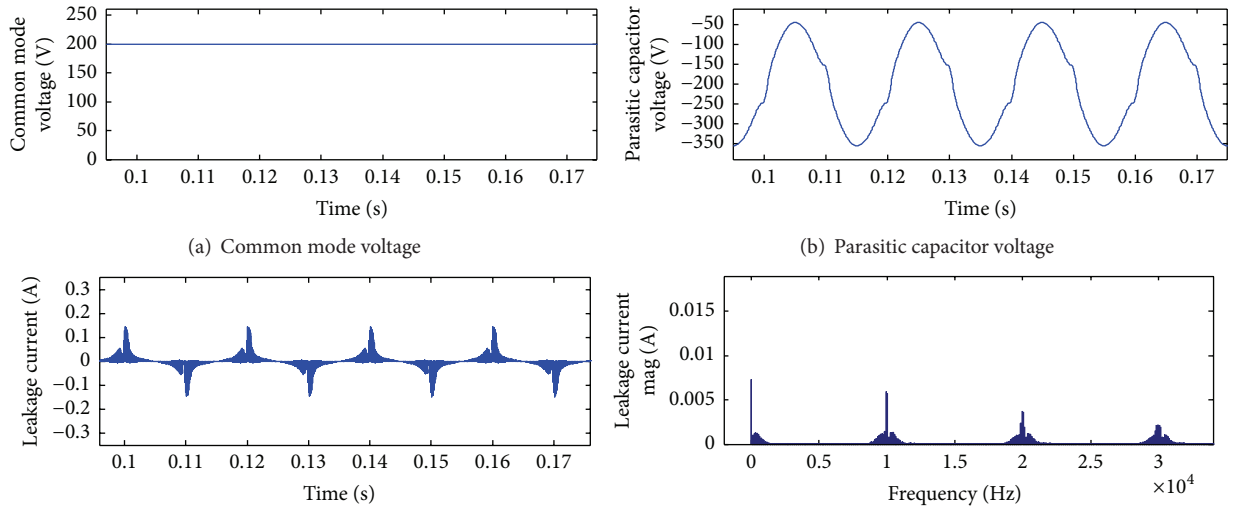


FIGURE 6: Simulation results of output waveforms in the time and frequency domains.



(a) Common mode voltage

(b) Parasitic capacitor voltage

(c) Common mode leakage current and spectrum

FIGURE 7: Simulation results of common mode voltage and leakage current.

that the output grid current is sinusoidal, and its total harmonic distortion (THD) is well below 5%, as specified in IEEE Std. 929-2000.

The simulation results of the common mode voltage and leakage current are shown in Figure 7. It can be observed that the common mode voltage is constant, which is in agreement with the theoretical analysis in Section 2. On the other hand, the parasitic capacitor voltage does not include any high frequency common mode voltage, and therefore the leakage current is significantly reduced, as shown in Figure 7(c). Its peak value is below 300 mA, and the RMS value is below 30 mA, which meets the international standard VDE 0126-1-1.

As shown in Figure 8, with the proposed topology, it can be observed that the parasitic capacitor voltage has only the fundamental frequency component, without any high frequency components. Therefore, the leakage current can be effectively reduced below 300 mA, which complies with the international standard VDE 0126-1-1.

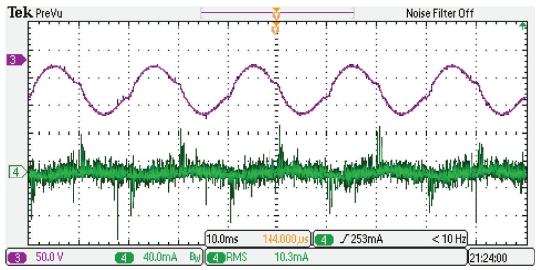


FIGURE 8: Experimental results of parasitic capacitor voltage and leakage current.

4. Conclusion

This paper has presented the theoretical analysis and experimental verification of a new inverter for transformerless PV systems. The proposed inverter has the following interesting features. It can keep the system common mode voltage constant during the entire operation cycle. Consequently, the common mode leakage current can be significantly reduced well below 300 mA, which meets the international standard VDE 0126-1-1. Therefore, it is attractive and a promising alternative topology for transformerless PV system applications.

Conflict of Interests

The author declares that there is no conflict of interests regarding publication of this paper.

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