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Research Article

Bus Implementation Using New Low Power PFSCL Tristate Buffers

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This paper proposes new positive feedback source coupled logic (PFSCL) tristate buffers suited to bus applications. The proposed buffers use switch to attain high impedance state and modify the load or the current source section. An interesting consequence of this is overall reduction in the power consumption. The proposed tristate buffers consume half the power compared to the available switch based counterpart. The issues with available PFSCL tristate buffers based bus implementation are identified and benefits of employing the proposed tristate buffer topologies are put forward. SPICE simulation results using TSMC 180 nm CMOS technology parameters are included to support the theoretical formulations. The performance of proposed tristate buffer topologies is examined on the basis of propagation delay, output enable time, and power consumption. It is found that one of the proposed tristate buffer topology outperforms the others in terms of all the performance parameters. An examination of behavior of available and the proposed PFSCL tristate buffer topologies under parameter variations and mismatch shows a maximum variation of 14%.

1. Introduction

Conventional CMOS circuits are widely used in digital integrated circuit design due to their design ease, high packing density, and negligible static power consumption [1]. The large switching noise generation in CMOS circuits restricts their use in applications pertaining to mixed-signal environment [2, 3]. Research efforts are, therefore, made towards exploring alternate low-noise logic styles. These logic styles are based on the current steering principle [4–7] and draw a constant current from power supply and generate low switching noise in comparison to CMOS logic style. Positive feedback source coupled logic (PFSCL) style [6–10] is one among these styles that works on current steering principle and is used in high speed designs.

This paper addresses implementation of PFSCL busses employed to transfer data between various peripherals inside the microprocessors based systems in mixed-signal environments. A typical bus system has many tristate buffers attached to a common node. The study of PFSCL tristate buffers/inverters reveals that only two topologies are available [11]. These topologies use either a switch or a sleep transistor to attain the tristate behavior. The suitability of the sleep transistor and the switch transistor based PFSCL tristate buffers [11] in bus system implementation is investigated and the drawbacks are identified. New PFSCL tristate buffers for this purpose are presented in this work.

The paper is organized in six sections including the introductory one. A brief review of available PFSCL tristate buffers is presented in Section 2. Design issues in implementing bus system using the available tristate buffers are identified in Section 3. Thereafter, the new PFSCL tristate buffer topologies are presented in Section 4. Their performance comparison and suitability in bus implementation are demonstrated through SPICE simulations by using TSMC 180 nm CMOS technology parameters in Section 5. The impact of parameter variations and the effect of parameter mismatch are also studied for the proposed topologies. Lastly, the paper is concluded in Section 6.

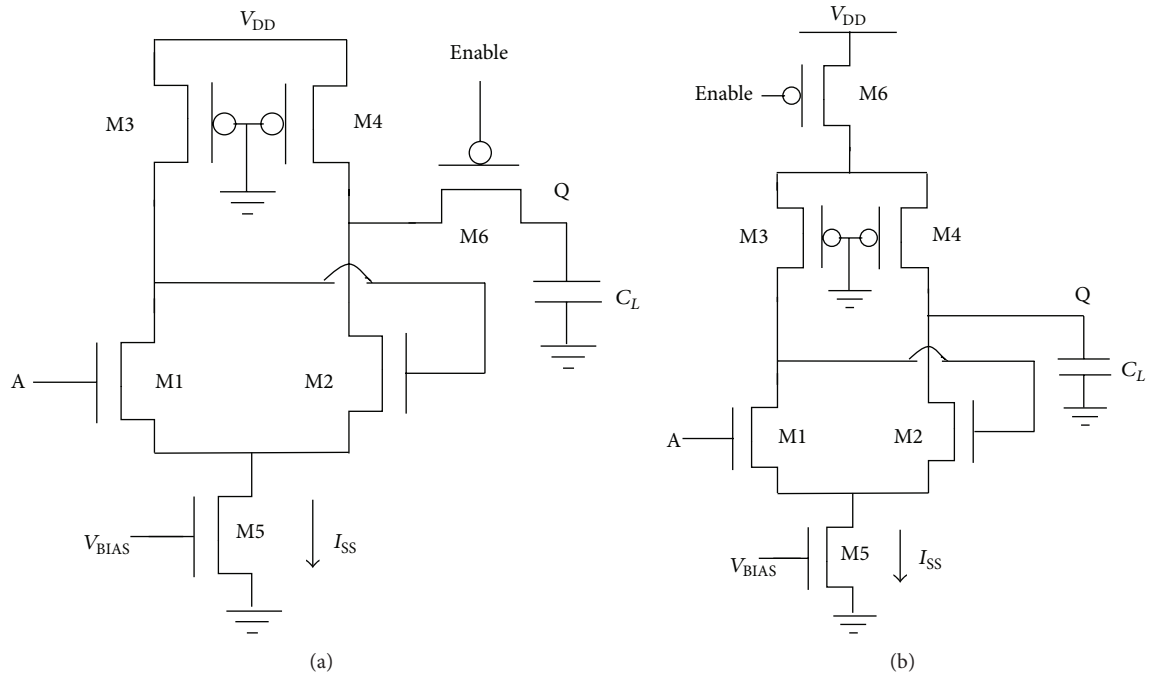

Figure 1: Available PFSCL tristate buffers [11]: (a) switch based; (b) sleep based.

2. Available PFSCL Tristate Buffers

A tristate gate exhibits a high impedance state in addition to high and low logic levels attained by a regular gate. An additional Enable signal is employed to achieve the desired functionality. In literature, two topologies to implement PFSCL tristate buffer are available [11]. These topologies use either a switch or a sleep transistor to attain a high impedance state.

A switch based PFSCL tristate buffer is shown in Figure 1(a). A transistor M6 is added to the output of the regular PFSCL gate to achieve tristate operation. For low value of Enable signal, transistor M6 is ON and the circuit acts as a regular buffer. Conversely, a high value of Enable signal turns transistor M6 OFF and provides a high impedance state at the output by disconnecting the regular buffer output to the actual output node Q. Therefore, it can be noted that this tristate buffer maintains a current in the circuit irrespective of the state of gate.

The other PFSCL tristate buffer [11], drawn in Figure 1(b), uses a sleep transistor M6 in series to the power supply terminal of the basic PFSCL buffer. It acts as regular buffer for low value of Enable signal by turning ON transistor M6 while providing a high impedance state at the output, otherwise. The sleep based tristate buffer is claimed to be more power efficient than the switch based counterpart due to the fact that there are no current flows in the circuit (Figure 1(b)) during high impedance state.

3. Issue in Bus Implementation

The discussion on the available PFSCL tristate buffers indicates that the sleep based topology is more power efficient than the switch based counterpart. However, bus implementation using sleep transistor based PFSCL tristate buffers suffers a major drawback of incomplete isolation of the common output node from the tristate disabled buffers.

To illustrate this, a typical bus environment consisting of two tristate buffers driving a common output node is considered. The test bench is shown in Figure 2(a). In this environment, for a low value of Enable signal, B1 is enabled while B2 operates in high impedance state and vice versa. The test bench is simulated by using the sleep and the switch based tristate buffers and the corresponding complete MOS based schematics are shown in Figures 2(b) and 2(c). When the sleep based tristate buffers are employed (Figure 2(b)), a low value of Enable signal enables B1 whereas B2 moves in high impedance state by disconnecting the output node from its power supply. In this condition, on careful examination of the circuit, it is found that as the pull-down network (PDN) of B2 is still connected to the output node, a path for the current to flow from the power supply of B1 to ground via the output node Q and B2 still exists. To make this point clear let us consider both inputs A and B as high. In this condition transistor M1 of buffer B1 and both the transistors in PDN of buffer B2 would be ON leading to drawing more bias current from power supply than that of an individual enabled buffer. It is pictorially represented in Figure 2(b) by marking ON transistors by bold lines and OFF transistors by dotted lines. The tick mark in the figure signifies a current flow in the current source section. Hence, the isolation of the output node Q from the buffer B2 is not established. This causes malfunctioning of the whole bus system by altering the magnitude of the high and low logic levels. The degradation in the output levels will increase with

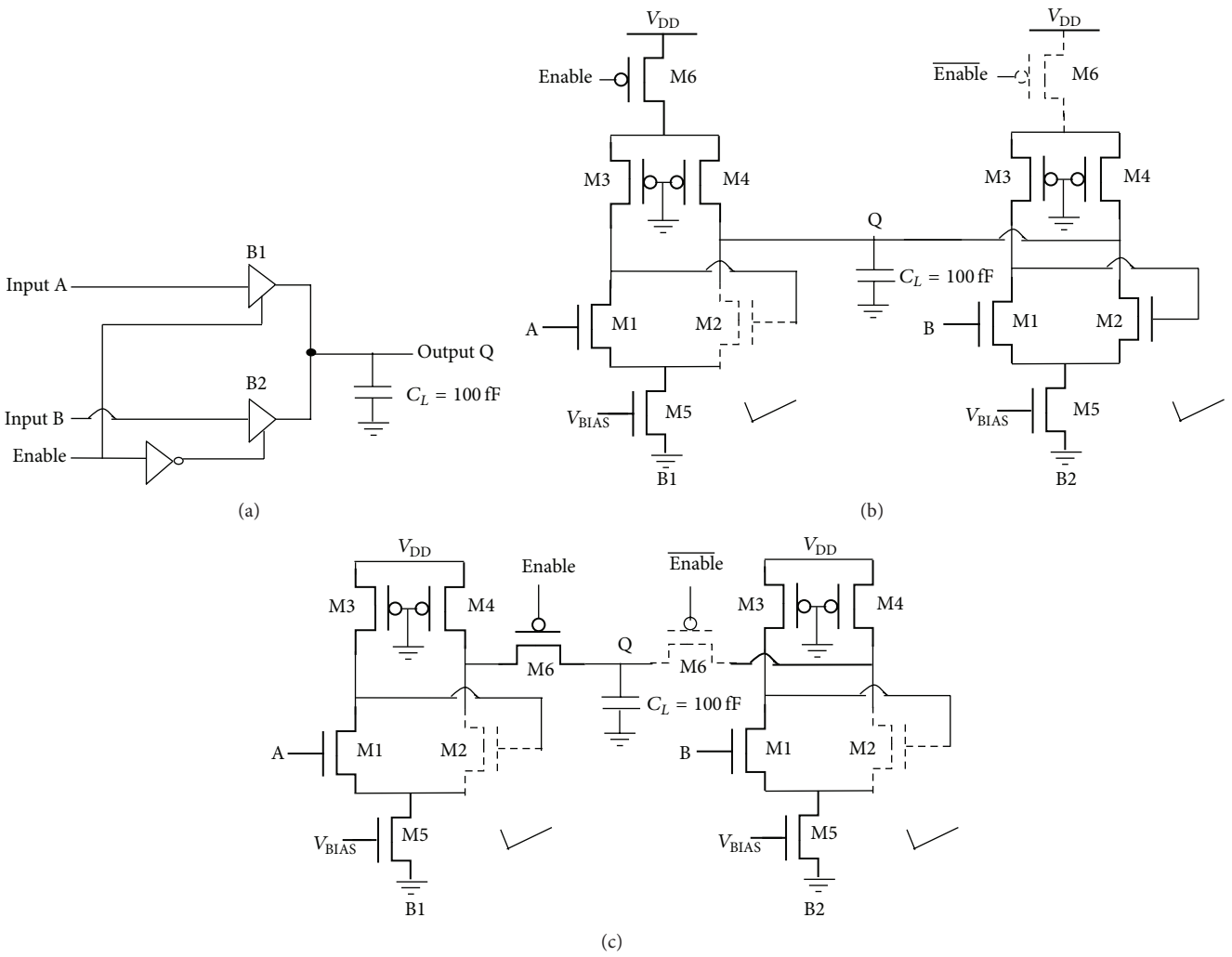

Figure 2: (a) Simulation test bench. (b) Bus operation by using sleep based tristate buffers. (c) Bus operation by using switch based tristate buffers.

the increase in number of gates connected to the common node Q. Also the functionality of the device which will be driven by the output of sleep based tristate buffer may completely be disrupted.

For the switch based tristate buffer based bus implementation (Figure 2(c)), a low value of Enable signal makes switch transistor M6 of buffer B1 ON and that in buffer B2 OFF. The ON and OFF transistors for inputs A and B high are shown by bold and dotted lines whereas a tick mark represents a current flow in the current source section in Figure 2(c) for the sake of completeness. It is, therefore, clear that the output follows input A and remains unaffected by input B. It, however, lacks in terms of power as both buffers draw current from the power supply irrespective of their state, that is, enabled or disabled.

The timing waveforms demonstrating this behavior are shown in Figure 3. The test bench is simulated with a power supply of 1.8 V and a voltage swing of 400 mV is considered for the inputs. It can be observed that correct voltage levels at the output are achieved for the switch based ones in contrast to the sleep based bus system.

4. New PFSCL Tristate Buffer Topologies

In this section, new PFSCL tristate buffer topologies derived from the available switch based tristate buffer are presented. All the topologies use an output switch to attain the high impedance state and save power by not allowing the current flow in the high impedance state. The current flow is restricted by modifying either the load or the current source section of the PFSCL switch based tristate buffer. The resulting topologies are accordingly classified into two categories. The topologies with the modified load section are presented first and are followed by the topologies with modified current source section.

4.1. PFSCL Tristate Buffer with Modified Load Section (Proposed Topology 1). This topology modifies the load by driving

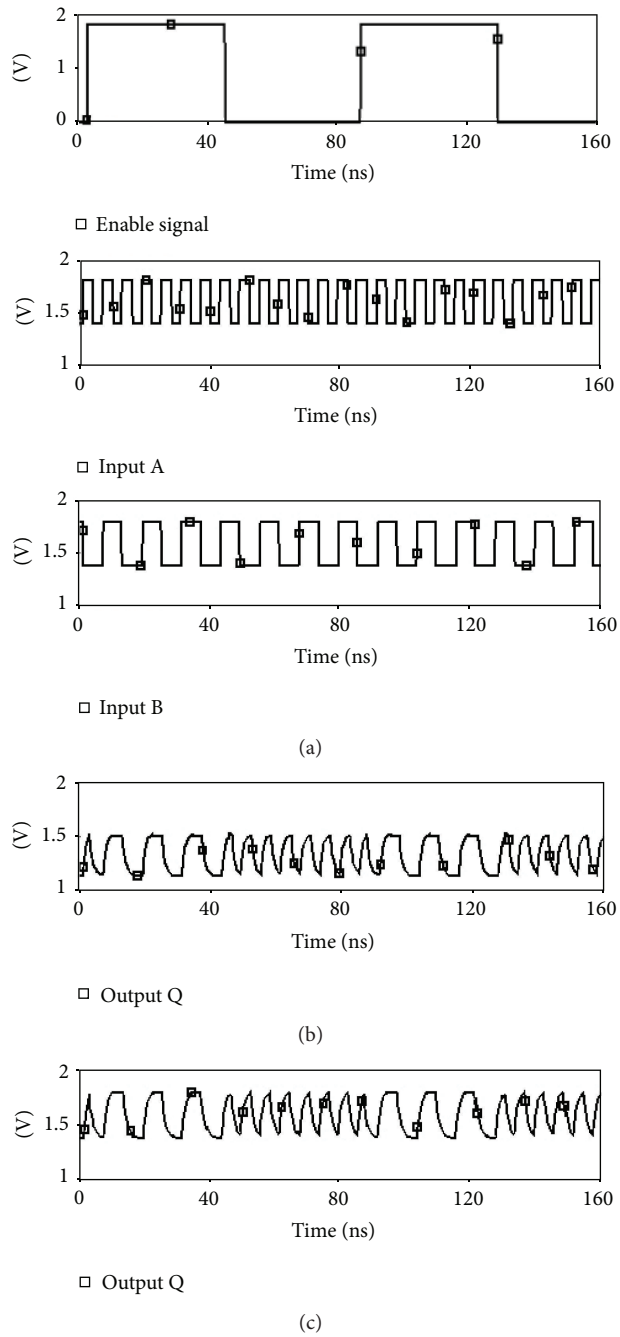

Figure 3: Timing waveform for bus implementation; (a) input signals: Enable, A, and B; (b) output of sleep transistor based bus; (c) output of switch transistor based bus.

the load transistors with an Enable signal instead of a fixed ground potential. The resulting topology is depicted in Figure 4. For a low value of Enable signal, the circuit behaves as a regular PFSCL buffer. On the contrary, for high value of Enable signal transistors M3, M4, and M6 are OFF so the buffer enters in the high impedance state and restricts the current flow in the circuit thereby providing overall reduction in power consumption.

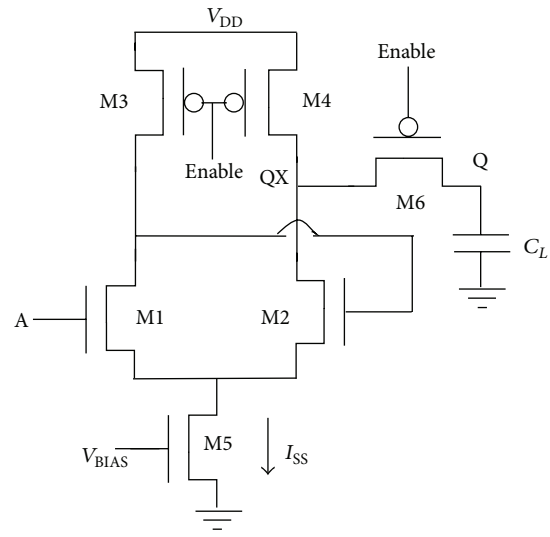

Figure 4: Proposed topology 1.

4.2. PFSCL Tristate Buffers with Modified Current Source Section

4.2.1. Proposed Topology 2. This topology modifies the current source section by adding a PMOS transistor M7 below the current source transistor M5 as shown in Figure 5(a). When Enable signal is low, the circuit behaves as a regular PFSCL buffer. Conversely, for high value of Enable signal, the transistors M6 and M7 are OFF. This allows the circuit to enter high impedance and avoids any current flow in this duration.

4.2.2. Proposed Topology 3. In proposed topology 2, the addition of the PMOS transistor below the current source requires a higher value of bias voltage (V_{BIAS}) in comparison to the one required in conventional PFSCL buffer in order to maintain the same current value (I_{SS}). This situation can be addressed by altering the placement of the transistors M5 and M7 as shown in Figure 5(b). A low value of Enable signal allows normal operation by providing a path to ground via transistor M7. Analogously, for a high value of Enable signal the path to ground is disconnected by turning OFF the said transistor. At this point, the transistor M6 is OFF; therefore, the circuit enters the high impedance state and does not consume power.

4.2.3. Proposed Topology 4. Proposed topologies 2 and 3 use stacking of the transistors in the current source section to reduce power consumption. In proposed topology 4, an alternate approach to avoid current flow in the circuit is presented. The availability of bias voltage to the current source is made dependent on Enable signal by using a PMOS transistor M7 and an NMOS transistor M8 as shown in Figure 5(c). For a low value of Enable signal, the transistor M5 receives the necessary biasing through transistor M7. At this point the transistor M6 is ON and the topology behaves

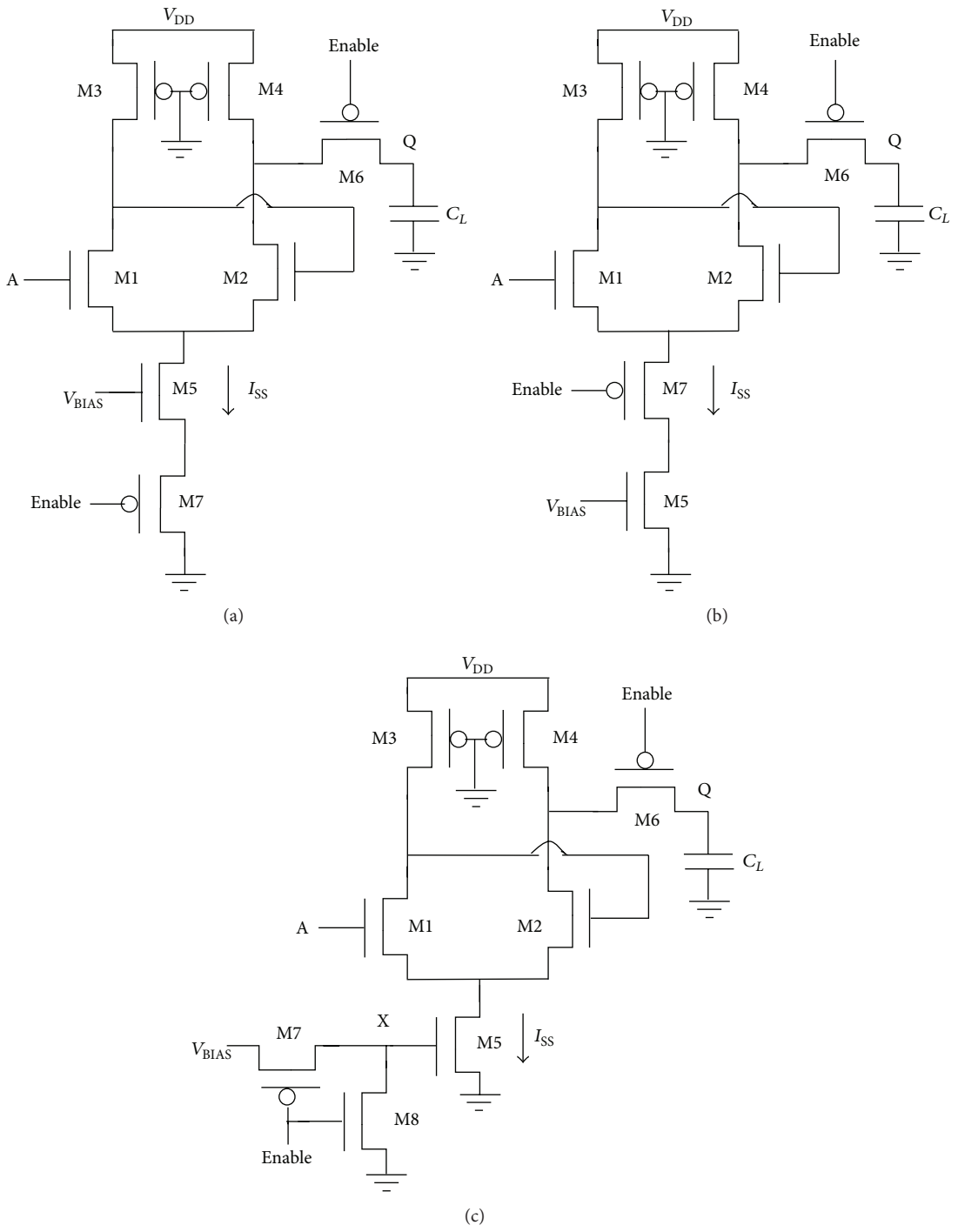

Figure 5: Proposed PFSCL tristate buffer: (a) topology 2, (b) topology 3, and (c) topology 4.

as a regular buffer. Conversely, when Enable signal is high, the transistor M7 is OFF and the transistor M8 is ON. This discharges the potential of node X to the ground potential and consequently disables the current source. Therefore, the buffer does not consume power and high impedance state is achieved as transistor M6 is turned OFF.

5. Simulation Results and Discussion

The section first compares performance of proposed PFSCL tristate buffers and thereafter verifies their suitability for bus system implementations through simulations. The TSMC 180 nm CMOS technology parameters and power supply of

Table 1: Summary of performance parameters for proposed and available PFSCL tristate buffers.

Tristate buffer	Parameter			
	Propagation delay (ps)	Output enable time (ps)	Power (μW)	Power delay product (fJ)
Proposed topology 1	425	553	45	19.125
Proposed topology 2	419	348	45	18.855
Proposed topology 3	408	132	45	18.360
Proposed topology 4	428	438	45	19.260
Switch based buffer [11]	430	182	90	38.700

1.8 V are taken in all the SPICE simulations. The bias current and voltage swing of 50 μA and 400 mV, respectively, are considered *for all PFSCL tristate buffers* uniformly.

5.1. Performance Comparison. The proposed PFSCL tristate buffer topologies 1–4 (Figures 4 and 5) and available switch based PFSCL tristate buffer (Figure 1(a)) are simulated with a load capacitance of 50 fF. The performance is compared in terms of propagation delay, output enable time, power consumption, and power delay product. The simulation results are summarized in Table 1.

It is found that all the proposed topologies consume half the power compared to the available switch based PFSCL tristate buffer [11] due to the fact that they all possess the provision of disabling the current flow in the high impedance state. In terms of propagation delay, it can be observed that all the topologies have almost equal delays since all of these possess similar loads and maintain the same bias current in the enabled state. These two factors account for the low power delay product values for the proposed topologies in comparison to the available one. A maximum reduction of 47% in the power delay product is obtained in proposed topologies.

There is a variation in the output enable time of the tristate buffers which, therefore, needs little more investigation on the behavior during high impedance state.

(i) For proposed topology 1 (Figure 4), wherein the load is modified, it is to be noted that transistors in the pull-down network (M1-M2) and current source (M5) sections are ON. This condition leads to discharging of node QX to the ground potential. Subsequently, when the gate is enabled, the node QX will attain the valid low or high voltage levels depending upon the applied input. This explains longer output enable time in proposed topology 1.

(ii) For proposed topologies 2–4 (Figure 5), current source section is modified. Out of these three, topology 4 (Figure 5(c)) shows the longest output enable time. It can be attributed to the fact that a proper V_{BIAS}, at node X, will be established through M7 whereas, in the remaining two topologies, the path from common source coupled point to the ground is instantly established the moment the buffer is enabled. Topology 2 uses larger bias voltage than topology 3 which explains its longer output enable time.

(iii) Proposed topology 3 shows the best output enable time among the available and the proposed topologies which is due to interaction of internal node capacitances.

The impact of parameter variations is also examined for all proposed and available switch based PFSCL tristate buffers at different design corners and is plotted in Figure 6. It is observed that the proposed tristate buffer topologies show maximum variations in the propagation delay, the output enable time, the power consumption, and the power delay product by a factor of 1.3, 4.35, 1.8, and 1.31 between the best/worst and typical cases, respectively. Similarly, the available switch based PFSCL tristate buffer shows maximum variations by a factor of 1.08, 3.14, 1.55, and 1.14 for all the above performance parameters, respectively.

The effect of width mismatch is also studied for all proposed and available switch based PFSCL tristate buffer topologies. The widths of the transistors are varied by 10% corresponding to which a maximum change of 11% is observed in propagation delay, 14% in output enable time, and 8% in power consumption.

Further, to explore the feasibility of working of proposed topologies at lower potential, it is necessary to compute minimum power supply requirement. Using the method outlined in [12] it is found that the minimum power supply requirement for topologies 1–4 is, respectively, given as

$$\begin{aligned} V_{\text{DD\_MIN\_topology1}} &= 2V_{\text{BIAS}} - V_T, \\ V_{\text{DD\_MIN\_topology2}} &= 2V_{\text{BIAS}} - V_T + \left|V_{TP}\right|, \\ V_{\text{DD\_MIN\_topology3}} &= 2V_{\text{BIAS}} - V_T + I_{\text{BIAS}}R_P, \\ V_{\text{DD\_MIN\_topology4}} &= 2V_{\text{BIAS}} - V_T, \end{aligned} \tag{1}$$

where V_T and V_{TP} are threshold voltages of NMOS and PMOS transistors. V_{BIAS} is the biasing voltage of transistor M5 and R_P is resistance of PMOS transistor. Assuming V_{BIAS} of 0.8 V, the minimum supply voltage for topologies 1 and 4 is 1.1 V. It is equal to 1.6 V for topology 2 and slightly larger than

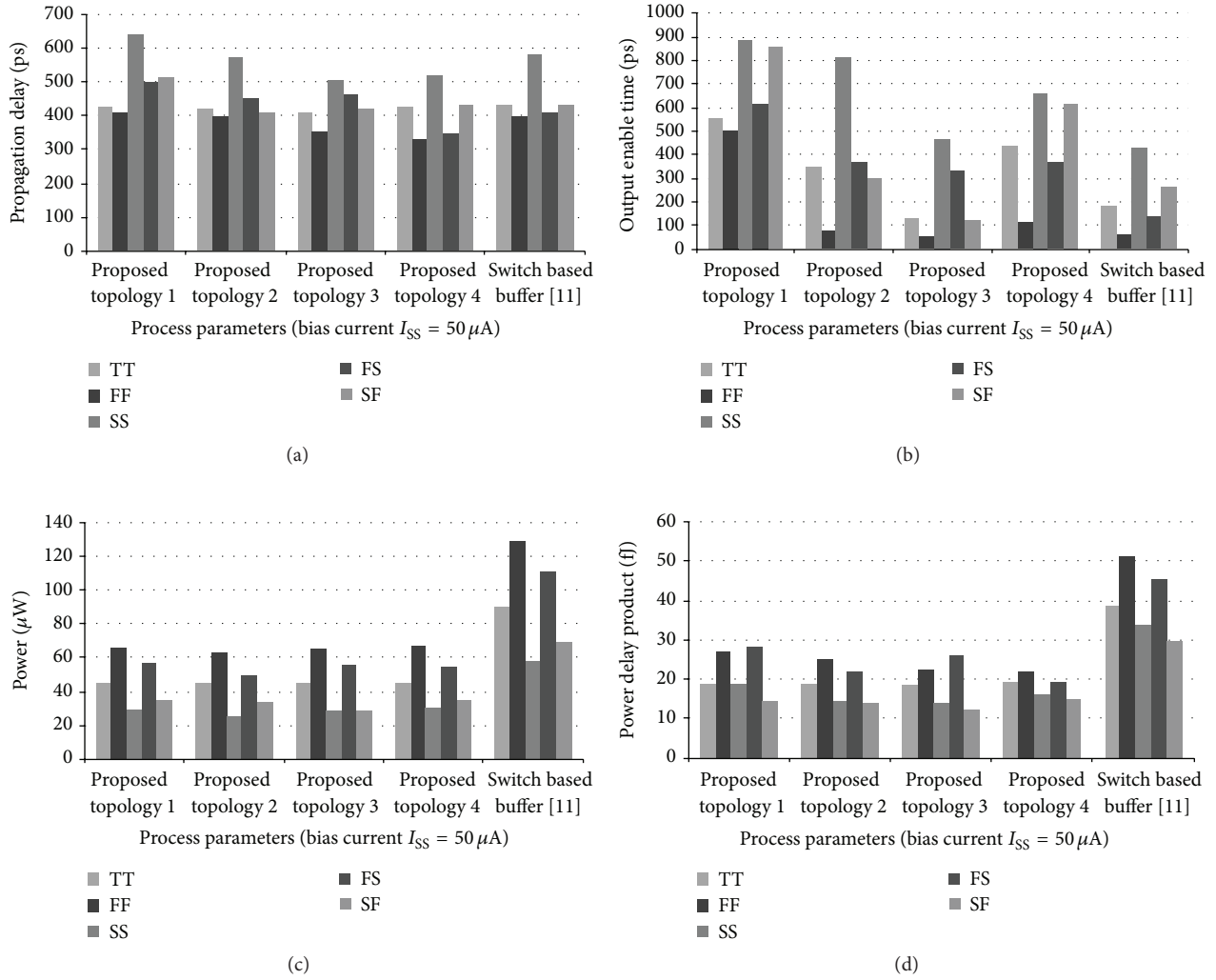

Figure 6: Impact of parameter variations on (a) propagation delay, (b) output enable time, (c) power, and (d) power delay product at different design corners.

1.1 V for topology 3 as $I_{BIAS}R_P$ is very small in comparison to other terms in the expression.

5.2. Bus System Implementation. After performance comparison of the PFSCL tristate buffers, their suitability in bus system implementation is now explored. The test bench shown in Figure 2(a) is considered and is simulated with all proposed and available PFSCL tristate buffer topologies. The simulation waveforms are shown in Figure 7. It is found that all proposed tristate buffers maintain the same voltage levels as the available ones. Also, none of the proposed tristate buffers exhibits the variation in the voltage levels as observed in the case of the sleep based PFSCL tristate buffers. Hence, it can be stated that proposed tristate PFSCL buffers conforms to the functionality.

6. Conclusion

In this paper, implementation of a bus employing tristate PFSCL buffers is presented. The drawbacks in the bus realization using the available PFSCL tristate buffers are put forward and different switch based PFSCL tristate buffer topologies are proposed. The load or the current source sections of the available switch based PFSCL tristate buffer are modified which culminate in reduced power consumption. The performance of proposed buffer topologies is compared through simulations by using 180 nm TSMC CMOS technology parameters. The results indicate that one of the proposed buffer topologies outperforms the others in terms of the propagation delay, the output enable time, and the power consumption. The impact of parameter variations and the effect of parameter mismatch are also included for completeness.

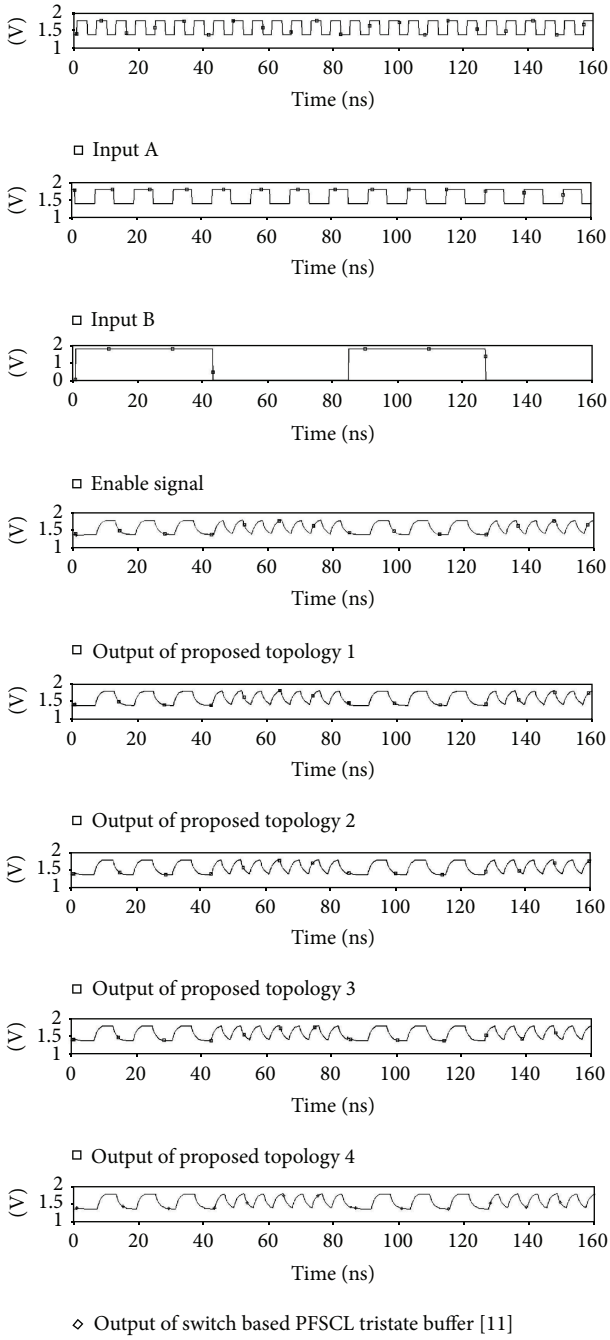

Figure 7: Simulation waveforms of the proposed and available switch based [11] PFSCL tristate buffer topologies.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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