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Research Article

Design and Simulation of a 6-Bit Successive-Approximation ADC Using Modeled Organic Thin-Film Transistors

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We have demonstrated a method for using proper models of pentacene P-channel and fullerene N-channel thin-film transistors (TFTs) in order to design and simulate organic integrated circuits. Initially, the transistors were fabricated, and we measured their main physical and electrical parameters. Then, these organic TFTs (OTFTs) were modeled with support of an organic process design kit (OPDK) added in Cadence. The key specifications of the modeled elements were extracted from measured data, whereas the fitting ones were elected to replicate experimental curves. The simulating process proves that frequency responses of the TFTs cover all biosignal frequency ranges; hence, it is reasonable to deploy the elements to design integrated circuits used in biomedical applications. Complying with complementary rules, the organic circuits work properly, including logic gates, flip-flops, comparators, and analog-to-digital converters (ADCs) as well. The proposed successive-approximation-register (SAR) ADC consumes a power of 883.7 μW and achieves an ENOB of 5.05 bits, a SNR of 32.17 dB at a supply voltage of 10 V, and a sampling frequency of about 2 KHz.

1. Introduction

Although Si-based integrated circuits (ICs) are dominant due to their excellent specifications, such as high precision, high speed, and ultra-low power consumption [1–3], organic ICs have recently emerged as a potential candidate for many applications, for instance, wearable devices and medical sensors. Its unique advantages over Si-based counterpart include flexibility, biocompatibility, and low-cost process [4–6]. In particular in research and development of organic IC, time and cost could be reduced significantly with computer-aided design (CAD) tools [7–10]. Among CAD tools, HSPICE and Cadence Virtuoso are famous for their high accuracy, multifunction, and ease to use. The VLSI group at University of Minnesota built an organic process design kit (OPDK) added in Cadence [11]. The tool supports organic integrated circuit design and simulation, but its library has only a P3HT P-channel OTFT and a CNT unipolar field-effect transistor (FET). In other works, the Spice level 1 MOS model was used to simulate the pentacene circuits [12]. However, a big difference between simulation and measurement results obviously occurred, since the model embraces a few electrical parameters of the charge mobility, threshold voltage, early voltage, and capacitive behavior.

On the other hand, at the circuit level, an analog-digital converter (ADC) plays an important role in signal processing due to its connection between analog and digital world. So far, the organic ADCs have been mainly constructed with P-type technology and those exhibit many limitations, for

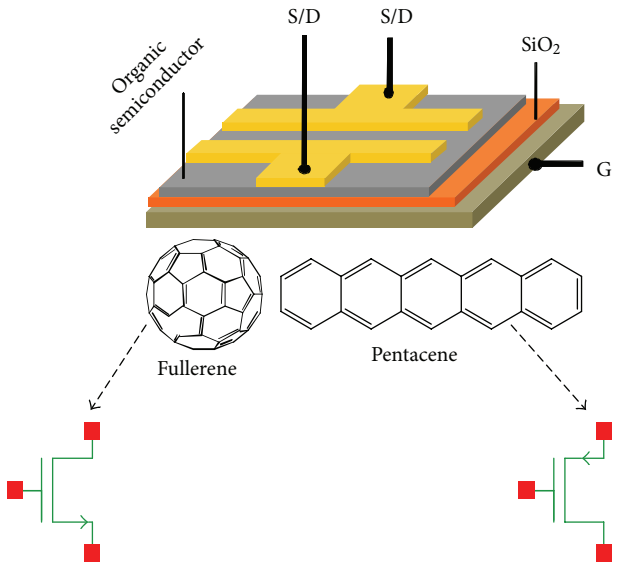

Figure 1: Illustrations of OTFT layout, fullerene, and pentacene molecular semiconductors and circuit symbols of fullerene N or pentacene P-channel OTFTs.

example, low gain, narrow bandwidth, low speed, and high power consumption [12–14].

In this work, widely used fullerene and pentacene OTFTs were fabricated and characterized. Subsequently, we utilized the Spice level 61 with 29 parameters, which originally is developed for amorphous silicon transistor, to improve OPDK models for such OTFTs. Electrical characteristics obtained by simulation matched very well with those from the experiments. The well-developed models of both P-type and N-type OTFTs allow construction of a complex circuit with complementary technology. In later progress, organic logic gates, flip-flops, comparators, and successive-approximation-register (SAR) ADCs were designed and verified in Cadence. The simulation results indicated that our 6-bit SAR ADC operated at a high sampling frequency up to 2 KHz and a relatively low power of about 883 μW.

2. Fabrication and Modeling OTFTs

Figure 1 shows the layout structure of OTFTs and molecular structures of pentacene and fullerene together with the OTFT symbols in Cadence. The OTFTs were fabricated on SOI (Silicon-On-Insulator) wafer with a heavily doped Si (n + Si, resistivity: 1–100 Ω cm) gate electrode coated with a 50 nm SiO_2 insulating layer. The experimental method was detailed in previous report [15]. In short, the substrate was cleaned by ultrasonication; 50 nm thick fullerene and 30 nm thick pentacene layers were thermally deposited on SOI via a designed shadow mask, for N-channel and P-channel, respectively, at a base pressure of 2×10^{-6} torr and deposition rate of 0.1 nm s^{-1}. Finally, Au source-drain electrodes were formed by thermal evaporation at a deposition rate of 0.3 nm s^{-1} through a designed shadow mask under a certain pressure of 2×10^{-6} torr. The channel length L and geometry factor W/L of OTFT devices were 50 μm and 40, respectively. Electrical measurements of the OTFTs were carried out with the Keithley 4200 semiconductor characterization system in a dry nitrogen atmosphere at room temperature in a dark probe station.

Table 1: Main parameters in the OTFT models.

Parameters	OTFTs	
	P-channel	N-channel
μ_0 [cm^2/Vs]	0.25	0.4
V_{th} [V]	−1.62	2
C_{diel} [$\mu F/m^2$]	6.91×10^2	6.91×10^2
V_{aa}	14.695	20
γ	5.28	0.02
λ	0.001	0.001
m	3.5	4
α_{sat}	0.2	0.73

In OTFT elements, drain-source current I_{DS} includes accumulation current and leakage current [15], which is described as

$$I_{DS} = \frac{W}{L} C_{diel} \mu_0 \left(\frac{V_{GS} - V_{th}}{V_{aa}} \right)^{\gamma} (V_{GS} - V_{th}) (1 + \lambda V_{DS}) \cdot \frac{V_{DS}}{\left[1 + \left(V_{DS} / \alpha_{sat} (V_{GS} - V_{th}) \right)^m \right]^{1/m}} + V_{DS} \text{SIGMA0}, \quad (1)$$

where C_{diel} is the gate dielectric capacitance, μ_0 is the mobility, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, V_{aa} is the characteristic voltage for field-effect mobility, γ is the power-law mobility, λ is the output conductance, α_{sat} is the saturation modulation, m is the knee shape parameter, and SIGMA0 is the minimum leakage current parameter. All of them would appear in model files of OTFT elements, so they need to be specified as accurately as possible.

Among those values, the W, L, and C_{diel} are the physical structure parameters; μ_0, V_{th}, γ, V_{aa}, and α_{sat} are extracted from the experimental data [10, 15, 16]. The others are fitting parameters determined by simulating with numerical different values. Accordingly, the optimized parameters of the OTFT models are summarized in Table 1. By using these parameters in Cadence, it allows replicating the electrical behaviors of OTFT elements.

Figures 2 and 3 indicate the transfer and output characteristics from simulation results of P-channel and N-channel OTFTs, which fit well to the experimental curves. These agreements corroborate that our proposed devices are modeled correctly; hence, it is acceptable to use them in organic integrated circuit designs.

Furthermore, we have also investigated operating frequencies of the elements so as to ensure that proposed circuits using these ones would be employed in appropriate applications. The frequency response characteristics at L = 50 μm are reflected in Figure 4(a). It is a general concept that the cut-off frequency f_c is defined as the frequency at which

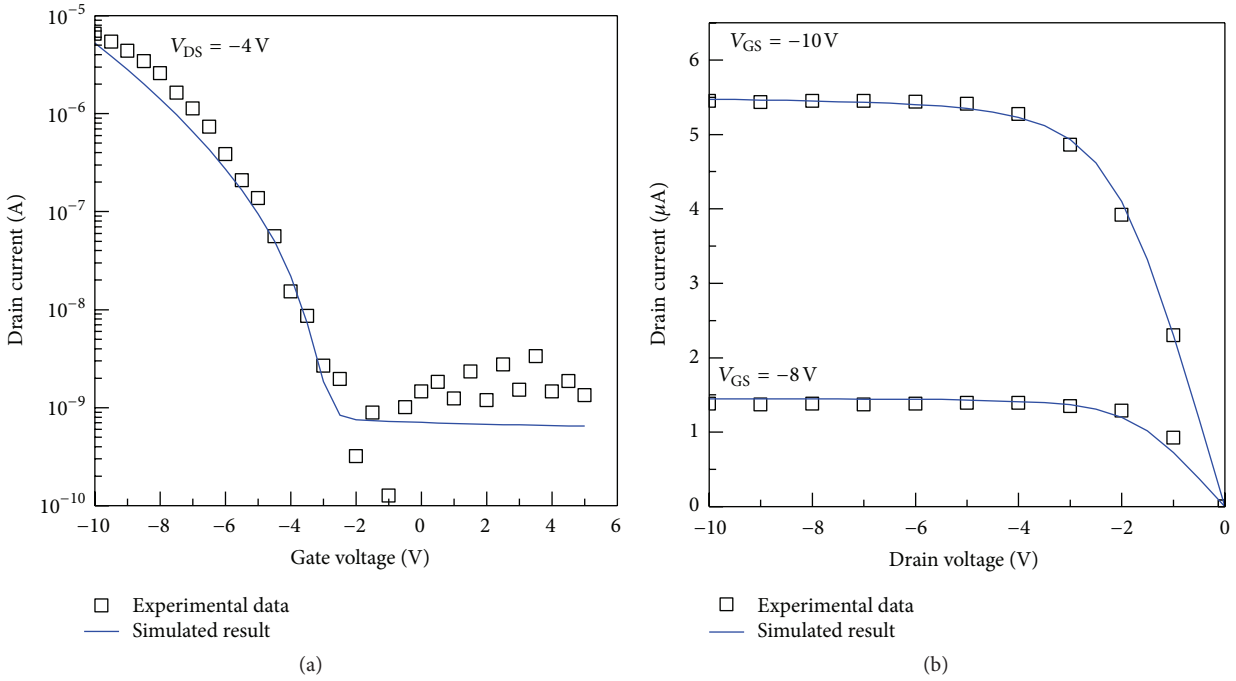

Figure 2: Characteristics of pentacene P-channel obtained from experiment and simulation: (a) transfer and (b) output.

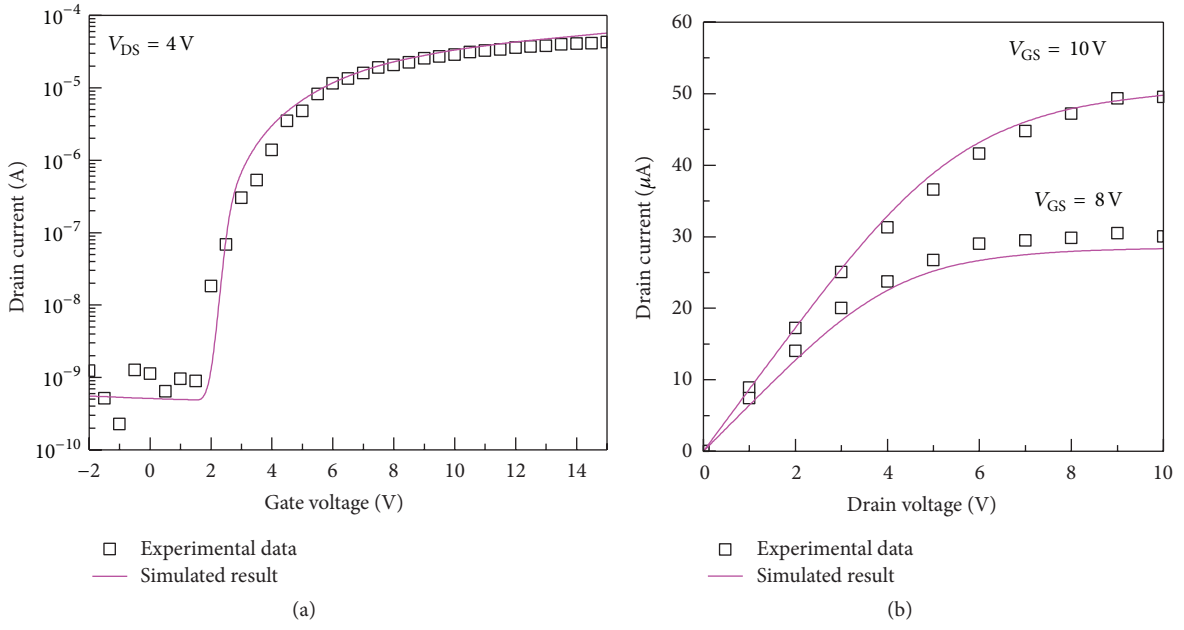

Figure 3: Characteristics of fullerene N-channel obtained from experiment and simulation: (a) transfer and (b) output.

the ratio of the output/input has a magnitude of 0.707. As can be realized in Figure 4(a), the f_c is 40.1 KHz and 10.8 KHz for the N-type and P-type, respectively.

The f_c in N-channel OTFT towers over that in P-channel one due to its higher mobility, as listed in Table 1. The f_c versus L is summarized in Figure 4(b). When the L varies from 100 μm to 10 μm the cut-off frequency f_c increases from several KHz to several MHz. In terms of frequency, the operating frequencies cover all biosignal frequency ranges in which the highest value is 10 KHz [17].

3. Organic Complementary Logic Gates

VLSI technology fundamentally is comprised of digital logic gates. To further confirm that our designed electronic circuits

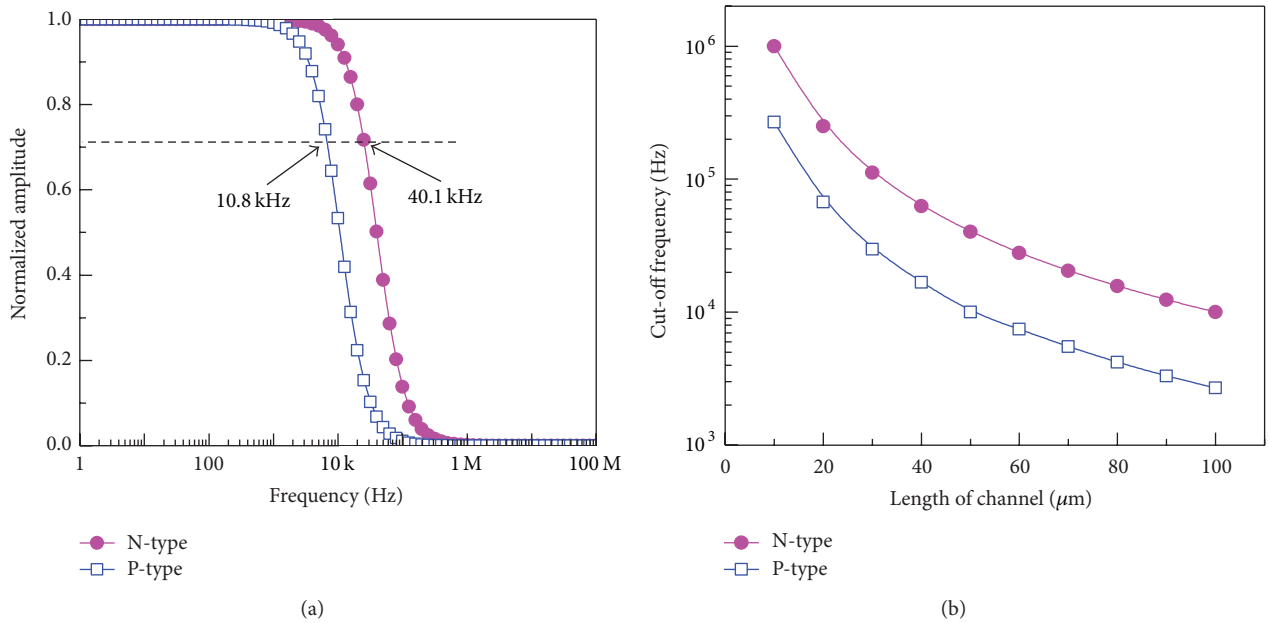

FIGURE 4: (a) Frequency response characteristics at $L = 50\ \mu$m. (b) Cut-off frequency versus length of channel.

are biocompatible, in this section, some basic organic complementary digital circuits, including a transmission gate, an inverter, a NOR, and a NAND, are created and verified with a 10 V power supply voltage and about 10 KHz input signals. The applied voltage supply of 10 V to set the OTFT elements works in deep accumulation mode. The chosen working frequency is to adapt to the highest biopotential signal frequency as above-mentioned.

3.1. Transmission Gate and Inverter. We assume that the voltage levels of 10 and 0 V correspond to a logical "1" and "0," respectively. Figure 5(a) shows the schematic and waveforms of the transmission gate, which is indeed a clocked circuit composing a P-channel and an N-channel transistor in parallel. The input signal passes through the gate when the clock is high only (in Figure 5(a)).

Figure 5(b) displays the schematic of the inverter and its waveforms. As defined, the output voltage (V_X) is invertible to the input voltage (V_A) in high or low levels. The simulation results suggest that the designed CMOS circuits operate properly.

3.2. NOR and NAND. Figure 6 presents the schematics and waveforms of the organic two-input CMOS NOR and NAND circuits. With the NOR gate in Figure 6(a), P-channel OTFTs firstly connect in parallel to form the pull-up network, and then, following the complementary design rule, the pull-down network is constructed of N-channel OTFT elements in serial connection. Similarly, in order to build the NAND gate in Figure 6(b), P-channel OTFTs are in serial, while N-channel OTFT elements are in parallel connection. The frequencies of A and B inputs are set to be 10 and 7.14 KHz, respectively. As can be realized in Figure 6, the outputs comply with the truth tables of NOR and NAND gates.

3.3. D Flip-Flop (D-FF). Flip-flop is a basic storage element in digital electronics with two stable states "1" and "0." Indeed, D-FF is most essential element in registers and digital logic blocks discussed in the next sections. Figure 7(a) presents a circuit diagram of *D* flip-flop composed by the logic gates designed in the aforementioned section. The observed waveforms in Figure 7(b) demonstrate that output *Q* equals input *D* at the rising edges of clk pulse; otherwise, *Q* does not change. It means *Q* is a "delay" of *D*, as expected.

4. 6-Bit Organic Fully Differential SAR ADC

Demand for portable compact products in modern life is increasing, so most integrated circuit designers desire to achieve energy saving goals. As for ADCs, the SAR structure is worth doing at all since its total power consumption is much lower than that in other ADC configurations, such as flash, delta-sigma, or pipelined ADCs [20].

4.1. Circuit Design. Figure 8(a) displays a conventional structure of SAR ADC, which is constructed of a minimum number of analog blocks, including a Sample/Hold (S/H), a Digital-to-Analog Converter (DAC), a comparator in connection with a SAR logic, and a register. In this work, to reduce as much as possible power consumption, we have employed simple schematics for the ADC with a limited number of transistor elements complying with complementary rules. The fully differential 6-bit SAR ADC having two analog inputs and six digital outputs was designed and simulated with the OPDK in Cadence Virtuoso environment, as simplified in Figure 8(b). The ADC consisted of two track and hold (T/H) blocks, two capacitive DACs, a comparator, a SAR logic, and an output register.

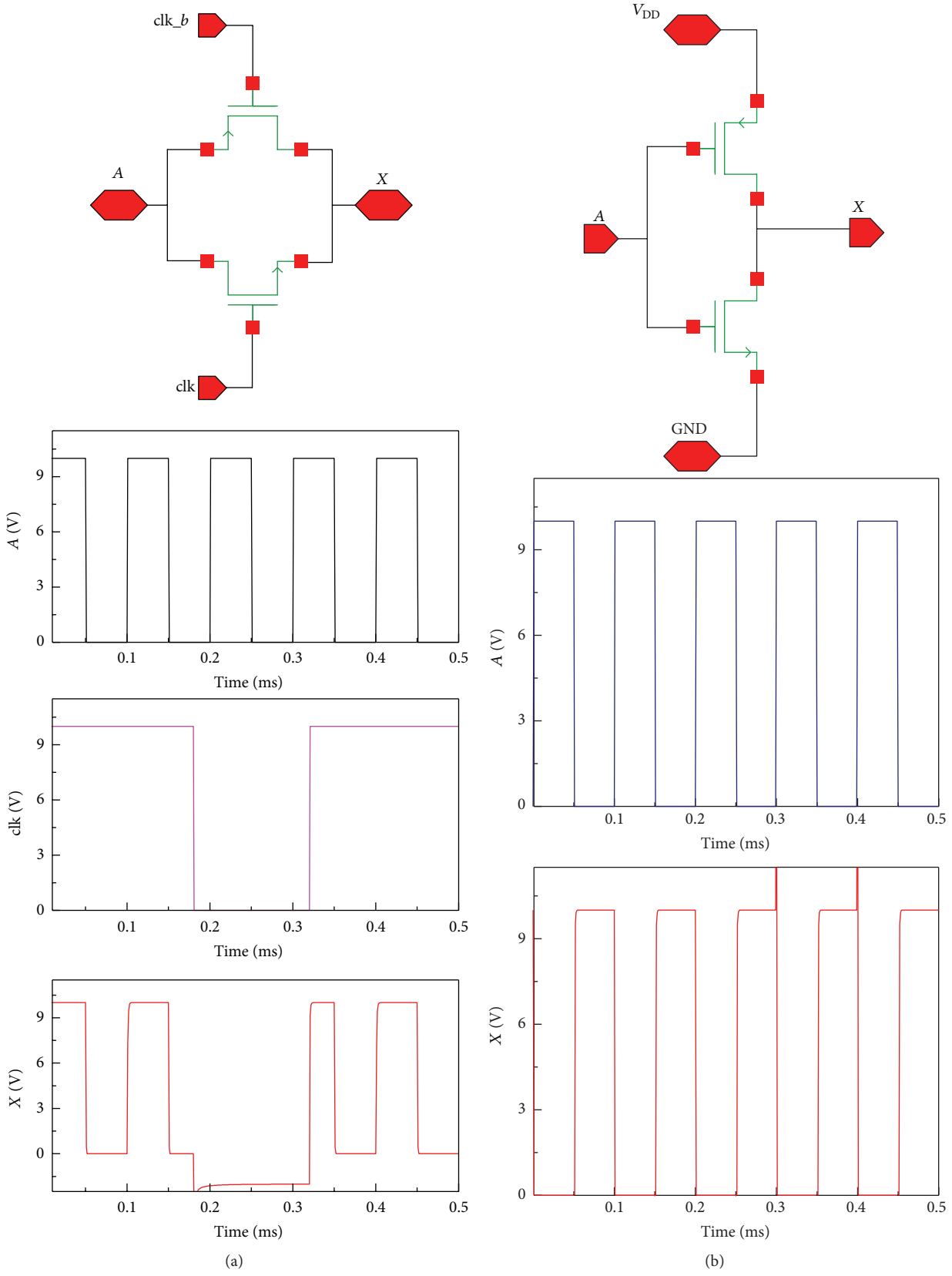

Figure 5: Schematics (top) and waveforms (bottom) of (a) transmission gate and (b) inverter.

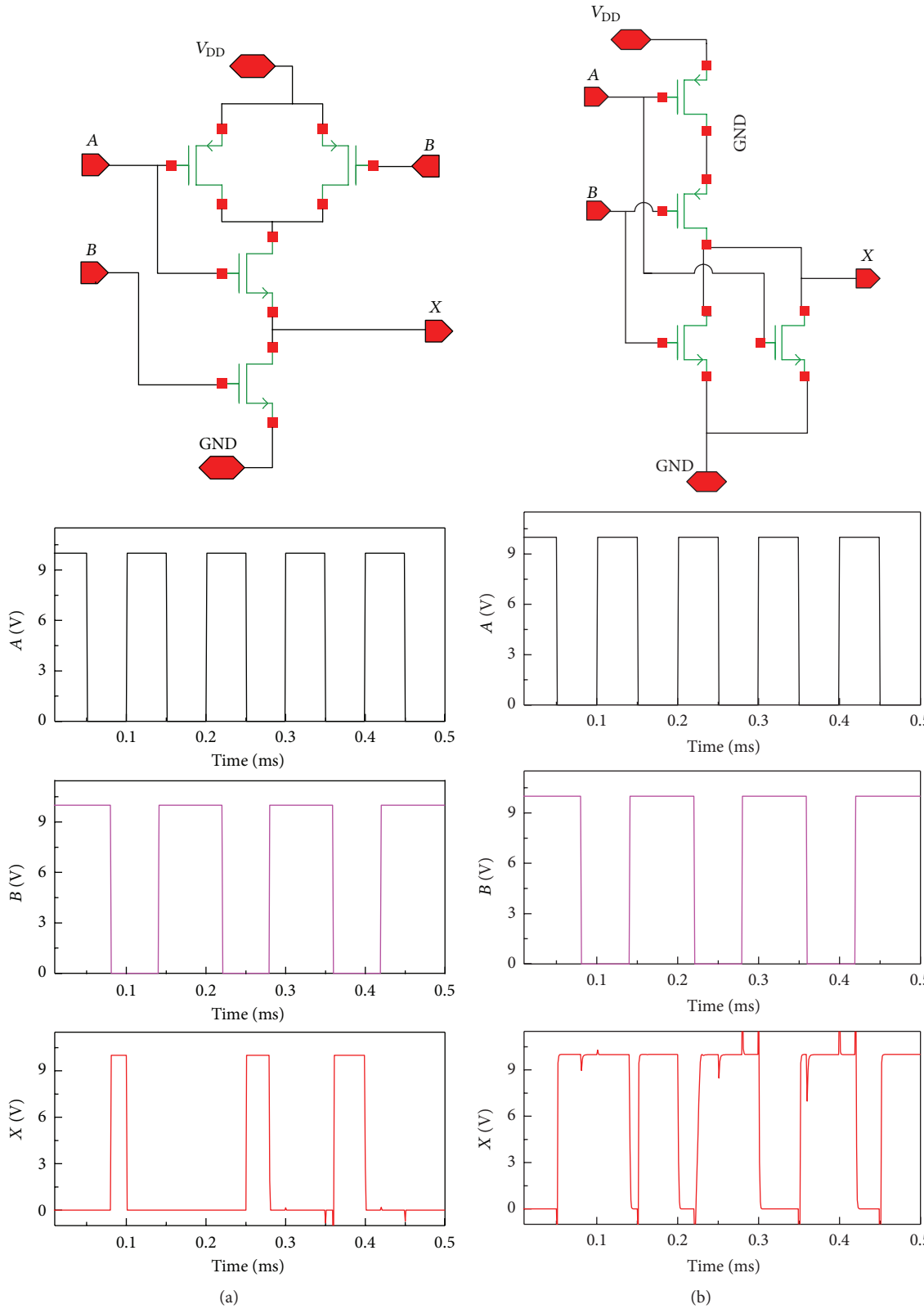

Figure 6: Schematics (top) and waveforms (bottom) of (a) NOR and (b) NAND.

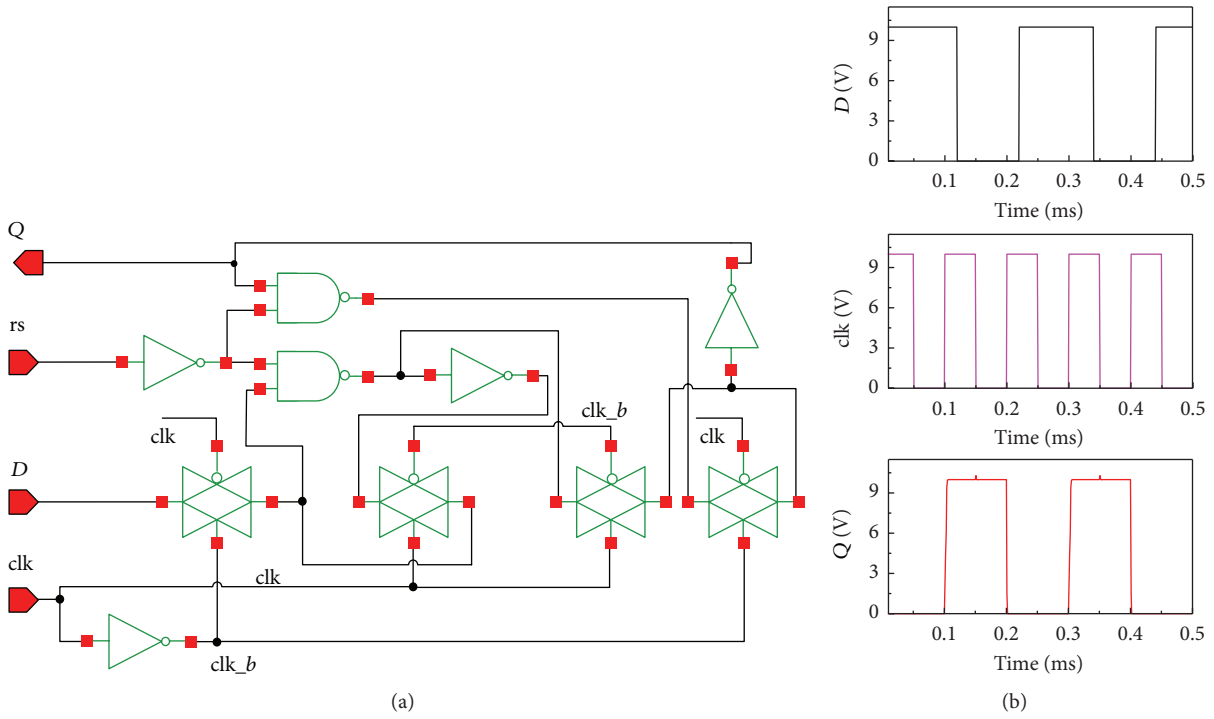

FIGURE 7: *D* flip-flop: (a) topology and (b) simulation result at a clock frequency of 10 KHz.

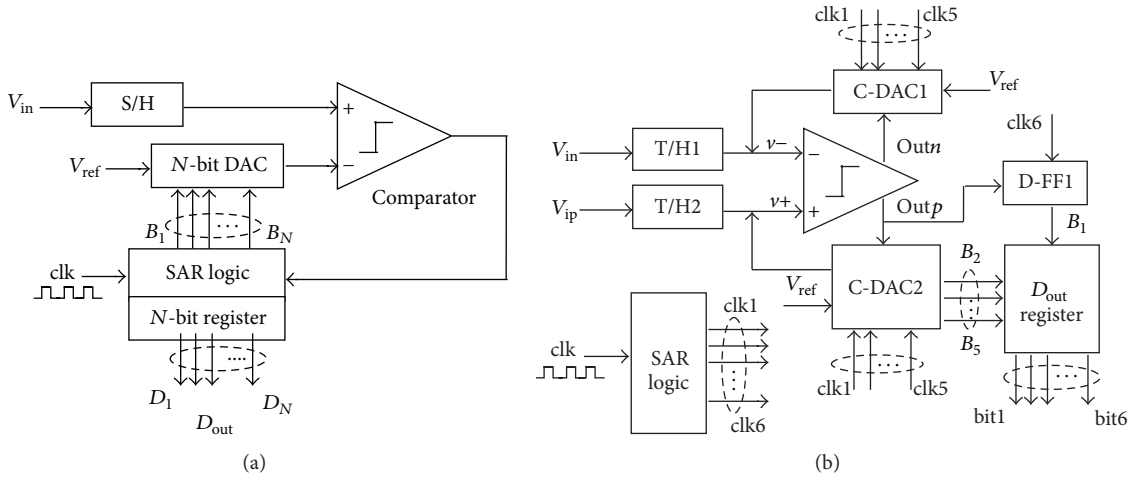

FIGURE 8: (a) Conventional structure of a SAR ADC. (b) Simplified structure of 6-bit SAR ADC.

Figure 9 describes the T/H circuit as a bootstrapped switch with the input large transistor Ms [21]. The size of Ms affects the linearity since drain-source capacitance of Ms couples to the Cs to sample the input signal. Both T/H blocks sample and hold input signals during conversion time. Their outputs connect to the inputs of the dynamic comparator.

It should be noted that the basic comparator structure is a two-stage comparator, including an amplifier and a positive feedback latch. Although that circuit is less sensitive to the effects of kickback noise and device offset, it consumes much more power. In contrast, our design aims to reduce power consumption; hence, the dynamic comparator is implemented with clock signals in order not to draw static currents. Figure 10 presents the schematic of the dynamic latch comparator with a P-type input differential pair M1-M2. When the clk signal goes to high, the outputs outp and outn

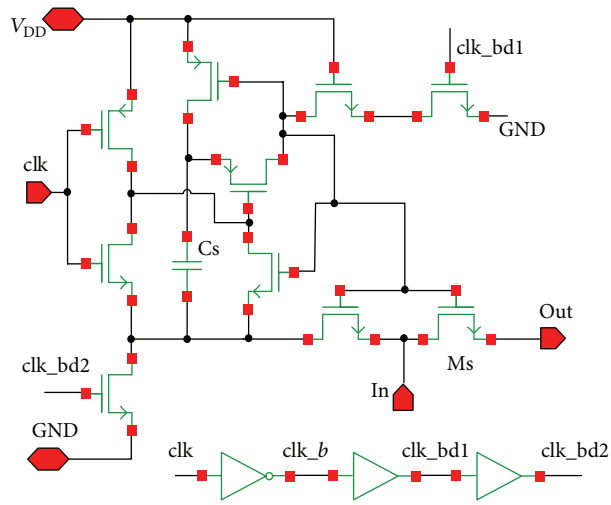

Figure 9: Schematic of track and hold block.

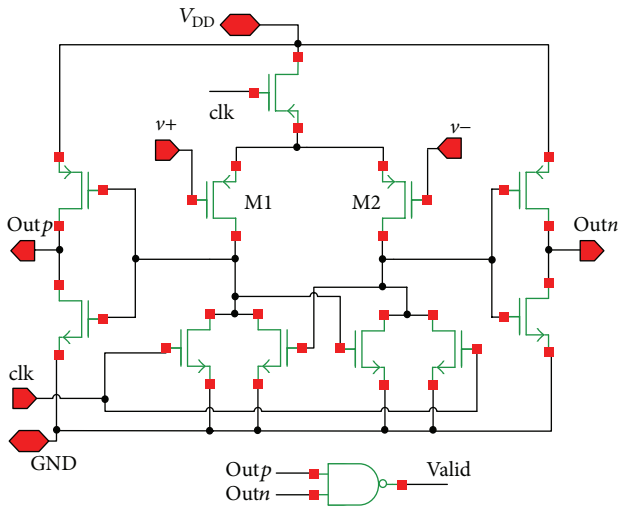

Figure 10: Schematic of dynamic latch comparator.

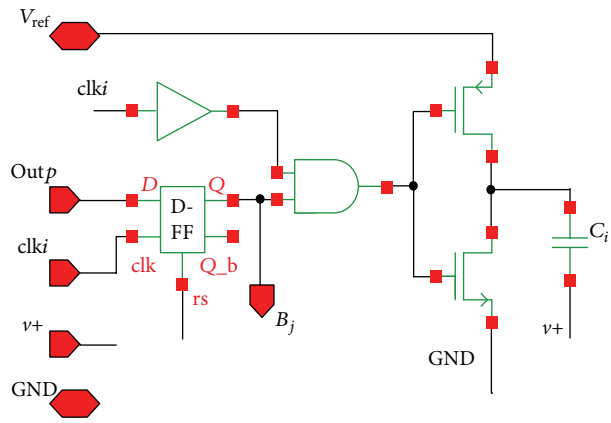

Figure 11: Typical subblock in C-DAC2.

are high, too. When the clk goes to low, the differential pair compares $v+$ and $v-$ resulting in output outp or outn being either high or low.

As for DACs, some architectures are well-known, including current-steering, C-2C, and capacitive switch types. The conventional N-bit capacitive DAC (C-DAC) uses a binary-weighted capacitor array leading to the total capacitance of 2^N unit capacitor. This structure obtains better linearity, but the large number of capacitors expands the circuit dimension rapidly and consumes lots of energy. However, the value of total capacitance of one C-DAC circuit in Figure 8(b) can be reduced a half since the most significant bit (MSB) is estimated separately [22]. The control algorithm of this ADC requires that the comparator sets the MSB to 1 if V_{ip} is higher than V_{in}; otherwise the MSB is 0. Sequentially, the N-bit ADC pushes MSB to LSB after N cycles of clock signals. That is, after several comparison cycles, one conversion step is complete; therefore, the SAR ADC exhibits limited speed. The DAC embraces 5 subblocks; a typical subblock circuit is presented in Figure 11 in which i is from 1 to 5 and j is from 6 to 2. The capacitance of unit capacitor is C_0, then C_5 equals C_0, and $C_{i-1} = 2C_i$. This induces that the total capacitance of one C-DAC circuit is $31C_0$. The C-DAC1 is designed similarly with inputs Out$n$ and $v-$.

The SAR logic comprises 6 D-FFs in serial to generate clk1 to clk6. Figure 8(b) shows that the clock signals from clk1 to clk5 are connected to C-DACs for controlling 5 capacitor arrays, while clk6 is connected to D-FF1 to push the MSB. The output register is also constructed with D-FFs to store all bits B_j from the C-DAC2 and the MSB (B_1).

4.2. Simulation Results. A power supply voltage of 10 V, a reference voltage of 5 V, a ~2 KHz clock frequency, and a 2 V, 10 Hz sine wave input signal were provided to simulate the designed SAR ADC.

Figure 12 presents a cycle of inputs and outputs of the T/H and its magnitude on time-axis. The data indicates that the circuit samples and holds the input signals during the conversion duty.

Simulation results in Figure 13 also attest the main power consumption at rising and falling edges of clock pulses of the dynamic comparator. Consequently, its average dissipated energy reduces significantly to about 112 μW. The simulation process also points out that the higher input voltage makes the power decrease. This is because of a reduction in the drain current resulting from the lower gate-source voltages of M1 and M2 (in Figure 10).

The timing diagram of the SAR logic is given in Figure 14. Each clk$i$ goes to high sequentially at the rising edges of the valid signal, which is created based on the comparator outputs, as seen in Figure 10. All of the clock pulses go to low at the rising edge of the primary clk signal to end one conversion step.

Dynamic performance of an ADC needs to use Fast Fourier Transform (FFT) test method to measure effective

Table 2: Performance summary of current organic ADCs.

Specification	[12][a]	[14][b]	[18][b]	[19][b]	This work[c]
Organic semiconductor material	Pentacene (only P-type)	Pentacene (only P-type)	DNTT F16CuPc SAM	PEN foil SAM	Pentacene and fullerene
Structure	Delta-sigma	VCO-based	SAR C-2C	SAR R-2R	C-SAR
Supply power [V]	15	20	3	40	10
Resolution [bit]	5	10	6	4	6
ENOB [bit]	4.69[†]	6	N/A	2.96	5.05
SNR [dB]	30[†]	48	N/A	19.6	32.17
Sampling frequency [Hz]	500	<40	100	4.17	2000
Power consumption [μW]	1500[‡]	480	3.6[*]	540	883.7

[*]Excluding circuits on FPGA.
[a]Simulated and measured results. [†]Simulation data with Spice level 1. [‡]Measured data.
[b]Measured results.
[c]Simulation results with Spice level 61.

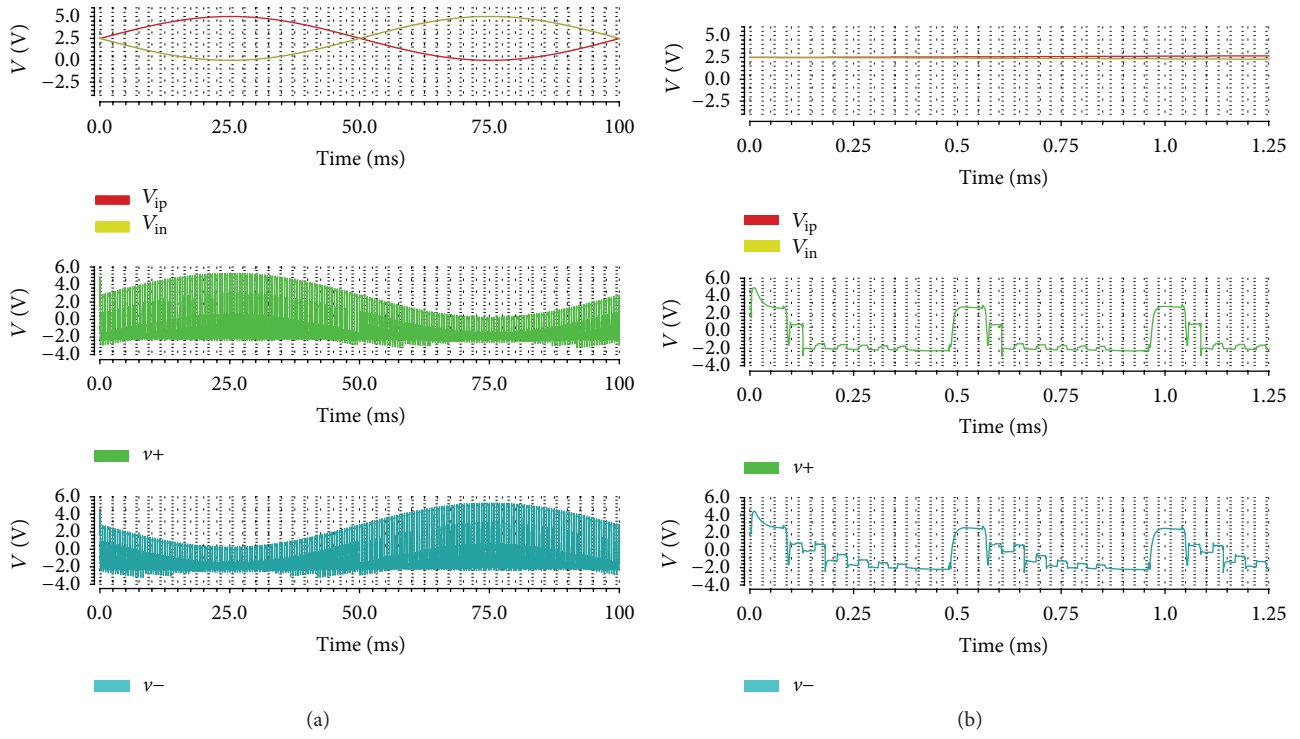

Figure 12: Cycle of T/H block outputs: (a) full and (b) partly magnified in time.

number of bits (ENOB) and signal-to-noise plus distortion ratio (SNDR). The input signal is sine wave; the output signals are the digital codes; then these codes are converted to analog formation by an ideal DAC. Figure 15 shows the output spectrum of the ADC, which extracts an ENOB of 5.05 bits, a SNDR of 32.17 dB at an average power consumption of 883.7 μW.

Table 2 presents the results obtained in this work in comparison to those from others. In terms of frequency, our circuit achieves the clock speed of 2 KHz, which is the highest value ever reported in organic ADC [12, 14, 18, 19]. Furthermore, other parameters, such as supply voltage, ENOB, sampling rate, and power dissipation, are very comparable to those from the others.

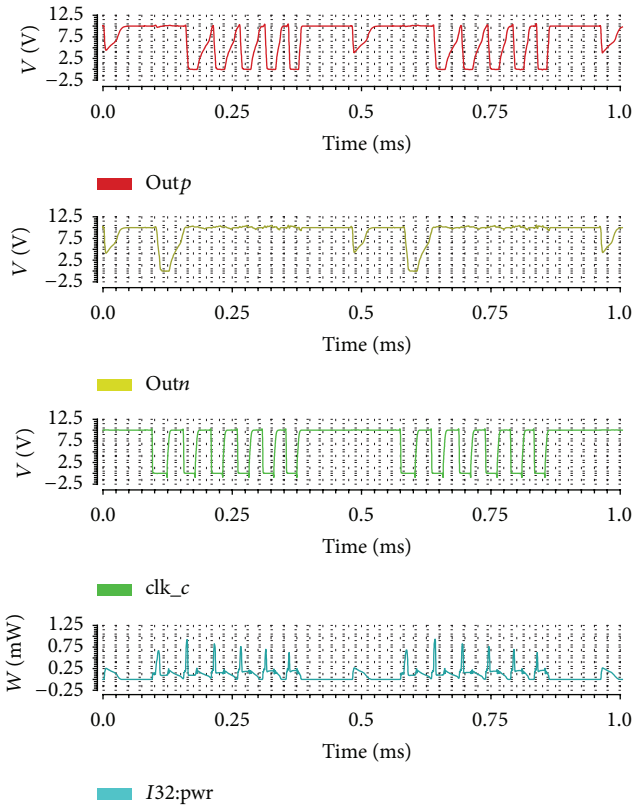

FIGURE 13: Waveforms of outputs (Out$p$, Out$n$), control clock signal (clk_c), and power consumption of dynamic comparator (I32:pwr).

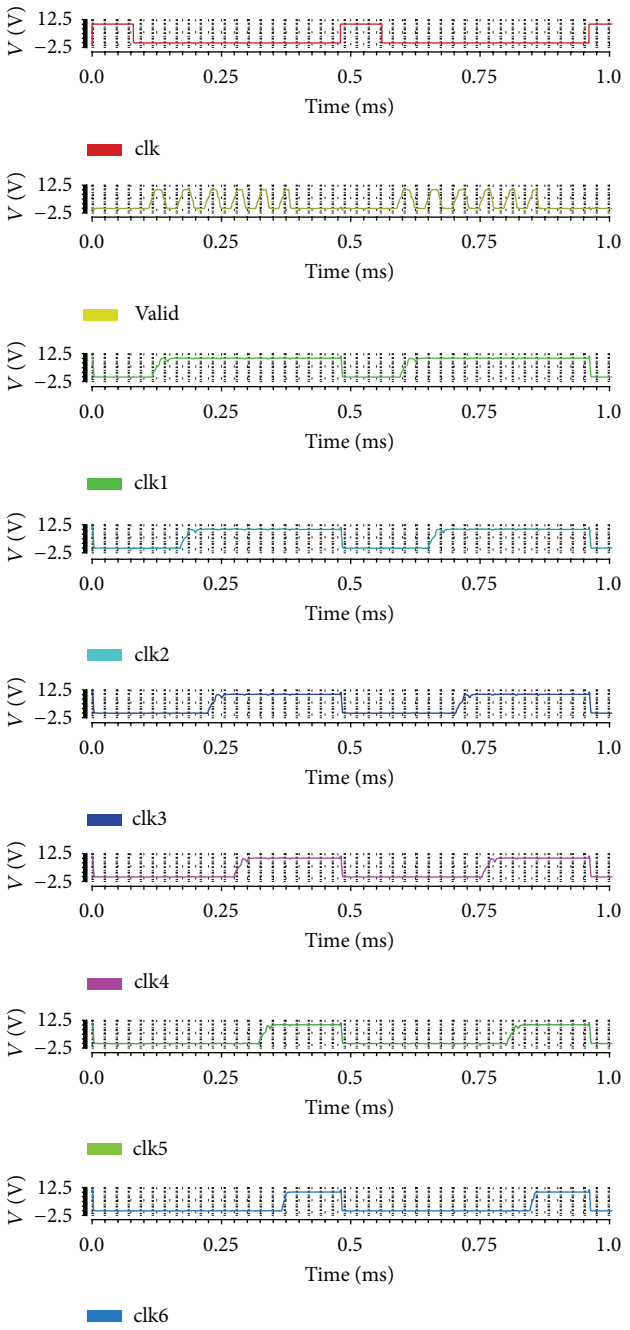

FIGURE 14: Timing diagram made from SAR logic outputs.

Up to now, there are four reported works on ADCs, which are compared to our work as seen in Table 2. Reference [12], for example, archives highest sampling frequency of 500 Hz; [18] reduces power supply voltage to the smallest value of 3 V compared to tens of volt in others. The highest resolution is 6 bits in [14, 18], and this work, and the best linearity in [19] is expressed with DNL and INL is 0.24 and 0.42 LSB, respectively. To obtain those encouragements the circuits have to suffer from some disadvantages. For instance, the ADC in [12] consumes up to 1.5 mW, and [18] gets DNL and INL is 2.6 and 3 LSB before digital calibration on FPGA, respectively. Reference [14] contains a voltage controlled oscillator (VCO) generating the maximum frequency below 40 Hz and uses a large number of transistors due to using only P-type technology, and sampling frequency in [19] is only 4.17 Hz at 40 V power supply voltage. It is noted that the above limitations would prevent the ADCs from any application apart from [14], which could be proposed for smart chemical or temperature sensors. In terms of frequency, our circuit gets the highest clock speed of 2 KHz, which is four times higher than that of the second one. Furthermore, our ENOB is good enough while the power consumption is medium.

5. Conclusions

We have utilized pentacene P-channel and fullerene N-channel TFTs to design and simulate organic integrated circuits thanks to creating their valid models with the OPDK added in Cadence. The organic circuits, including logic gates, flip-flops, comparators, and analog-to-digital converters (ADCs), work properly in biopotential frequency ranges. The SAR ADC achieves 5.05-bit ENOB, 32.17 dB SNR with a power consumption of 883.7 μW at 10 V supply voltage, and 2 KHz clock pulses. With above-mentioned results, we strongly believe that the models can help to save the time and cost in organic IC design and manufacturing.

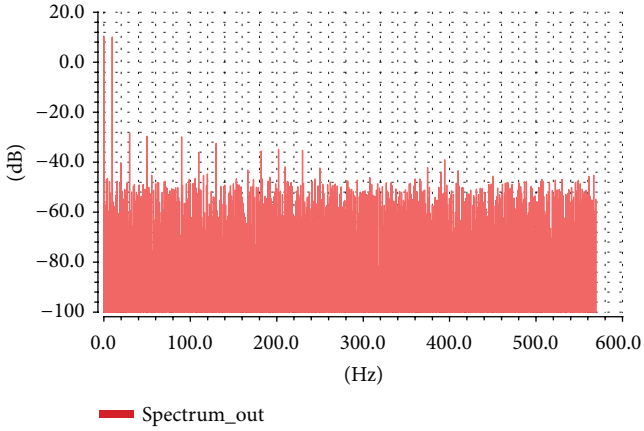

Figure 15: Output spectrum.

Competing Interests

The authors have no conflict of interests associated with this paper.

Acknowledgments

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