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Research Article

Energy-Aware Low-Power CMOS LNA with Process-Variations Management

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A reconfigurable low-noise amplifier (LNA) with digitally controllable gain and power consumption is presented. This architecture allows increasing power consumption only when required, that is, to improve LNA's radiofrequency performance at extreme communication-channel conditions and/or to counteract the effect of process, voltage, and temperature variations. The proposed design leads to significant power saving when a relaxed operation is acceptable. The LNA is implemented in a 130 nm 1.2 V CMOS technology for a 2.4 GHz IEEE-802.15.4 application. Simulated LNA performance (taking into account the worst cases under process variations) is comparable to recently published works.

1. Introduction

A system with multiple operation modes, able to adapt its performance dynamically depending on working conditions, can be implemented using reconfigurable circuits. Modes with relaxed requirements can be designed to operate at lower biasing current and/or voltage, leading to an overall decrease in power consumption compared to conventional fixed circuits. This power-saving approach has been applied in the following two scenarios: (1) to mitigate the effects of process variations (improving yield and reliability) [1–3] and (2) to implement wireless-receiver blocks which adjust their power consumption depending on communication-channel conditions (energy-aware receivers) [4–7]. Combining both features in an integrated receiver circuit shows up as a very attractive design goal, due to the growing demand and mass production of low-power wireless devices. However, such a solution has not been already reported.

In the receiver context, especially in fully integrated implementation scenarios, the low-noise amplifier (LNA) is a key block that determines the overall system performance [8]. It has to offer, simultaneously, good input matching, low-noise contribution, high linearity, and high reverse isolation, constrained by power consumption. In addition, its gain is crucial and represents a trade-off between receiver's noise and linearity performances [8, 9]. In this sense, adjusting RF parameters of the LNA, especially gain, by controlling the biasing of amplifying-stage transistors, has been used to allow power-consumption saving under relaxed communication-channel conditions [6, 7, 10].

On the other hand, adaptability has been also used to mitigate the effects of process variations on CMOS-LNAs [3, 11–15]. The proposal presented by González et al. [3] shows the potentials of an adaptable LNA to save power when its behavior under process variations remains close to the typical-case performance. However, the reported solutions focus on calibrating fixed-gain LNAs; thus, they do not exploit the advantages of variable-gain schemes.

This work presents a reconfigurable LNA capable of adjusting its power consumption taking into account

communication-channel conditions and the effects of process, supply-voltage, and temperature variations. This energy-aware LNA uses architecture with digitally controllable gain and power consumption. The proposed power-saving strategy is corroborated by implementing a 130 nm 1.2 V CMOS LNA for a 2.4 GHz IEEE-802.15.4 application. LNA behavior under process variations is analyzed via Monte Carlo simulations, the results of which are used to evaluate the corresponding receiver performance.

This paper is organized as follows. Section 2 summarizes the main equations that support the ideas followed in this work, from a system-level point of view. Section 3 describes the reconfigurable architecture and the proposed power-saving strategy as a function of communication-channel conditions and the effects of process variations. Section 4 presents the main implementation details and discusses simulation results, including the comparison with other LNAs for IEEE-802.15.4 receivers. Finally, conclusions are given in Section 5.

2. A System-Level Overview

The working principle of an energy-aware receiver relies on the fact that noise figure (NF) and linearity requirements depend on the received input-signal level. This can be understood by examining the following expressions [16]:

$$\mathrm{NF} \leq P - 10\log(kTB) - \mathrm{SNR}_{\mathrm{min}}, \tag{1}$$

$$\mathrm{IIP}_3 \geq \frac{3P_{\mathrm{interf}} - P + \mathrm{SNR}_{\mathrm{min}}}{2}, \tag{2}$$

$$\mathrm{IIP}_3 \geq P + 10\,\mathrm{dB}. \tag{3}$$

In the above equations, NF is the noise figure, P is the input-signal power, k is the Boltzmann constant, T is the absolute temperature, B is the channel bandwidth, $\mathrm{SNR}_{\mathrm{min}}$ is the minimum signal-to-noise ratio required by the application (including some design margin which accounts for losses that are not certainly determined at system-level design time), IIP_3 is the input-referred third-order intermodulation intercept point, and P_{interf} is the power of interferer signals. All the magnitude values are expressed in logarithmic units (dB or dBm), with the exception of kTB product. Equation (3) derives from the general assumption that considers the 1 dB compression point ($\mathrm{CP}_{1\,\mathrm{dB}}$) as the upper limit of input power [17] and from the approximate relationship $\mathrm{CP}_{1\,\mathrm{dB}} = \mathrm{IIP}_3 - 10\,\mathrm{dB}$ [8], in order to use IIP_3 as the only linearity measurement.

It can be seen from (1) that NF can be relaxed as input-signal power increases. On the other hand, IIP_3 has two critical values: one required to detect a weak desired signal in the presence of interferers (see (2)) and the other required to drive the maximum signal level (see (3)). However, linearity requirement of the receiver can be lessened at intermediate signal levels. This can be exploited for saving energy by implementing a reconfigurable circuit with multiple operation modes (i.e., with different values of NF and IIP_3), taking into account the fact that more relaxed NF and IIP_3 can be achieved with lower power consumption [19]. The aforementioned approach contrasts with the use of traditional circuits, which must be designed to work at worst-case conditions, thus requiring higher and fixed power consumption.

2.1. LNA in the Receiver Context. Receiver parameters (F_{Rx}, $\mathrm{IIP}_{3\mathrm{Rx}}$) can be related to those of the LNA (G_{LNA}, F_{LNA}, and $\mathrm{IIP}_{3\mathrm{LNA}}$) and the other building blocks (F_{fs}, $\mathrm{IIP}_{3\mathrm{fs}}$, where subscript "fs" stands for "following stages," i.e., from mixer input to A/D output) using cascaded-stages equations (4) [8]. Hence,

$$F_{\mathrm{Rx}} = F_{\mathrm{LNA}} + \frac{F_{\mathrm{fs}} - 1}{G_{\mathrm{LNA}}},$$
$$\frac{1}{\mathrm{IIP}_{3\mathrm{Rx}}} = \frac{1}{\mathrm{IIP}_{3\mathrm{LNA}}} + \frac{G_{\mathrm{LNA}}}{\mathrm{IIP}_{3\mathrm{fs}}}. \tag{4}$$

In the above equations, F is the noise factor, such as $\mathrm{NF} = 10\log F$, while gain and IIP_3 are expressed in "times" (W/W) and W (or mW), respectively.

Controlling LNA parameters, particularly gain, allows adjusting the noise figure and linearity of the receiver. The LNA should provide high gain and low-noise figure to guarantee the required noise figure of the receiver for detecting the minimum input-signal level. However, LNA gain can be reduced as the NF of the receiver can be relaxed, when receiving higher input-signal levels. LNA gain reduction also allows lowering the linearity of the LNA and the subsequent stages, without affecting the receiver linearity required to drive large input-signal power. Therefore, it is convenient to design adaptable LNAs, with the capability of switching between high and low gain modes [20, 21].

When needed, gain can be lowered by reducing the transconductance of amplifying-stage transistors, which in fact allows for power-consumption saving [6, 7, 10]. However, changing the DC operation point affects other RF parameters, thus limiting the gain variation rate. Therefore, the inclusion of extra DC-invariant gain-controlling methods could be useful, for example, to compensate for linearity degradation, as it is shown here.

3. The Proposed Energy-Aware LNA

Based on the widely used inductively degenerated common-source topology, Figure 1 shows the proposed reconfigurable LNA implementing the above ideas. This is an improved proposal with respect to that presented at [3], where only worst-case process variations were dealt with.

Gain and power consumption are digitally controlled through inputs $\Phi_{1,2}$ and $\Phi_{1,2}^{g}$. Controllability is introduced by connecting two extra branches in parallel with the traditional cascode configuration (M_1 and M_2). Each branch comprises a transconductance stage (M_3 and M_5) and a cascode pair acting as a current switch (M_{41}/M_{61}, connected to signal output, and M_{42}/M_{62}, connected to V_{DD} as a signal-dumping path). Identical branches are considered for simplicity. This circuit combines two different control techniques: (1) gain and power control through transistor width scalability [7] and (2) current-splitting gain-control technique [22, 23].

Table 1: Summary of operation modes features.

$\Phi_1\Phi_2/\Phi_1^g\Phi_2^g$	11/00	10/00 01/00	00/00	00/01 00/10	00/11
Mode	HG-FP	MG-MP	LG-LP	LG-MP	LG-FP
Gain	Highest	↓	↓↓	↓↓↓	Lowest
Power consumption	Highest	Medium	Lowest	Medium	Highest
Input resistance	Highest	Medium	Lowest	Medium	Highest

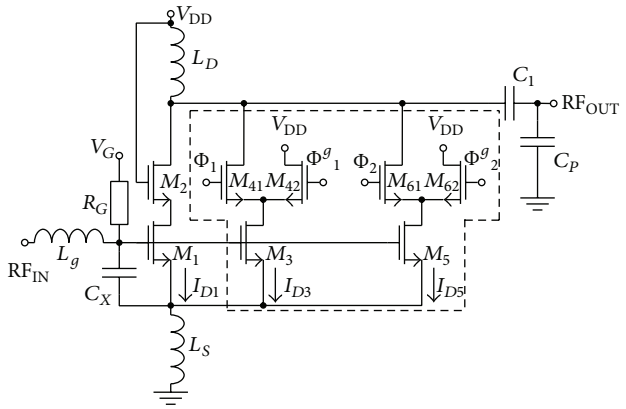

Figure 1: Reconfigurable LNA.

Other characteristics associated with the base topology can be summarized as follows. Degeneration inductance (L_s) provides the real part of input impedance without adding an extra noise source [24]. Gate-source connected capacitor (C_X) allows reducing noise figure without increasing power consumption in gain constrained applications [25, 26]. Gate inductor (L_g) tunes the necessary input impedance and drain inductor (L_D) provides parallel resonance with the total capacitance at output. Capacitive divider (C_1, C_P) is used to match output impedance with 50 Ω termination for stand-alone prototype testing.

3.1. Operation Modes Description. The operation modes that arise from the scheme of Figure 1 can be described as follows.

The highest gain of the LNA is set by connecting both switchable branches to the output network ($\Phi_1\Phi_2 = 11/\Phi_1^g\Phi_2^g = 00$). However, this HG-FP (standing for "high gain, full power") mode also presents the highest power consumption. If one of the extra branches is turned off (setting $\Phi_1\Phi_2$ to 10 or 01, with $\Phi_1^g\Phi_2^g = 00$), a midgain and midpower mode (MG-MP) is obtained, while turning off both switchable branches ($\Phi_1\Phi_2 = 00/\Phi_1^g\Phi_2^g = 00$) leads to a low gain mode with the lowest power consumption (LG-LP mode).

The drawback of the above-described operation (width scalability) is that it affects the input-impedance matching. The reason is that the input resistance is lower as less current flows through the degeneration inductor (as switchable branches are disconnected). Thus, the allowable impedance matching degradation limits the total gain variation and power-saving ratio.

When needed, modes with lower gain can be achieved, but at the expense of consuming the middle or the highest power values. Low gain/midpower (LG-MP) and low gain/full power (LG-FP) modes are set by turning on one or both switchable branches via the dumping cascode transistors ($\Phi_1\Phi_2 = 00$ with $\Phi_1^g\Phi_2^g = 10$ or 01, for LG-MP mode, and $\Phi_1\Phi_2 = 00/\Phi_1^g\Phi_2^g = 11$, for LG-FP mode). Although in the three low gain modes (LG-LP, LG-MP, and LG-FP) only the fixed branch (M_1 and M_2) is connected to the output, different gain values are obtained because of the variations of the input-stage operation point. When a switchable branch is turned on but the signal flowing through it is dumped to ground (via V_{DD} path), it does not contribute to the output signal; however, it does increase the input resistance, causing a reduction of the amplifier transconductance.

In summary, Table 1 shows the controlling codes and the expected performance of the different operations modes.

3.2. Adjusting Strategy. Next, the proposed usage of the different operation modes, or adjusting strategy, is presented.

HG-FP mode should provide gain over a certain value, G_{min}, in the worst case due to process variations, with G_{min} being the minimum gain value needed to achieve the required sensitivity (i.e., NF_{Rxmax}). On the other hand, the midgain typical value can be set slightly over G_{min} by properly sizing M_1, M_3, and M_5. This way, those receivers less affected by process variations can use MG-MP mode instead of HG-FP mode to receive minimum input-signal level, thus saving power consumption in such cases without degrading production yield.

LG-LP mode can be used for saving power when input-signal level allows relaxing receiver NF. Depending on the linearity of both, the LNA and the subsequent stages, this low gain mode could also satisfy the system requirement for the maximum input-signal level. However, lower gain modes (LG-MP or LG-FP) could be useful to compensate possible linearity degradation in the LNA due to process variations, increasing power consumption but only when being required.

4. Implementation and Results

In order to corroborate the proposed ideas, a LNA was designed and simulated using a 130 nm CMOS technology for a 2.4 GHz IEEE-802.15.4 application. Channel length was set to the minimum value (120 nm) for each transistor. Cascode-transistor width was set to half of the corresponding transconductance-stage transistor. Taking a value of 10 dB for G_{min} [27], gain of 12 dB is required for the HG-FP mode

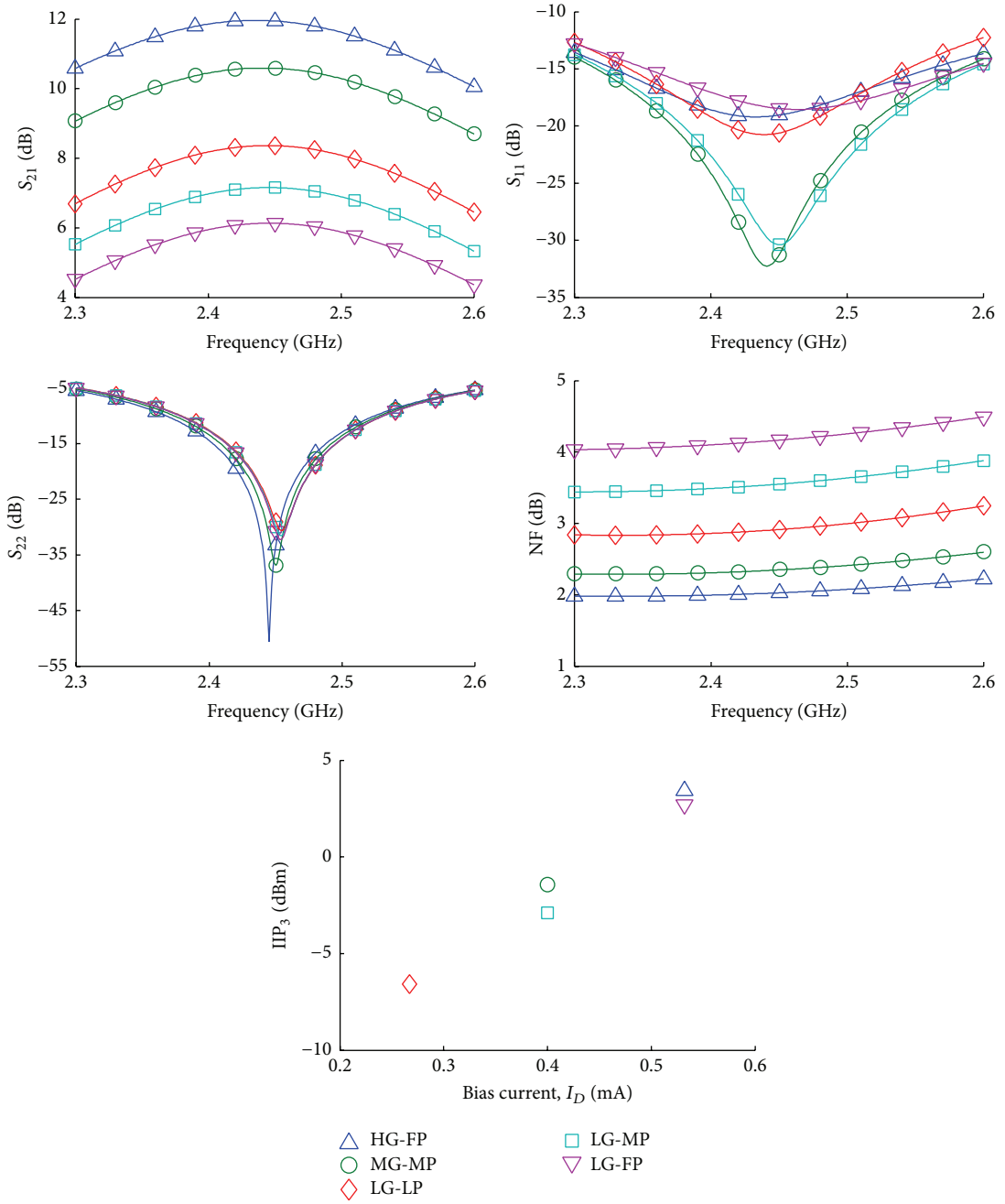

Figure 2: Typical-case simulation results.

in the typical case (obtained by corner simulations). MG-MP gain was set close to 10.5 dB. Transistor widths ratio $W_1 : W_3 : W_5 = 2:1:1$ was found to offer a suitable gain variation having proper input-impedance matching in every mode ($S_{11} < -10$ dB). Transistor widths and current values were chosen from the results of simulation-based design space exploration carried out with the conventional topology (i.e., without switchable branches), minimizing power consumption while trading off LNA's NF and IIP_3. Passive components were determined to match impedance values at MG-MP mode, in order to tolerate both the increase and the decrease of input resistance when switching among modes with different biasing currents. Table 2 shows the selected components sizes and biasing. The full power consumption (all branches turned on) is 0.64 mW from a 1.2 V supply, with 25% and 50% power saving when using mid- and lowest power modes, respectively. A current mirror was included to provide gate-biasing voltage, V_G.

Figure 2 shows typical-case simulation results at 27°C. Pairs of modes with the same power consumption (HG-FP/LG-FP and MG-MP/LG-MP) show similar input matching (S_{11}) and IIP_3, as expected taking into account the fact

Table 2: LNA component values.

I_{D1}/W_1 (μA/μm)	$I_{D3,5}/W_{3,5}$ (μA/μm)	L_S (nH)	L_g (nH)	C_X (fF)	C_1 (fF)	C_P (pF)	L_D (nH)
267/28	133/14	2.4	11.2	246	426	1.59	10.5

that corresponding DC operating points remain fixed. On the other hand, output matching (S_{22}) is not practically affected when switching between modes. The higher the biasing current, the higher the IIP_3 and the larger the gain variation obtained by current splitting. This higher-IIP_3/lower gain combination reinforces using LG-MP or LG-FP if the receiver requires better linearity.

4.1. LNA under Process Variations. LNA behavior under process variations was analyzed via 1000-run Monte Carlo simulations, using the statistical distribution provided by the foundry. Receiver performance was evaluated analytically, using LNA simulation results and (4). The overall NF and IIP_3 specifications of the stages following the LNA (NF_{fs}, IIP_{3fs}) were set to meet receiver requirements, at every Monte Carlo run, with at least one high gain/low gain modes combination. Receiver specifications were taken to comply with IEEE-802.15.4 standard [28], using the requirements at extreme communication-channel conditions proposed by [29]: {NF = 15.5 dB; IIP_3 = −32 dBm}, for detecting minimum input-signal level (−85 dBm, although, for IIP_3 calculation, minimum input-signal power is taken as 3 dB over receiver's sensitivity [28], i.e., −82 dBm [16]) with maximum interference (−52 dBm) and SNR_{min} = 10.5 dB (derived from the values given by [29]); and IIP_3 = −10 dBm, for receiving the maximum input power (−20 dBm). The most relaxed NF_{fs} and IIP_{3fs} were selected (25.3 dB and 4.2 dBm, resp.), achieved when using the HG-FP/LG-FP modes combination.

Figure 3 shows the values of NF and IIP_3 of the receiver, corresponding to every run of Monte Carlo simulations (dots) and to the typical case (color-filled diamond). Dashed lines mark out receiver specifications according to the function of each operation mode (NF specification for high gain and midgain modes, IIP_3 specification for low gain modes).

IIP_3 is always higher than the minimum value required for receiving weak signals in the presence of interferers (−32 dBm); thus, noise figure determines receiver sensitivity in all cases. In addition, in each case, the maximum input-signal power that can be handled by the high gain and midgain modes is always higher than the sensitivity of the low gain modes. This guarantees that any input-signal level is covered by at least one operation mode.

According to the minimum power consumption that needs to be used to meet receiver requirements at extreme communication-channel conditions, five possible scenarios were obtained. For each scenario, the behavior of a specific run has been highlighted in Figure 3. Circuits with lower or no degradation in their RF performance (e.g., run A), with respect to the typical case, can use the lowest power-consumption combination (MG-MP/LG-LP, consuming 0.48 and 0.32 mW, resp.) for receiving the minimum and maximum input-signal levels required by the standard ($NF_{RxMG\text{-}MP}$ < 15.5 dB and $IIP_{3RxLG\text{-}LP}$ > −10 dBm).

When the noise figure of the receiver using MG-MP mode does not ensure the receiver sensitivity ($NF_{RxMG\text{-}MP}$ > 15.5 dB), thus HG-FP mode (increasing power consumption to 0.64 mW) has to be used instead (e.g., runs B, D, E, and F). In such cases, HG-FP mode should be combined with one of the low gain modes depending on linearity performance: having acceptable linearity ($IIP_{3RxLG\text{-}LP}$ > −10 dBm) allows using LG-LP mode (e.g., run B); midlevel linearity degradation ($IIP_{3RxLG\text{-}LP}$ < −10 dBm but $IIP_{3RxLG\text{-}MP}$ > −10 dBm) requires using LG-MP mode (consuming 0.48 mW, e.g., run D), while runs with more degraded linearity ($IIP_{3RxLG\text{-}MP}$ < −10 dBm) demand the mode with the lowest gain and highest IIP_3, LG-FP mode (0.64 mW, e.g., runs E and F). Particularly, runs E and F correspond with the worst cases of receiver's noise figure and linearity, respectively.

On the other hand, if receiver noise figure is acceptable but linearity degrades, MG-MP/LG-MP combination is used (e.g., run C). The last possible scenario, cases with an acceptable receiver NF and highly degraded IIP_3, does not present any occurrence; thus, MG-MP/LG-FP combination is not required.

Table 3 summarizes the above information, including the occurrence probability of each scenario. In most of the runs, the lowest power-consumption combination (MG-MP/LG-LP) can be used, while the most power-consuming combination (HG-FP/LG-FP) is required only in 1% of the cases.

Additionally, with independence of operation modes required to handle extreme communication-channel conditions, the lowest DC power can be consumed (i.e., using the LG-LP mode) during circuit operation as input-signal level moves away from its minimum and maximum values and more relaxed behavior of receiver's noise and linearity can be tolerated (according to (1)–(3)). This can be observed in Figure 4, where the minimum required power consumption of the LNA has been plotted as a function of input-signal level. Five different plots have been included, corresponding to each process-variations scenario. It is noticeable that the LG-LP mode can handle most of the input-signal power range. This should increase the probabilities of saving energy at operation time.

4.2. Supply and Temperature Variations. The capabilities of the proposed circuit to counteract the effects of supply-voltage and temperature variations, as other important causes of performance degradation in microelectronics circuits, were also analyzed. Simulations sweeping V_{DD} value, at 27°C, and temperature, with V_{DD} = 1.2 V, were carried out using the typical-case circuit with respect to process variations.

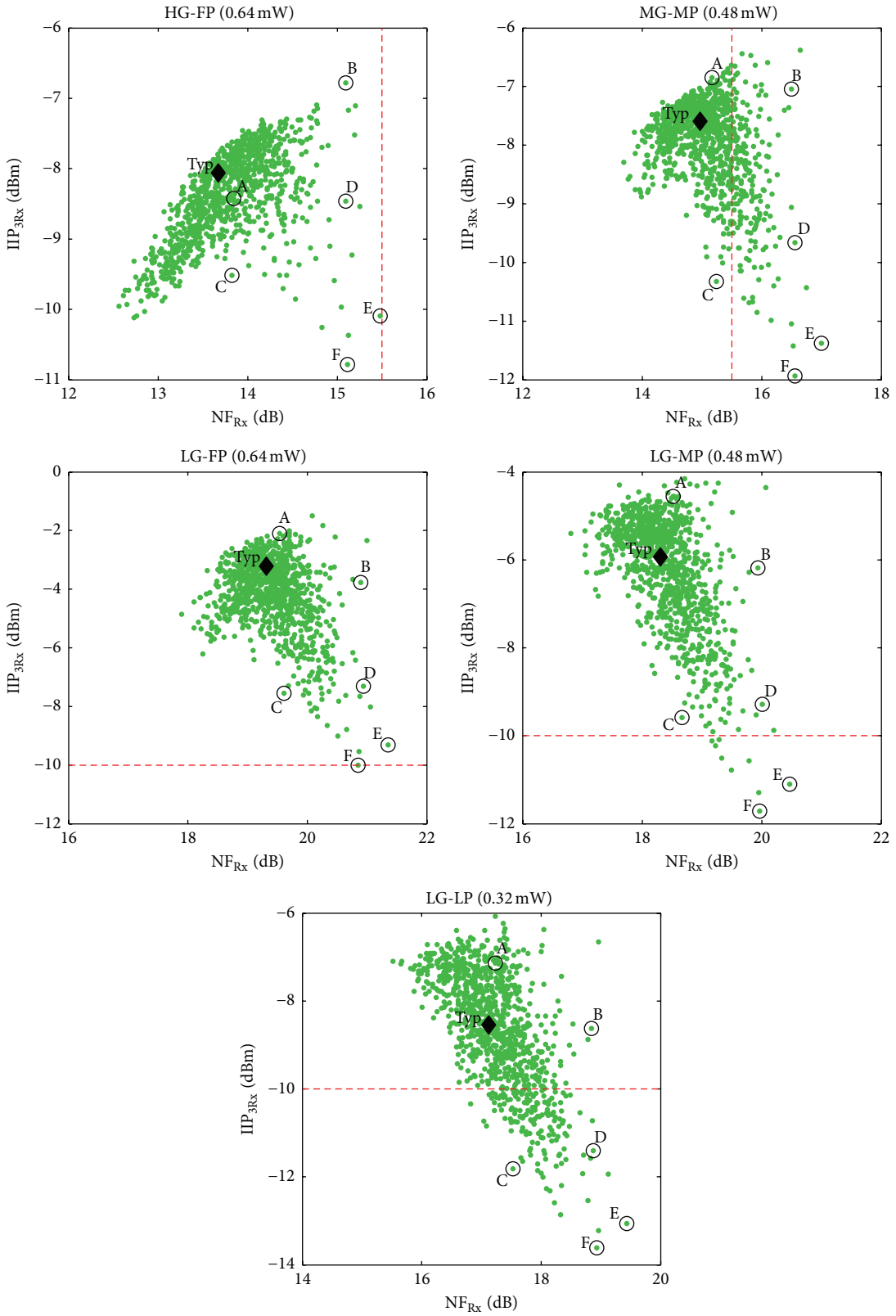

Figure 3: NF and IIP_3 of the receiver calculated from Monte Carlo simulation results of the designed LNA.

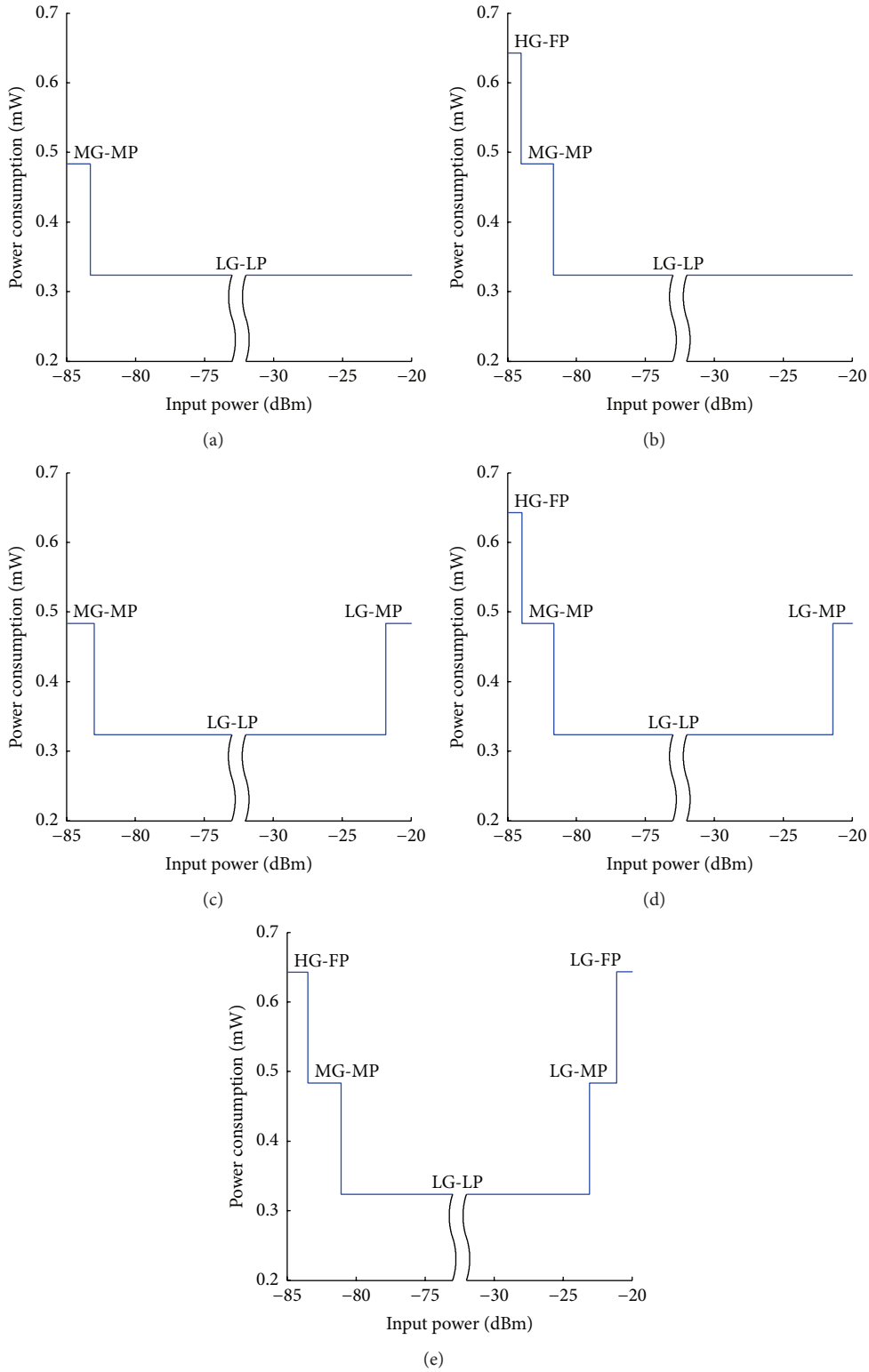

Figure 4: LNA power-consumption profile as a function of input-signal power, for different process-variations scenarios.

Table 3: Modes utilization at extreme communication-channel conditions, depending on the effects of process variations.

LNA performance	Receiver performance	Minimum input-power reception	Maximum input-power reception	Number of cases	Sample in Figure 3
Gain ok and IIP_3 ok	NF ok and IIP_3 ok	MG-MP (−25%†)	LG-LP (−50%†)	74%	A
Gain↓ and IIP_3 ok	NF↑ and IIP_3 ok	HG-FP (100%†)	LG-LP (−50%†)	11%	B
Gain ok and IIP_3↓	NF ok and IIP_3↓	MG-MP (−25%†)	LG-MP (−25%†)	6%	C
Gain↓ and IIP_3↓↓	NF↑ and IIP_3↓	HG-FP (100%†)	LG-MP (−25%†)	8%	D
Gain↓ and IIP_3↓↓↓	NF↑ and IIP_3↓↓	HG-FP (100%†)	LG-FP (100%†)	1%	E and F

†Power consumption with respect to the full power modes.

Table 4: Performance comparison of LNAs for IEEE-802.15.4 receivers.

Reference	Tech. (nm)	f_o (GHz)	V_{DD} (V)	P_{DC} (mW)	Gain (dB)	NF (dB)	IIP_3 (dBm)	NF_{fs} (dB)	IIP_{3fs} (dBm)
This work	130	2.45	1.2	0.64	10.1	2.5	−8.1	25.3	4.2
				0.32	6.5	3.4	−13.3		
				0.64	4.6	4.5	−9.5		
[6]†	180	2.25	1.8	4.3	27	7	−11.5	41.9	25.3
				2.5	26	8	−9.5		
				1.1	19	9	−10.5		
[18]	90	2.45	1.2	0.68	9.7	4.36	−4	24.9	1.0

†Half the power from differential structure considered, in order to normalize comparison.

Receiver performance was evaluated using the values of NF_{fs} and IIP_{3fs} calculated to cover the worst cases of process variations (25.3 dB and 4.2 dBm, resp.).

Figure 5 shows the performance of NF and IIP_3 in the receiver under LNA supply variations, up to ±20% with respect to its nominal value (i.e., from 0.96 V to 1.44 V). Dashed lines indicate receiver requirements ($NF_{Rx} < 15.5$ dB; $IIP_{3Rx} > -10$ dBm), while color-filled markers denote the operation mode meeting each specification with the lowest power consumption. Receiver's NF rises as V_{DD} decreases, mainly because LNA gain drops due to a decrease of M_1's transconductance. On the other hand, despite the LNA gain reduction, receiver's IIP_3 also degrades for V_{DD} decreasing below 1.2 V, caused by degradation of LNA linearity. However, the proposed LNA shows up to be capable of counteracting these effects. When using MG-MP mode does not meet receiver's sensitivity ($NF_{RxMG\text{-}MP} > 15.5$ dB for $V_{DD} < 1.06$ V), switching to HG-FP mode allows fulfilling this requirement at the expense of increasing power consumption. Similarly, LG-LP mode cannot be used to receive the maximum input-signal level ($IIP_{3RxLG\text{-}LP} < -10$ dBm) for $V_{DD} < 1.03$ V, but lower gain modes maintain the required receiver's linearity (e.g., LG-MP in the analyzed range).

Regarding temperature variations, Figure 6 shows receiver's NF and IIP_3 behavior calculated using simulation results of the LNA, sweeping this parameter from −40°C to 85°C. When temperature increases, it causes the degradation of noise figure, while if it decreases then IIP_3 drops. Again, switching to higher power-consumption operation modes allows meeting the required sensitivity or linearity when needed ($NF_{RxMG\text{-}MP} > 15.5$ dB for $T > 49$°C; $IIP_{3RxLG\text{-}LP} < -10$ dBm for $T < -30$°C).

4.3. Comparison to Other Works. Table 4 compares the performance of the proposed LNA with previously published IEEE-802.15.4 LNAs (energy-aware [6] and conventional [18] designs). From our work, the following modes and cases from process-variation analysis are presented: the lowest gain (highest NF) case of HG-FP mode and the lowest IIP_3 case of LG-LP and LG-FP modes. In order to evaluate and compare the performance of each LNA in the receiver context, required NF and IIP_3 of the following stages were calculated and presented.

The power-saving ratio $[(P_{DCmax} - P_{DCmin})/P_{DCmax}]$ in [6] is better than ours (74% versus 50%), but our design presents significantly lower power consumption. The higher gain in [6] relaxes NF in the subsequent stages but demands better linearity in a similar degree. On the other hand, RF performance and full power consumption of the proposed LNA are comparable to those presented at [18], but ours can save up to 50% of power under relaxed working conditions.

5. Conclusions

A reconfigurable LNA with digitally controllable gain and power consumption is presented as an energy-aware solution. Novel design guidelines are given to minimize power consumption as a function of both communication-channel conditions and the effects of process variations. A 130 nm 1.2 V CMOS LNA following the presented proposal was designed for a 2.4 GHz IEEE-802.15.4 application, corroborating the effectiveness of the power-saving strategy. The designed LNA shows up to be capable of counteracting the effect of supply-voltage and temperature variations as well. Simulation results, taking into account worst cases under process variations,

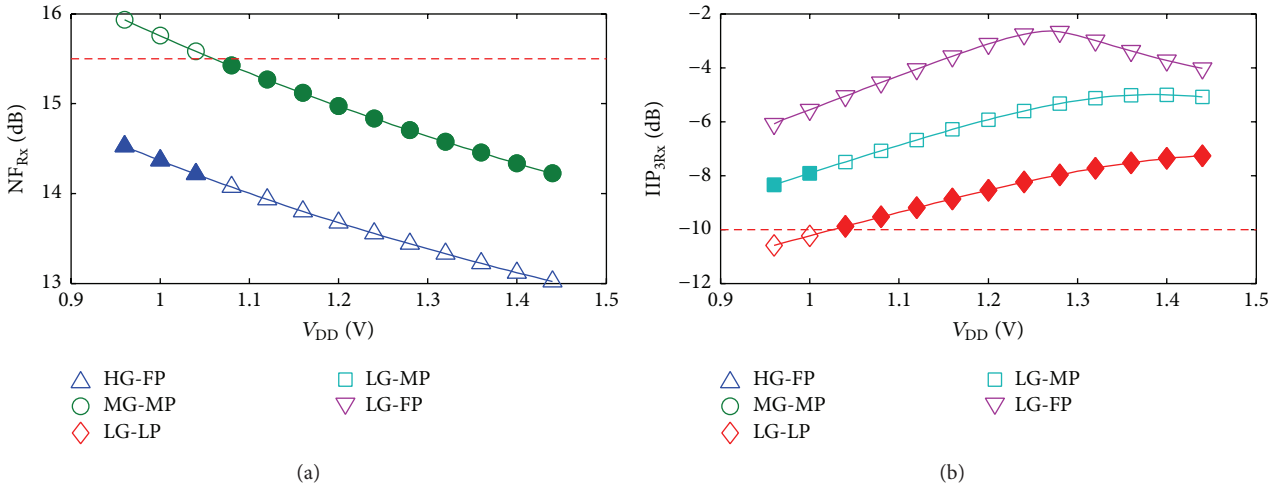

Figure 5: Receiver's NF (a) and IIP_3 (b) under LNA supply variations.

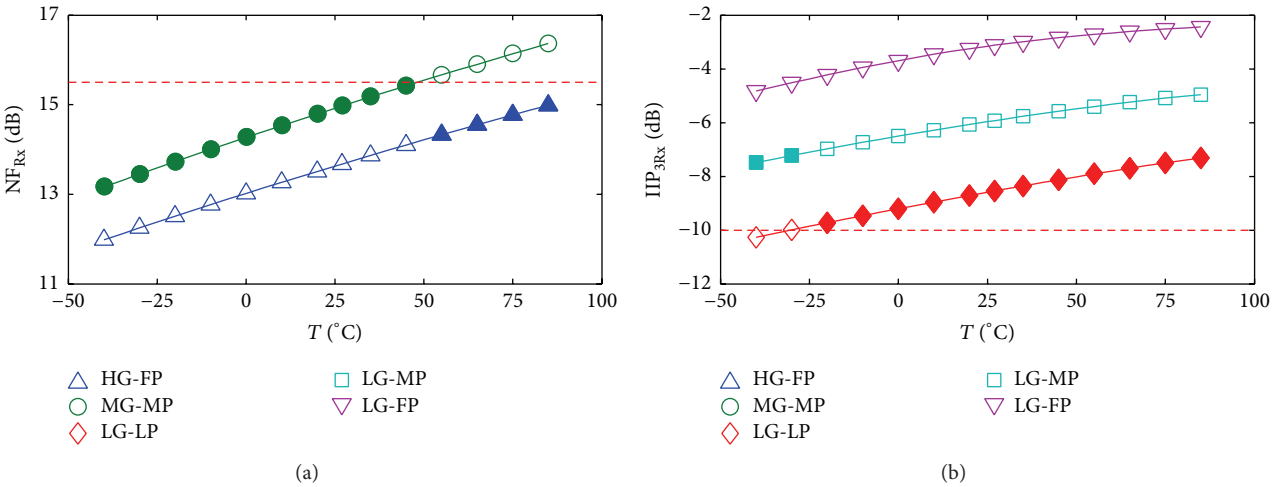

Figure 6: Receiver's NF (a) and IIP_3 (b) under LNA temperature variations.

are comparable to recently published works, having the advantage that significant power saving can be achieved with our proposal under relaxed working conditions.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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