Hindawi
Active and Passive Electronic Components
Volume 2017, Article ID 1609787, 12 pages
https://doi.org/10.1155/2017/1609787

Research Article

A Novel Floating Memristor Emulator with Minimal Components

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Received 4 July 2017; Revised 23 August 2017; Accepted 6 September 2017; Published 19 October 2017

Academic Editor: Jiun-Wei Horng

A new floating emulator for the flux-controlled memristor is introduced in this paper. The proposed emulator circuit is very simple and consists of only two current feedback operational amplifiers (CFOAs), two analog multipliers, three resistors, and two capacitors. The emulator can be configured as an incremental or decremental type memristor by using an additional switch. The mathematical model of the emulator is derived to characterize its behavior. The hysteresis behavior of the emulator is discussed in detail, showing that the pinched hysteresis loops in v-i plane depend not only on the amplitude-to-frequency ratio of the exciting signal but also on the time constant of the emulator circuit itself. Experimental tests are provided to validate the emulator's workability.

1. Introduction

The memristor, next to the resistor, the capacitor, and the inductor, was postulated as the fourth passive circuit element by Chua in 1971 [1]. It is defined as a two-terminal element that provides the missing constitutive relationship between charge and flux. Ignited by the successful fabrication of a real nanoscale memristor by HP Labs in 2008 [2], tremendous research has been devoted to explore memristor-based potential applications in such areas as resistive random access memory (RRAM) [3, 4], analog circuits [5, 6], digital circuits [7, 8], chaotic circuits [9, 10], and neural networks [11, 12]. Although memristor has many potential applications, it is not available as a universal electronic device for ordinary researchers. For this reason, a lot of SPICE models [13–15] were implemented to serve as a possible alternative to simulate memristor. But they cannot be used to build real-world applications. Recently, Bio Inspired Technologies has launched the world's first commercially available memristor [16]. However, it has a high price and can only be applied under special conditions in order to avoid irreparable damage [17]. Therefore, a replacement that behaves like a real memristor is still urgently needed to allow ordinary researchers to study memristor-based practical applications. Indeed, many memristor emulator circuits have been developed in recent years [17–32]. For example, using a JFET to implement the required nonlinearity, a memristor emulator constructed with five operational amplifiers, a floating capacitor, a large number of resistors, and an analog multiplier is presented in [19]. In addition to its complexity, the emulator reported in [19] is grounded and therefore is unsuitable for use as a two-terminal device in more complicated circuits. A unified approach for transforming nonlinear resistors into memristors is developed in [20], but the resultant emulators based on this methodology are limited by grounded operation. Emulator presented in [21, 22] can well imitate the features of TiO_2 memristor. However, the circuits are very complex and are built with an analog multiplier and a number of operational amplifiers (OAs), resistors, and MOS transistors. In order to make circuits in [21, 22] have a capacity of floating operation, further modification was made in [23] by adding a current conveyor. In [24], Sanchez-Lopez et al. proposed a floating memristor emulator which can operate at a high operating frequency (up to 14 kHz). But the circuit uses a large number of active and passive elements,

namely, five CFOAs, one analog multiplier, and a number of passive elements. Two simplified emulators with higher operating frequency were presented in [17, 26]. However, the grounded restriction places a substantial obstacle on their connectivity with other circuit elements. The emulator circuit in [27] uses a light-dependent resistor (LDR) to provide the required nonlinearity. Although the emulator circuit is very simple, it can only work at low frequency and has a narrow variation range of memristance. Pershin and Ventra built a memristor emulator using digital and analog mixed circuits [28]. The resolution of its memristance, however, is limited by the limited performance of the A/D converters. Using diode-resistive networks to implement the required nonlinearity, a binary-level emulator was developed in [29] and a continuous-level emulator implemented by using the nonlinear transfer characteristics of OTA was presented in [30] by Abuelma'atti and Khalifa. However, the grounded restriction is still the main obstacle to its connectivity with other circuit elements. A floating emulator, which is built with four CFOAs and avoids the use of analog multipliers, was developed by the same authors [31]. In order to make it successfully emulate a floating memristor, the emulator circuit must satisfy strict parameter matching conditions. An electronically tunable memristor emulator circuit is presented in [32] and its memristance value can be controlled by changing transconductance parameters of the used OTAs.

In this paper, we propose a floating memristor emulator, which is built with two CFOAs, two analog multipliers, and five passive elements. In fact, multipliers are often used to realize the product of voltage and flux (current and charge) for the design of the flux-controlled (charge-controlled) memristor emulators [21–27]. Different from the above design methods, however, herein the multipliers are employed to construct a floating voltage-controlled resistor (VCR). The emulator is implemented by using the flux across it as the controlled voltage of the VCR. The proposed emulator not only has a simple topology but also can be configured as an incremental or decremental type memristor. The mathematical model of the emulator is derived in detail. Its hysteresis behavior is further discussed, showing that the pinched hysteresis loops in v-i plane depend not only on the amplitude-to-frequency ratio of the exciting signal but also on the time constant of the emulator circuit itself. Furthermore, PSpice simulations and experimental tests are included to demonstrate the properties of the emulator. The organization of the paper is as follows: in Section 2, we introduce our emulator circuit and derive its mathematical model, hysteresis behavior analysis is performed in Section 3, and PSpice simulations and experimental results are given in Sections 4 and 5, respectively. We conclude the paper in the last section.

2. Proposed Floating Emulator Circuit

The memristor completes the missing link between charge q and flux ϕ. When its constitutive relation is expressed as a single-valued function $q_m = q_m(\phi_m)$, the memristor is flux-controlled and can be characterized by its memductance $W(\phi_m)$, which describes the ratio of change of the charge q_m with respect to the flux ϕ_m across the device:

$$W(\phi_m) = \frac{dq_m(\phi_m)}{d\phi_m}. \tag{1}$$

The corresponding i-v relationship of the memristor in this case is expressed as

$$i_m(t) = \frac{dq_m(t)}{dt} = \frac{dq_m}{d\phi_m} \times \frac{d\phi_m}{dt} = W(\phi_m)\, v_m(t). \tag{2}$$

The proposed floating flux-controlled memristor emulator circuit is shown in Figure 1. It is composed of two AD844 type CFOAs, two AD633 type analog multipliers, three resistors, and two capacitors. Here, R_{x1} and R_{x2} are parasitic resistors at X-terminal of AD844(1) and AD844(2); R_{z1} and R_{z2} and C_{z1} and C_{z2} are the parasitic resistors and capacitors associated with Z-terminal. Each CFOA is characterized by the following terminal relations [20]:

$$\begin{aligned} i_Z &= \alpha i_X, \\ i_Y &= 0, \\ v_X &= \beta v_Y, \\ v_W &= \delta v_Z, \end{aligned} \tag{3}$$

where α, β, and δ are the port transfer ratios. From Figure 1, the current through the resistor R_1 can be expressed as

$$i_{R1} = \frac{\beta_1 v_A - \beta_2 v_B}{R_1 + R_{x1} + R_{x2}}. \tag{4}$$

The current will be transferred to Z-terminal of AD844(1) and it will be integrated by the capacitors C_1 and C_{z1} to produce a output voltage at W-terminal of AD844(1) given by

$$v_{1\text{out}} = \frac{\alpha_1 \delta_1}{1/R_{z1} + s(C_1 + C_{z1})} i_{R1}. \tag{5}$$

The influence of the parasitic resistor R_{z1} on the emulator circuit is negligible due to its high resistance value which is approximately 3 MΩ. Substituting (4) into (5), one can obtain the output voltage $v_{1\text{out}}$ given by

$$v_{1\text{out}} = \frac{\alpha_1 \delta_1}{(C_1 + C_{z1})(R_1 + R_{x1} + R_{x2})} \int (\beta_1 v_A - \beta_2 v_B)\, dt. \tag{6}$$

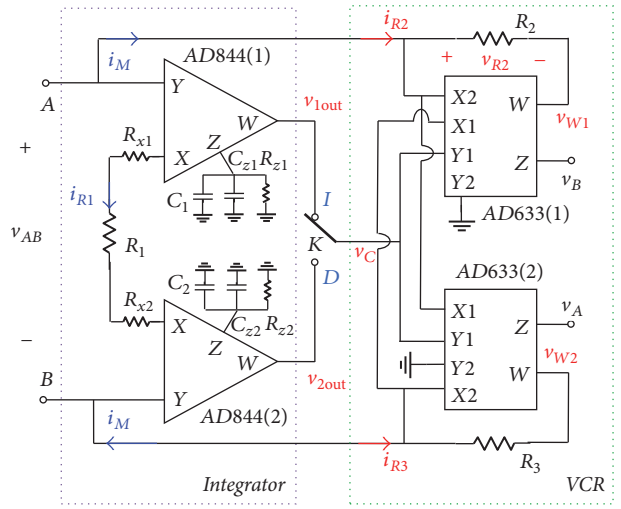


FIGURE 1: The proposed floating memristor emulator circuit.

Considering the fact that $\beta_1 \approx \beta_2$, (6) can be rewritten as

$$v_{1\text{out}} = \frac{\alpha_1 \delta_1 \beta_1}{(C_1 + C_{z1})(R_1 + R_{x1} + R_{x2})} \phi_{AB}, \tag{7}$$

where ϕ_{AB} corresponds to the flux across the emulator and it is defined as $\phi_{AB} = \int_0^t (v_A - v_B) d\tau$. Here, we consider that the initial condition of the integrator is zero. Similarly, one can obtain the output voltage $v_{2\text{out}}$:

$$v_{2\text{out}} = -\frac{\alpha_2 \delta_2 \beta_2}{(C_2 + C_{z2})(R_1 + R_{x1} + R_{x2})} \phi_{AB}. \tag{8}$$

Analog multipliers AD633(1) and AD633(2) and the resistors R_1 and R_2 construct a floating voltage-controlled resistor (VCR) and v_C is the controlled voltage. Referring to the input-to-output characteristic of AD633, the output voltages v_{W1} and v_{W2} can be given as

$$\begin{aligned} v_{W1} &= \frac{(v_B - v_A) v_C}{10} + v_B, \\ v_{W2} &= \frac{(v_A - v_B) v_C}{10} + v_A. \end{aligned} \tag{9}$$

Thus, the currents i_{R2} and i_{R3} can be expressed as

$$\begin{aligned} i_{R2} &= \frac{v_A - v_{W1}}{R_2} = \frac{v_A - ((v_B - v_A) v_C/10) - v_B}{R_2}, \\ i_{R3} &= \frac{v_B - v_{W2}}{R_3} = \frac{v_B - ((v_A - v_B) v_C/10) - v_A}{R_3} \\ &= -\frac{v_A - \left(\dfrac{(v_B - v_A) v_C}{10}\right) - v_B}{R_3}. \end{aligned} \tag{10}$$

It is can be inferred from (10) that $i_{R3} = -i_{R2}$ holds if $R_2 = R_3 = R$ is satisfied. Thus, the equivalent conductance of the VCR can be described as

$$G_{\text{eq}} = \frac{i_{R2}}{(v_A - v_B)} = G\left(1 + \frac{v_C}{10}\right), \tag{11}$$

where $G = 1/R$. From Figure 1, when the switch K is switched to node I, that is, $v_C = v_{1\text{out}}$, the emulator realizes an incremental type memristor and the corresponding memductance can be expressed as

$$\begin{aligned} &W_I(\phi_{AB}) \\ &\quad = G\left(1 + \frac{\alpha_1 \delta_1 \beta_1}{10(R_1 + R_{x1} + R_{x2})(C_1 + C_{z1})} \phi_{AB}\right). \end{aligned} \tag{12}$$

When the switch K is switched to node D, that is, $v_C = v_{2\text{out}}$, the emulator is equivalent to a decremental type memristor whose memductance is decided by

$$\begin{aligned} &W_D(\phi_{AB}) \\ &\quad = G\left(1 - \frac{\alpha_2 \delta_2 \beta_2}{10(R_1 + R_{x1} + R_{x2})(C_2 + C_{z2})} \phi_{AB}\right). \end{aligned} \tag{13}$$

Thus the emulator has the same advantage as the emulators in [17, 23]; that is, the incremental or decremental type memristor can be interchanged by using an additional switch K. Due to $C_{z1} \approx C_{z2}$, $\alpha_1 \approx \alpha_2$, $\delta_1 \approx \delta_2$, and $\beta_1 \approx \beta_2$ and assuming that $C_1 = C_2$, (12) and (13) can be described as the following unified expression:

$$W(\phi_{AB}) = G\left(1 \pm \frac{\alpha_1\delta_1\beta_1}{10(R_1 + R_{x1} + R_{x2})(C_1 + C_{z1})}\phi_{AB}\right). \quad (14)$$

It can be seen from (14) that the two different type memductances are linearly dependent on the flux $\phi_{AB}(t)$; thus the emulator is flux-controlled, and it can be controlled by a voltage imposed on the input terminals.

3. Hysteresis Behavior Analysis

In order to study the hysteresis behavior of the proposed emulator, assuming that a sinusoidal voltage $v_{AB} = A_m \sin 2\pi ft$ is applied on terminals A and B, the flux across the device is $\phi_{AB} = (A_m/2\pi f)\cos(2\pi ft - \pi)$. Note that the initial condition of the integrator, for the sake of simplicity, is considered as zero. As a consequence, the memductance $W(\phi_{AB})$ can be calculated as

$$W(\phi_{AB}) = G \pm \frac{A_m\alpha_1\delta_1\beta_1}{20\pi(R_1 + R_{x1} + R_{x2})(C_1 + C_{z1})f}G \cdot \cos(2\pi ft - \pi). \quad (15)$$

It is seen from (15) that the memductance is composed of a linear time-invariant conductance and a linear time-varying conductance. The pinched hysteresis behavior of the emulator is dependent on the relationship between the time-varying and time-invariant parts of the memductance [21]. The relationship between the two parts can be described by the ratio of their amplitudes, given as

$$k = \frac{A_m\alpha_1\delta_1\beta_1}{20\pi(R_1 + R_{x1} + R_{x2})(C_1 + C_{z1})f} = \frac{r_{A/F}}{\tau}, \quad (16)$$

where $\tau = 20\pi(R_1 + R_{x1} + R_{x2})(C_1 + C_{z1})/\alpha_1\delta_1\beta_1$ is the time constant of the emulator itself; $r_{A/F} = A_m/f$ is the amplitude-to-frequency ratio of the stimulating signal. From (16), one can deduce that the pinched hysteresis behavior depends not only on the amplitude-to-frequency ratio of the stimulating signal but also on the time constant of the emulator circuit itself. There are three cases between k and the pinched hysteresis loop of the proposed memristor:

(1) $k \to 0$ when $r_{A/F} \ll \tau$. The memductance is dominated by a linear time-invariant conductance and the pinched hysteresis loop shrinks into a straight line.

(2) $k \to 1$ when $r_{A/F} \to \tau$. The corresponding memductance variation range is $(0, 2G)$ from (15) and the maximum pinched hysteresis loop can be achieved.

(3) $k > 1$ when $r_{A/F} > \tau$. The memductance has zero or negative conductance value and the hysteresis loop is lost.

As a consequence, in order to hold the pinched hysteresisloop, the numerical value of k must lie on the interval $0 < k < 1$. This means that τ must be updated according to f and A_m. The task can be done by updating the values of capacitors C_1 and C_2 with the following expression:

$$C_1 = C_2 = \frac{A_m\alpha_1\delta_1\beta_1}{20\pi k(R_1 + R_{x1} + R_{x2})f} - C_{z1}. \quad (17)$$

For simplicity, we assume that $A_m = 0.5V_p$, $k = 1$, $R_{x1} = R_{x2} = 50\,\Omega$, and $\alpha_1 = \delta_1 = \beta_1 = 0.98$; the circuit parameters of the chosen elements in Figure 1 for different operating frequency are given in Table 1. It is worth noting that the parasitic capacitors C_{z1} and C_{z2} are negligible, since their values are far less than those of the capacitors C_1 and C_2.

Table 1: Circuit parameters for different frequency ranges.

f (Hz)	10–100	100–1 k	1 k–10 k	10 k–35 k
R_1 (Ω)		7.5 k		
$R_2 = R_3$ (Ω)		10 k		
$C_1 = C_2$ (F)	100n	10n	1n	100p

4. PSpice Simulations

In order to verify the workability of the proposed emulator, using the circuit parameters given in Table 1 for $C_1 = C_2 = 100$ nF, the circuit was simulated by PSpice simulator. A sinusoidal voltage with $f = 10$ Hz and $A_m = 0.5V_p$ is applied across the memristor; the transient waveforms of $v_{AB}(t)$, $i_m(t)$, and $W(t)$ in the incremental type emulator are shown in Figure 2(a). The corresponding hysteresis loop is pinched at the origin in v-i plane, as illustrated in Figure 2(b). It can be seen from Figure 2(a) that the injected sinusoidal voltage produces a distorted current due to the nonlinearity of the memductance. Inspection of Figure 2(a) clearly also shows that the memductance varies periodically in the range of 0 to 200 uS under the sinusoidal voltage excitation. The similar simulation results, as shown in Figure 3, are obtained with the same circuit parameters when the circuit is configured as the decremental type memristor. Comparing Figure 2(b) with Figure 3(b), one can find that the incremental type memristor and the decremental type memristor have the same hysteresis loop in v-i plane. But the hysteresis loop of the incremental type memristor moves counterclockwise in the first quadrant and clockwise in the third quadrant, while that of the decremental type memristor is just the reverse.

In order to observe the impact of circuit parameter variations on the pinched hysteresis loop, Monte Carlo analysis was performed for all passive elements with the above circuit parameters, where 5% Gaussian deviations were used. As a consequence, Figures 4(a) and 4(b) illustrate the simulation results for the incremental and the decremental types, respectively. As seen from Monte Carlo analysis results, the proposed emulator circuit has reasonable sensitivity performances.

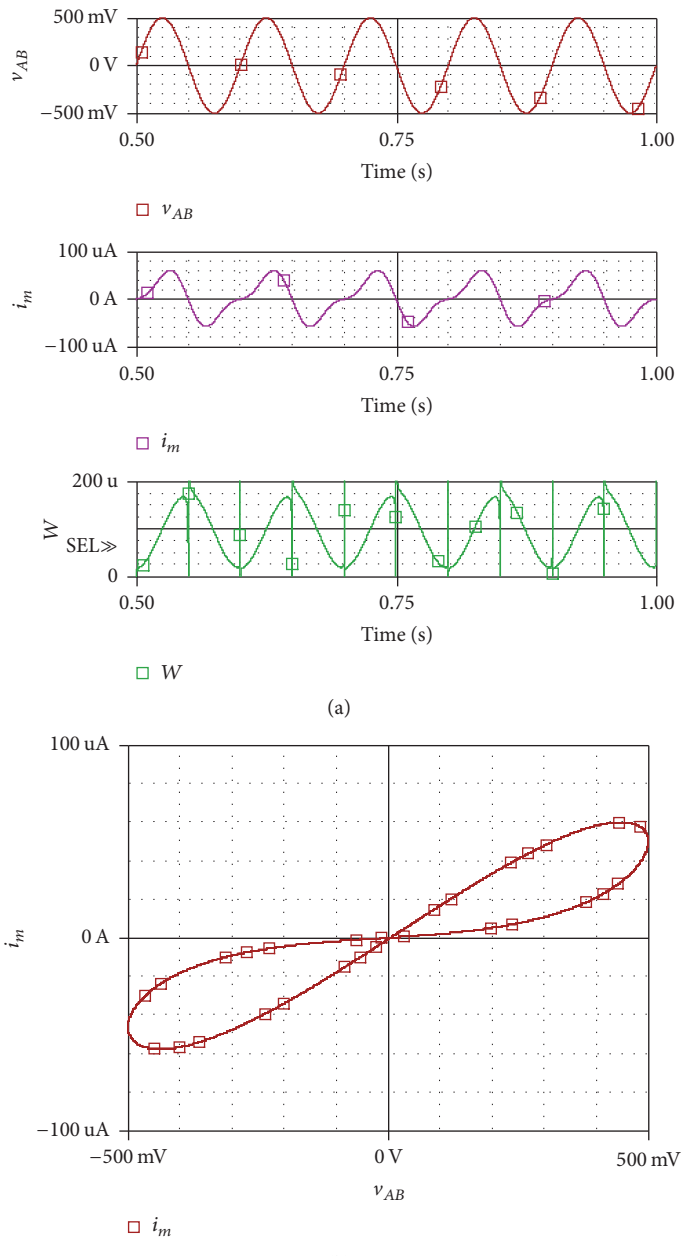


FIGURE 2: PSpice simulation results obtained with the incremental type memristor. (a) Time waveforms of the input voltage v_{AB}, the input current i_m, and the memductance W; (b) hysteresis loops in v-i plane operating at 10 Hz.

5. Experimental Tests

The emulator circuit was also implemented with off-the-shelf electronic devices on a prototype PCB for experimental validation and observation of the hysteresis behavior. Circuit parameters for different operating frequency ranges used in experimental tests are presented in Table 1. Since the voltage v_{R2} is proportional to the current i_m with coefficient R_2 from Figure 1, v_{R2} is used to indirectly represent the current i_m in the process of experimental tests. In order to obtain the voltage v_{R2}, an additional differential amplifier circuit built with operational amplifiers is also included in the experimental testing platform, as shown in Figure 5.

When a sinusoidal voltage signal with $f = 10$ Hz and $A_m = 0.5V_p$ is applied to the emulator circuit, the transient waveforms of $v_{AB}(t)$ and $i_M(t)$ are shown in Figure 6(a). The hysteresis loop is pinched at the origin in v-i plane as shown in Figure 6(b). When the stimulus frequency f is increased to 50 Hz and 100 Hz, the corresponding hysteresis loops are illustrated in Figures 6(c) and 6(d), respectively. Inspection of Figures 6(b)–6(d) clearly shows that the lobe area decreases gradually as the frequency increases, and when f is increased

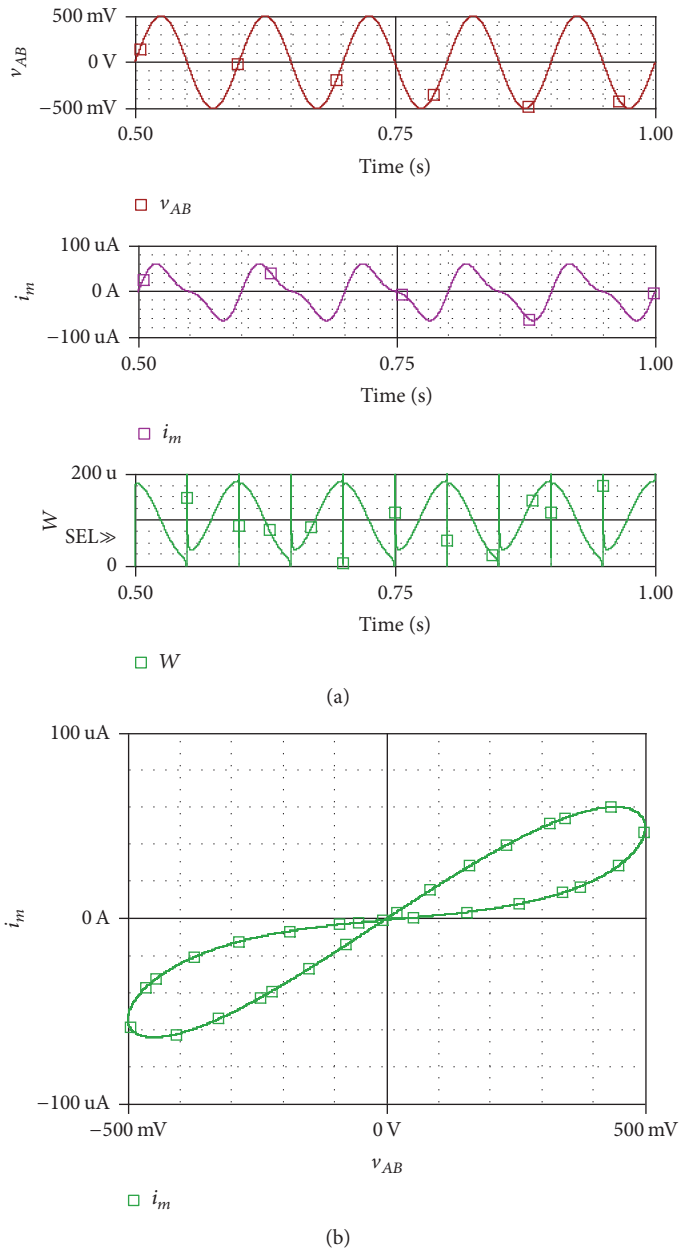


FIGURE 3: PSpice simulation results obtained with the decremental type memristor. (a) Time waveforms of the input voltage v_{AB}, the input current i_m, and the memductance W; (b) hysteresis loops in v-i plane operating at 10 Hz.

to 100 Hz the hysteresis loop shrinks into a straight line. On the contrary, when the stimulus frequency is decreased to 7 Hz, which results in $k > 1$ from (16), the hysteresis loop shown in Figure 6(e) is not complete and it is in a state of imminent disappearance. Figures 6(b)–6(e) demonstrate the unique property of memristors, namely, the frequency-dependence of hysteresis loop.

Furthermore, in order to maintain the hysteresis loop at high frequency, we scale down the capacitors C_1 and C_2 to 10 nF. Figures 7(a) and 7(b) show the experimental results for $f = 100$ Hz and $f = 500$ Hz, respectively. When stimulus frequency f is increased to 1 kHz, the memductance $W(\phi_m)$ is mainly dominated by the linear time-invariant conductance and the corresponding hysteresis loop approximates a straight line as shown in Figure 7(c).

Similarly, when the capacitors C_1 and C_2 are scaled down to 1 nF, the pinched hysteresis loops operating at $f = 1$ kHz, $f = 5$ kHz, and $f = 10$ kHz are given in Figures 8(a), 8(b), and 8(c), respectively. When the capacitors C_1 and C_2 are further scaled down to 100 pF, the emulator circuit can still perform hysteresis behavior at $f = 10$ kHz as shown in Figure 9(a). Unfortunately, when the stimulus frequency f is increased to 35 kHz, the hysteresis loop does not pinch at the origin and thus performs an asymmetrical behavior as

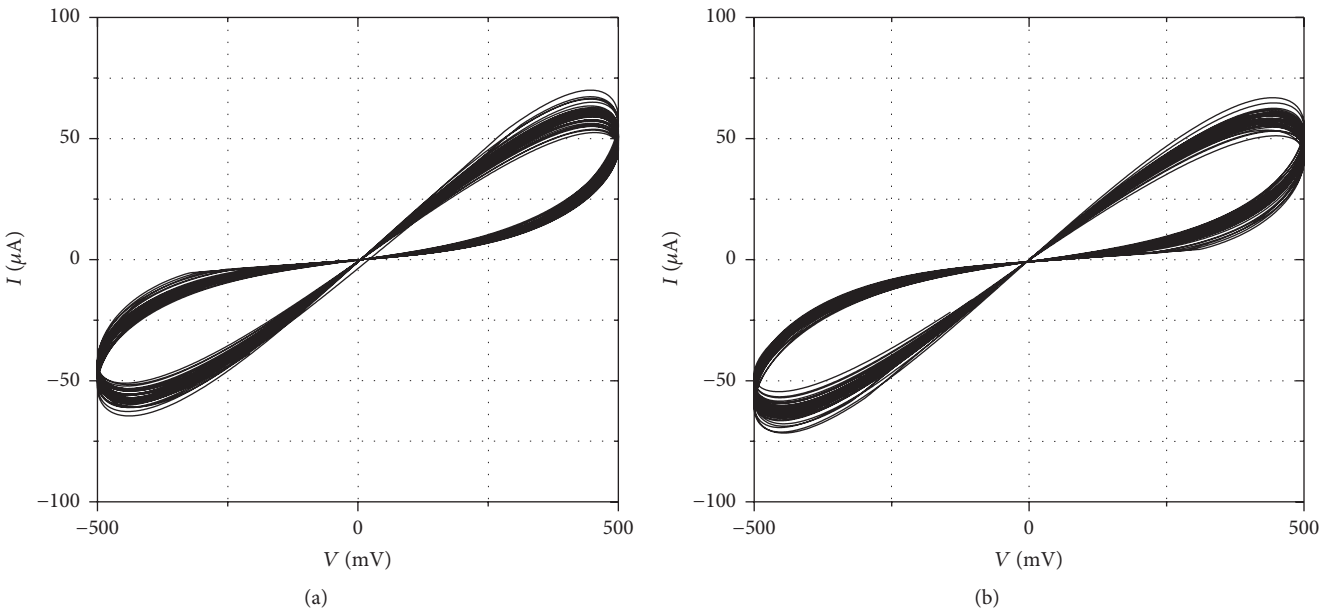


Figure 4: Monte Carlo analysis of the emulator for all passive elements: (a) the incremental type and (b) the decremental type.

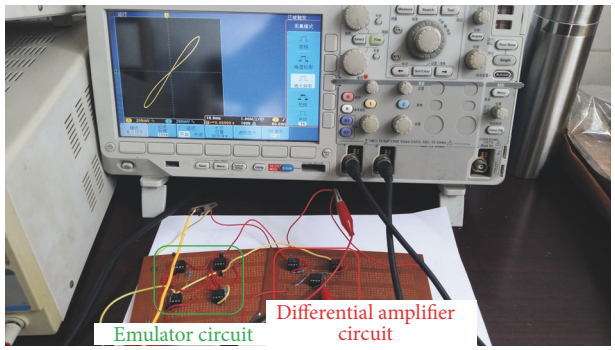


Figure 5: Experimental testing platform.

shown in Figure 9(b). This deformation will become more and more serious with the increase of the stimulus frequency. Figure 9(c) illustrates the hysteresis loop operating at 50 kHz. As can be observed, not only is the pinched hysteresis loop more deviated from the origin, but also the areas enclosed in the first and third quadrants are not equal.

The same experimental tests were conducted on the decremental type emulator. The pinched hysteresis loops can also be obtained by updating the capacitors C_1 and C_2 for different operating frequency ranges. For example, Figures 10(a), 10(b), and 10(c) illustrate the hysteresis loops operating at 1 kHz, 5 kHz, and 10 kHz, respectively. When the capacitors C_1 and C_2 are scaled down to 100 pF, the hysteresis loops operating at 10 kHz, 35 kHz, and 50 kHz are depicted in Figures 11(a), 11(b), and 11(c). It is evident from Figure 11(b) that the decremental emulator exhibits a deformed hysteresis loop just as the incremental emulator performs when the stimulus frequency f is increased to the top limit of 35 kHz. This deformation is due mainly to the integrator circuit nonidealities, which is built with C_1, C_2, R_1, and AD844(1) and AD844(2) along with the parasitic elements at their Z-terminals. The effect of the parasitic elements is negligible when the operating frequency f is low. But when the operating frequency f is increased monotonically, the parasitic elements manifest themselves as a high offset voltage imposed on the output of the integrator circuit. Due to this, the hysteresis loop does not pinch at the origin, and the areas enclosed in the first and third quadrants are not equal. In order to avoid the deformation of the hysteresis loop, both the incremental type and the decremental type memristors can only be used from 10 Hz to 35 kHz.

To further verify the effectiveness of the emulator, a pulse train (0.5 V, 10 ms duration, 30 ms period) is applied

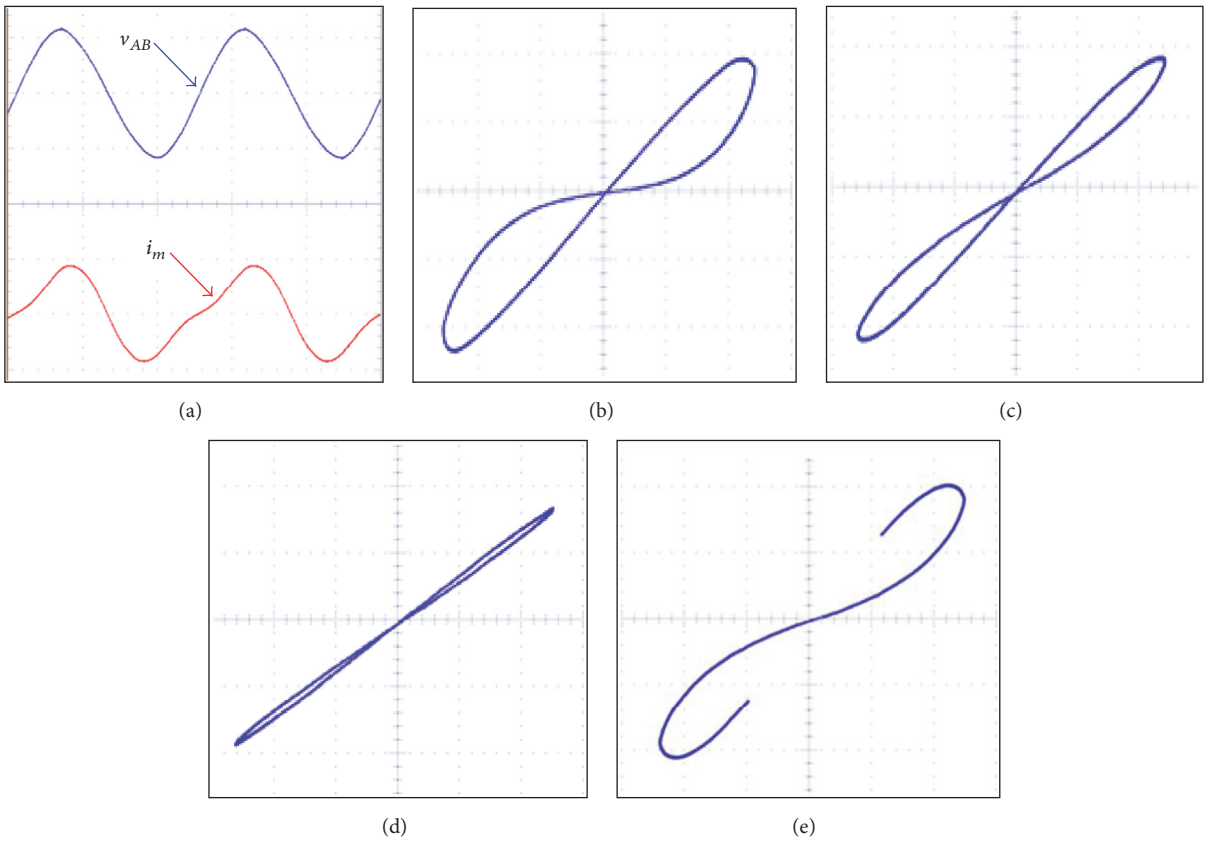


FIGURE 6: Experimental results of the incremental type emulator when $C_1 = C_2 = 100$ nF. (a) waveforms of the input voltage v_{AB} and input current i_M in the time domain; (b), (c), (d), and (e) represent hysteresis loops in v-i plane operating at 10 Hz, 50 Hz, 100 Hz, and 7 Hz, respectively. The time scale is 40 ms/div, and scales are 0.2 V/div for x-axis and 0.2 V/div for y-axis.

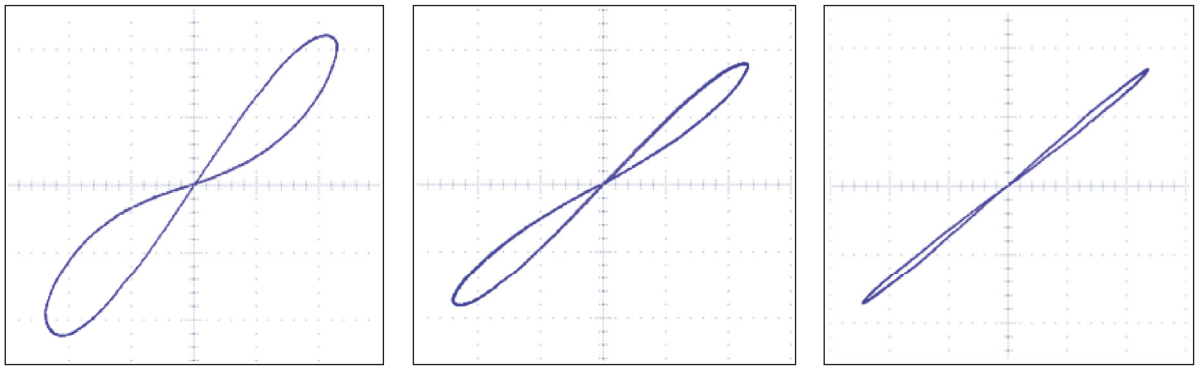
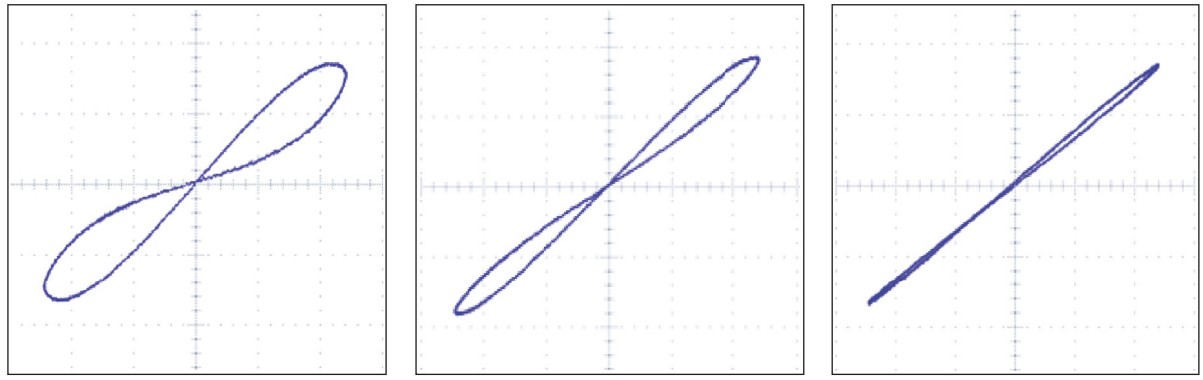


FIGURE 7: Experimental results of the incremental type emulator when $C_1 = C_2 = 10$ nF. (a), (b), and (c) represent hysteresis loops in v-i plane operating at 100 Hz, 500 Hz, and 1 kHz, respectively. The scales are 0.2 V/div for x-axis and 0.2 V/div for y-axis.

successively to the input of emulator circuit; the current i_m is experimentally measured by using the circuit parameters given in Table 1 for $C_1 = C_2 = 100$ nF. Figures 12(a) and 12(b) illustrate the current responses of the incremental type and the decremental type memristors under successive voltage pulse excitation, respectively. For the incremental type, the current i_m increases as more voltage pulses are applied. Thus, one can indirectly infer that its memductance increases as input voltage pulses are applied, whereas for the decremental type, we can derive the opposite conclusion.

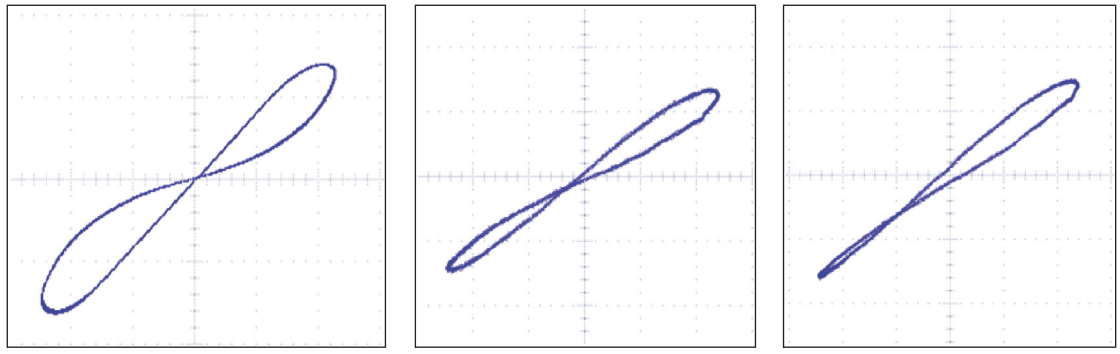
6. Conclusions

In this paper, a floating emulator circuit for the flux-controlled memristor has been presented. The proposed simulator is very simple and contains only two CFOAs, two



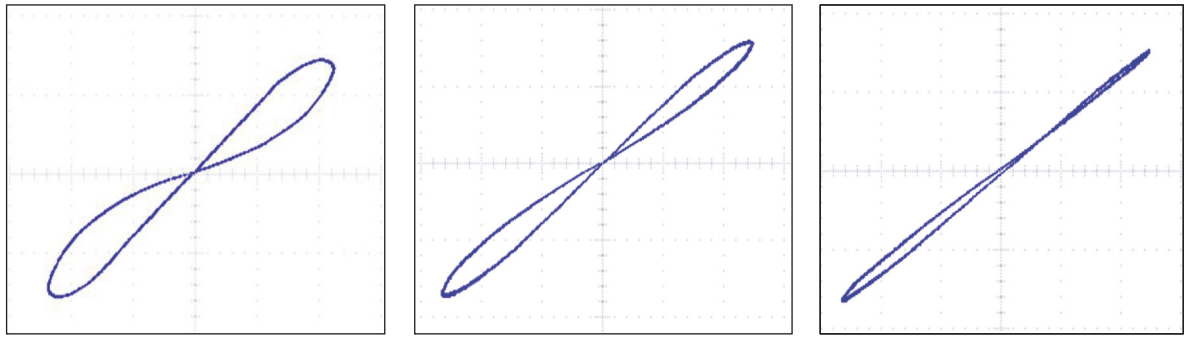
(a) (b) (c)

Figure 8: Experimental results of the incremental type emulator when $C_1 = C_2 = 1$ nF. (a), (b), and (c) represent hysteresis loops in v-i plane operating at 1 kHz, 5 kHz, and 10 kHz, respectively. The scales are 0.2 V/div for x-axis and 0.2 V/div for y-axis.



(a) (b) (c)

Figure 9: Experimental results of the incremental type emulator when $C_1 = C_2 = 100$ pF. (a), (b), and (c) represent hysteresis loops in v-i plane operating at 10 kHz, 35 kHz, and 50 kHz, respectively. The scales are 0.2 V/div for x-axis and 0.2 V/div for y-axis.



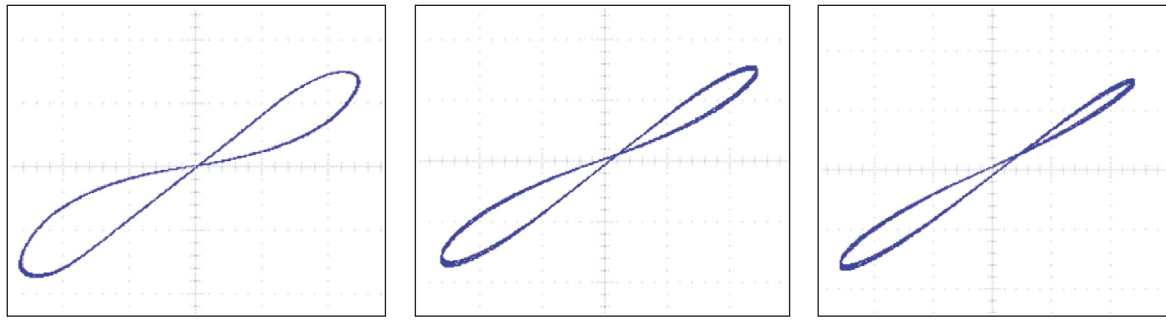
(a) (b) (c)

Figure 10: Experimental results of the decremental type emulator when $C_1 = C_2 = 1$ nF. (a), (b), and (c) represent hysteresis loops in v-i plane operating at 1 kHz, 5 kHz, and 10 kHz, respectively. The scales are 0.2 V/div for x-axis and 0.2 V/div for y-axis.

Table 2: Comparison of presented emulator with other published studies.

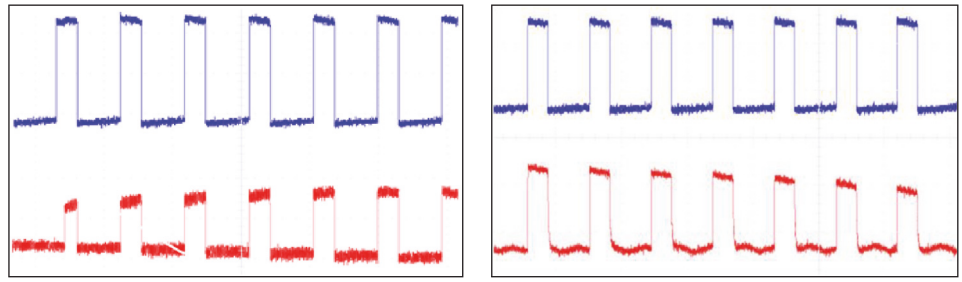
Emulators	Employed circuit elements	Floating/grounded type	Operating frequency range	Memristance or memductance variation range	Incremental/decremental type
[17]	1 CFA, 1 multiplier, 1 capacitor, 1 resistor, and 2 DC voltage sources	Grounded	16 Hz–860 kHz	/	Both
[19]	1 multiplier, 5 OAs, 1 JFET, 1 capacitor, and 9 resistors	Grounded	/	Narrow	Incremental
[21, 22]	1 multiplier, 5 OAs, 10 MOSs, 1 capacitor, and 8 resistors	Grounded	100 Hz–800 Hz	$4.5\,k\Omega < M < 16\,k\Omega$	Both
[23]	1 multiplier, 6 OAs, 1 CCII, 10 MOSs, 1 capacitor, 10 resistors, 1 diode	Floating	5 Hz–100 Hz	$4.5\,k\Omega < M < 16\,k\Omega$	Both
[24]	1 multiplier, 5 CFOAs, 1 capacitor, and 5 resistors	Floating	16 Hz–14 kHz	/	Incremental
[26]	1 multiplier, 2 CFOAs, 1 capacitor, and 4 resistors	Grounded	16 Hz–160 kHz	/	Both
[27]	3 OAs, 1 LDR, 1 capacitor, and 11 resistors	Grounded	/	$500\,\Omega < M < 1\,k\Omega$	Incremental
[28]	1 digital potentiometer, 1 ADC, and 1 microcontroller	Grounded	0.2 Hz–50 Hz	$50\,\Omega < M < 10\,k\Omega$	Incremental
[29]	3 CFOAs, 2 capacitors, 1 diode, and 4 resistors	Grounded	/	Binary state levels	/
[30]	2 CFOAs, 1 OTA, 2 capacitors, and 3 resistors	Grounded	/	/	Incremental
[31]	4 CFOAs, 4 capacitors, 2 resistors, and 2 potentiometers	Floating	/	Binary state levels	/
[32]	4 CCIIs, 3 OTAs, 5 resistors, 1 capacitor, and 1 DC voltage source	Floating	/	$0 < M < 2R_1$	Decremental
Presented	2 CFOAs, 2 multipliers, 2 capacitors, and 3 resistors	Floating	10 Hz–35 kHz	$0 < W < 2G$	Both

multipliers, three resistors, and two capacitors. The emulator has been built with commercially available AD844 and AD633 ICs. Experimental results show that the proposed emulator circuit satisfies the three fingerprints of the memristor [30] and reveal how the frequency of the exciting voltage signal modifies its hysteresis behavior. When compared with the existing memristor emulator circuits, the proposed emulator not only has a simple topology but also can be configured as an incremental or decremental type memristor. Furthermore, the emulator can hold up the frequency-dependent pinched hysteresis loop at high frequency by updating the values of capacitors C_1 and C_2. Detailed comparison of the presented emulator circuit with other published studies is summarized in Table 2. Since



(a) (b) (c)

Figure 11: Experimental results of the decremental type emulator when $C_1 = C_2 = 100$ pF. (a), (b), and (c) represent hysteresis loops in v-i plane operating at 10 kHz, 35 kHz, and 50 kHz, respectively. The scales are 0.2 V/div for x-axis and 0.2 V/div for y-axis.



(a) (b)

Figure 12: Current responses of emulator under pulse excitation. (a) Incremental type emulator; (b) decremental type emulator. The time scale is 25 ms/div and scale is 0.2 V/div for y-axis.

the emulator circuit can easily be implemented with the commercially available electronic devices, it can be used for memristor-based circuit designs and applications.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

The authors would like to acknowledge the National Natural Science Foundation of China (Grants nos. 61176032 and 61471310) and the Natural Science Foundation of Hunan Province (Grants nos. 2015JJ2142 and 2015JJ2140) for supporting this research.

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