Hindawi
Active and Passive Electronic Components
Volume 2017, Article ID 1836727, 8 pages
https://doi.org/10.1155/2017/1836727

Research Article

Operational Simulation of LC Ladder Filter Using VDTA

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Received 29 June 2016; Revised 18 November 2016; Accepted 4 December 2016; Published 23 January 2017

Academic Editor: Jiun-Wei Horng

In this paper, a systematic approach for implementing operational simulation of LC ladder filter using voltage differencing transconductance amplifier is presented. The proposed filter structure uses only grounded capacitor and possesses electronic tunability. PSPICE simulation using 180 nm CMOS technology parameter is carried out to verify the functionality of the presented approach. Experimental verification is also performed through commercially available IC LM13700/NS. Simulations and experimental results are found to be in close agreement with theoretical predictions.

1. Introduction

Current mode approach has received a considerable attention in the last few years for analog signal processing applications due to their low power consumption, large dynamic range, higher frequency ranges of operation, better accuracy, higher slew rate, and less complexity. As a result, a large number of current mode active elements such as operational transconductance amplifier (OTA), current conveyor (CC), current controlled conveyor (CCC), current feedback amplifier (CFOA), operational transresistance amplifier (OTRA), differential voltage current conveyor (DVCC), current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA), and voltage differencing transconductance amplifier (VDTA) are published. A literature review of such analog active block is presented in [1, 2]. The VDTA is a recently proposed analog building block composed of two transconductance amplifiers and may be used to implement different analog processing application such as floating and grounded inductor simulation [3, 4], analog filter [5–10], and oscillators [11–13].

For the active simulation of higher-order LC ladder filter, mainly three methods exist, which are wave active method, topological simulation, and operational simulation. In wave active approach, a wave equivalent is developed for inductor in series branch and then it is configured for other passive components by making suitable connection [14–21]. Large numbers of active blocks are used in this approach. In the second method, topological simulation or element replacement method, the inductor of LC ladder structure is replaced by appropriate configured active elements [22, 23]. The drawback of this configuration is that a floating capacitor is generally required and this degrades the performance of the derived filter topology in high frequency application. In the third approach, operational simulation or leap-frog method [23–30], simulation is carried out for the operation of ladder rather than its component.

Literature survey reveals the operational simulation of ladder filter using operational amplifier (OA) and current controlled conveyor (CCCII) [24], OTA [25, 26], CC [27], multiple output second generation current controlled conveyor (MO-CCCII) [28], current feedback amplifier (CFA) [29], and CFOA [30]. This paper presents a systematic approach for operational simulation of LC ladder filter using voltage differencing transconductance amplifier (VDTA). The proposed operational simulation of LC ladder using VDTA has the following advantage over existing circuits:

(i) Lesser numbers of active blocks are used as compared to [24, 26, 28–30].

(ii) There is no use of resistors in realization, while [25, 29, 30] use both floating and grounded resistors and [27] uses only grounded resistors.

(iii) Only grounded capacitors are used in proposed implementation, while [25, 29] use floating capacitors too.

(iv) Proposed operational simulation of LC ladder also possesses electronic tunability of cut-off frequency, while [27, 29, 30] do not.

As an example, a fourth-order Butterworth low pass filter is simulated by outlined approach and the workability of the filter is confirmed through PSPICE simulation using 180 nm CMOS technology parameter. The functionality of the ladder filter is also tested experimentally through IC LM13700/NS.

2. VDTA

The voltage differencing transconductance amplifier is consisting of two transconductance amplifiers [5]. Figures 1 and 2 represent the symbolic representation and CMOS implementation of VDTA.

The port relationship of VDTA in matrix form is characterized by the following equation:

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{mi} & -g_{mi} & 0 \\ 0 & 0 & g_{mo} \\ 0 & 0 & -g_{mo} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}, \tag{1}$$

where g_{mi} and g_{mo} are the input and output transconductance gain of VDTA. The input transconductance amplifier converts the input voltage difference $(V_P - V_N)$ into current at Z terminal and the voltage developed at Z terminal is converted into current at $X+$ and $X-$ terminal by output transconductance amplifier. In this paper, VDTA is used as an active analog building block because of

(i) the simple CMOS implementation of VDTA,

(ii) presence of two transconductance amplifiers giving resistorless realization,

(iii) the transconductance gain of VDTA which can vary via bias current, therefore providing the electronic tunability to designed filter.

3. Operational Simulation Using VDTA

The operational simulation method takes a different approach from topological simulation or wave active method, as it simulates the operation of ladder rather than its component [23]. The circuit equations and voltage-current relationship of each element are written using KVL and KCL. Then these equations are represented by block diagrams or signal flow graph. Each block represents some analog operation such as summation, integration, and subtraction. The final circuit is obtained by properly combining these blocks.

To explain the above statement, a fourth-order low pass Butterworth filter of Figure 3 has been taken as a prototype. The transfer function of this prototype filter can be expressed as

$$\frac{V_o}{V_{\text{in}}} = \frac{R_L}{s^4 C_1 C_2 L_1 L_2 R_L + s^3 \left(C_1 L_1 L_2 + C_1 C_2 L_2 R_s R_L\right) + s^2 \left(L_1 C_1 R_L + L_1 C_2 R_L + L_2 C_2 R_L + L_2 C_1 R_s\right) + s\left(R_s R_L C_1 + R_s R_L C_2 + L_1 + L_2\right) + \left(R_s + R_L\right)}. \tag{2}$$

To develop operational simulation in a systematic manner, consider the general ladder of Figure 4, where the series branch elements are labelled by admittance Y_i and the shunt branch elements are labelled by impedance Z_i. The ladder of Figure 4 can be described by the voltage and current equation as in (3a), (3b), (3c), and (3d) as follows:

$$I_1 = Y_1 \left(V_{\text{in}} - V_2\right), \tag{3a}$$

$$V_2 = Z_1 \left(I_1 - I_3\right), \tag{3b}$$

$$I_3 = Y_2 \left(V_2 - V_o\right), \tag{3c}$$

$$V_o = Z_2 \left(I_3 - I_5\right);$$

$$\text{assume } I_5 = 0; \tag{3d}$$

$$\text{then } V_o = Z_2 I_3,$$

where

$$Y_1 = \frac{1}{R_s + sL_1},$$

$$Y_2 = \frac{1}{sL_2},$$

$$Z_1 = \frac{1}{sC_1},$$

$$Z_2 = \frac{1}{sC_2 + 1/R_L}. \tag{4}$$

Both voltage and current terms are present in (3a), (3b), (3c), and (3d). This problem can be easily resolved by scaling these equations by a resistor R_V.

$$R_V I_1 = R_V Y_1 \left(V_{\text{in}} - V_2\right) \Longrightarrow$$

$$V_{I1} = \frac{R_V}{R_s + sL_1} \left(V_{\text{in}} - V_2\right), \tag{5a}$$

$$V_2 = \frac{Z_1}{R_V} \left(R_V I_1 - R_V I_3\right) \Longrightarrow$$

$$V_2 = \frac{1}{sC_1 R_V} \left(V_{I1} - V_{I3}\right), \tag{5b}$$

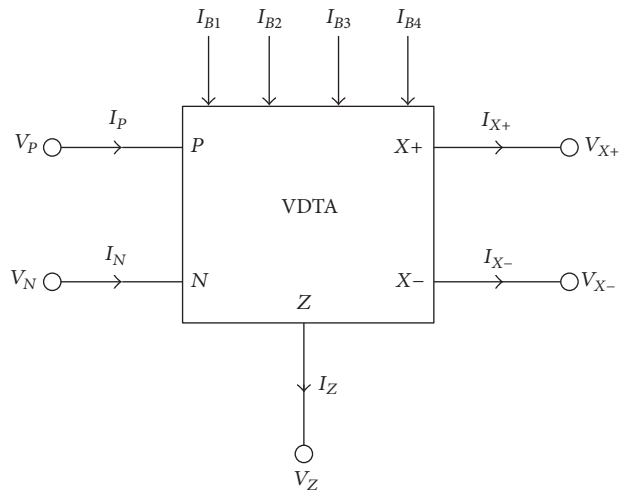

Figure 1: Symbolic representation of VDTA.

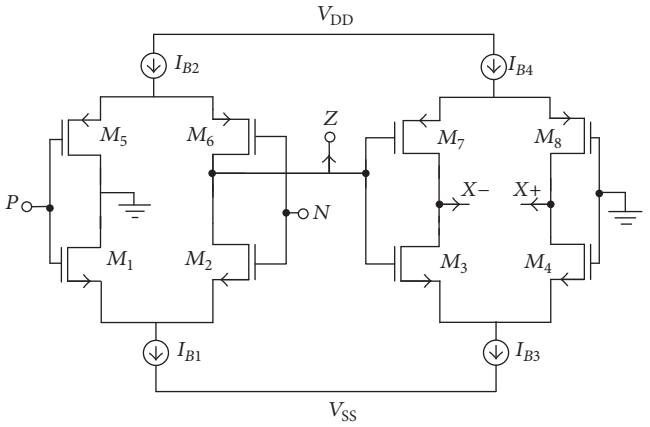

Figure 2: CMOS representation of VDTA.

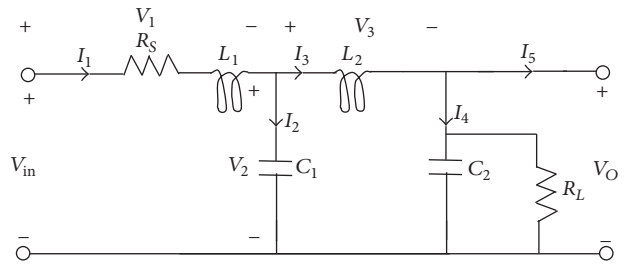

Figure 3: Fourth-order Butterworth low pass LC ladder.

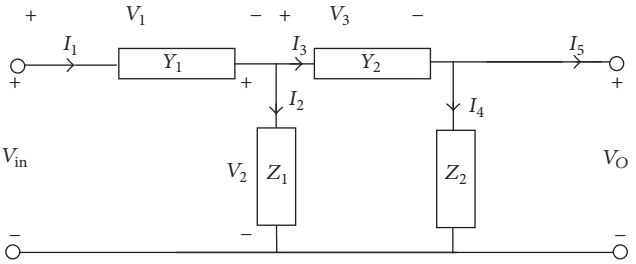

Figure 4: The ladder of Figure 3 with admittance in series arm and impedance in shunt arm.

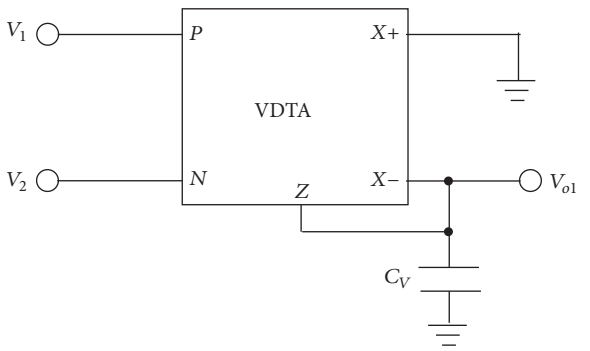

Figure 5: Lossy integrator using VDTA.

$$R_V I_3 = R_V Y_2 (V_2 - V_o) \Longrightarrow$$
$$V_{I3} = \frac{R_V}{sL_2}(V_2 - V_o), \tag{5c}$$

$$V_o = \frac{Z_2}{R_V} R_V I_3 \Longrightarrow$$
$$V_o = \frac{1}{sC_2 R_V + R_V/R_L} V_{I3}, \tag{5d}$$

where $V_{I1} = R_V I_1$; $V_{I3} = R_V I_3$.

The subscript I with voltages represents the fact that this voltage is derived from a current in the circuit.

Realization of (5a) to (5d) gives the operational simulation of prototype ladder filter of Figure 3. Implementation of (5a) and (5d) requires lossy integrator, while implementation of (5b) and (5c) requires lossless integrator. The lossy and lossless integrator can be easily realized using VDTA as discussed in the following section.

3.1. Lossy Integration. The implementation of lossy integration using VDTA is shown in Figure 5. The expression for output voltage of lossy integrator can be written as

$$V_{O1} = \frac{1}{1 + s\tau}(V_1 - V_2), \tag{6a}$$

where

$$\tau = \frac{C_V}{g_m} \quad (\text{with } g_{mi} = g_{mo} = g_m). \tag{6b}$$

3.2. Lossless Integrator. Lossless integrator can be implemented using VDTA as shown in Figure 6 and its output voltage expression is

$$V_{o2} = \frac{1}{s\tau}(V_1 - V_2). \tag{7a}$$

Again

$$\tau = \frac{C_V}{g_m} \quad (\text{with } g_{mi} = g_{mo} = g_m). \tag{7b}$$

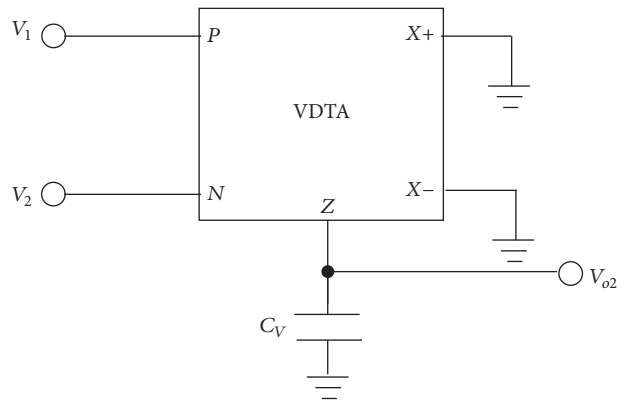

Figure 6: Lossless integrator using VDTA.

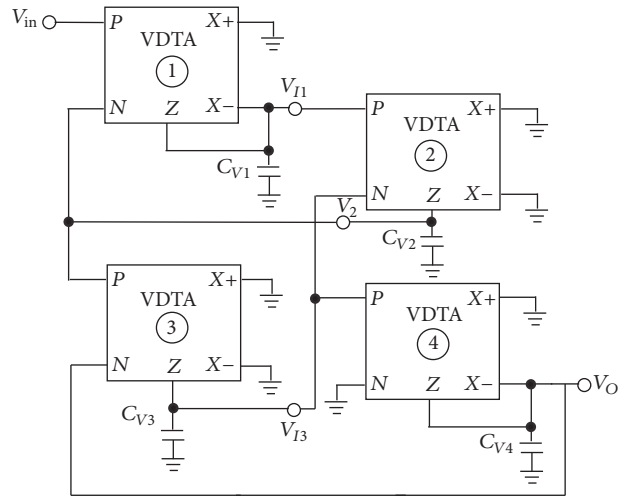

Figure 7: VDTA implementation of Figure 3 using operational simulation approach.

3.3. Complete Realization Using VDTA. With the help of lossy and lossless integrator of Figures 5 and 6, the complete realization of prototype 4th-order filter using operational simulation approach is shown in Figure 7.

The value of capacitor used in VDTA 1 and VDTA 4 can be calculated by comparing (6a) and (6b) with (5a) and (5d) as follows.

From (6a) and (6b) and (5a),

$$\frac{R_s}{R_V} = 1 \Longrightarrow \qquad (8)$$
$$R_s = R_V.$$

And $\tau = C_{V1}/g_m = L_1/R_V \Rightarrow C_{V1} = L_1 g_m/R_V$.

Take the value of scaling resistor

$$R_V = \frac{1}{g_m}. \qquad (9)$$

Then

$$C_{V1} = L_1 {g_m}^2. \qquad (10)$$

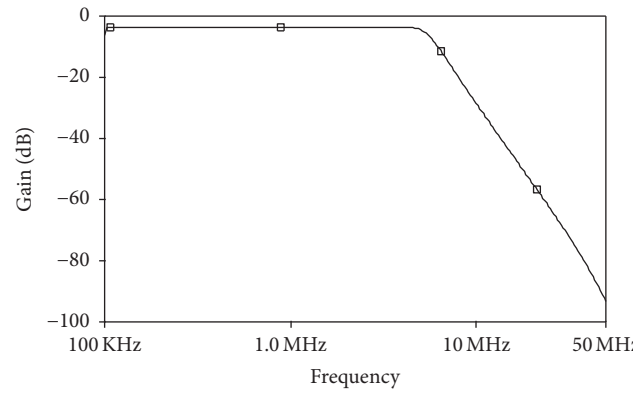

Figure 8: Simulated frequency response of 4th-order Butterworth low pass filter.

And from (6a) and (6b) and (5d)

$$\frac{R_V}{R_L} = 1 \Longrightarrow \qquad (11)$$
$$R_L = R_V,$$

$$\tau = \frac{C_{V4}}{g_m} = C_2 R_V \Longrightarrow \qquad (12)$$
$$C_{V4} = C_2.$$

Similarly, the value of capacitor used in VDTA 2 and VDTA 3 can be calculated by comparing (7a) and (7b) with (5b) and (5c) as follows.

From (7a) and (7b) and (5b),

$$\tau = \frac{C_{V2}}{g_m} = C_1 R_V \Longrightarrow \qquad (13)$$
$$C_{V2} = C_1.$$

And from (7a) and (7b) and (5c),

$$\tau = \frac{C_{V3}}{g_m} = \frac{L_2}{R_V} \Longrightarrow \qquad (14)$$
$$C_{V3} = L_2 {g_m}^2.$$

4. Simulation

The normalized component values of the prototype filter of Figure 3 are $R_s = 1$, $L_1 = .7654$, $C_1 = 1.8485$, $L_2 = 1.8485$, $C_2 = .7654$, and $R_L = 1$. The aspect ratio of various transistor used in CMOS implementation of VDTA is given in Table 1. The values of supply voltage and bias current for VDTA are $V_{DD} = V_{SS} = -0.9$ V and $I_{B1} = I_{B2} = I_{B3} = I_{B4} = 150\ \mu$A ($g_{mi} = g_{mo} = g_m = 627\ \mu$S), respectively.

For cut-off frequency of 5 MHz, the values of capacitor used in Figure 7 can be calculated by (10), (12), (13), and (14) as $C_{V1} = 15.28$ pF, $C_{V2} = 36.9$ pF, $C_{V3} = 36.9$ pF, and $C_{V4} = 15.28$ pF. Figure 8 shows the frequency response of the low pass fourth-order Butterworth filter. The simulated cut-off

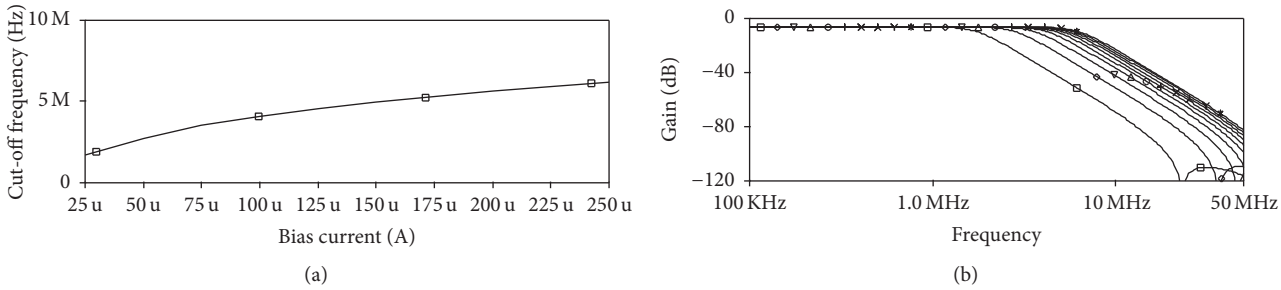

Figure 9: Electronic tuning demonstration. (a) Cut-off frequency variation with bias current. (b) Frequency response for various bias currents.

Table 1: Aspect ratio of various transistors used in CMOS implementation of VDTA.

Transistors	Aspect ratios (W (μm)/L (μm))
M_1–M_4	3.6/.36
M_5–M_8	16.64/.36

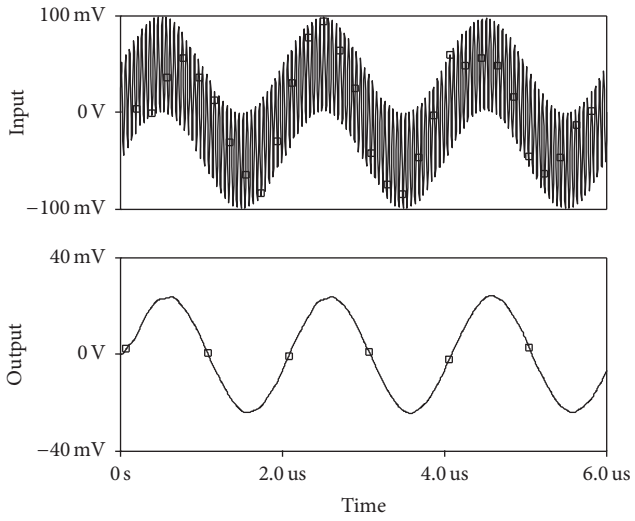

Figure 10: Transient response of input and output signals.

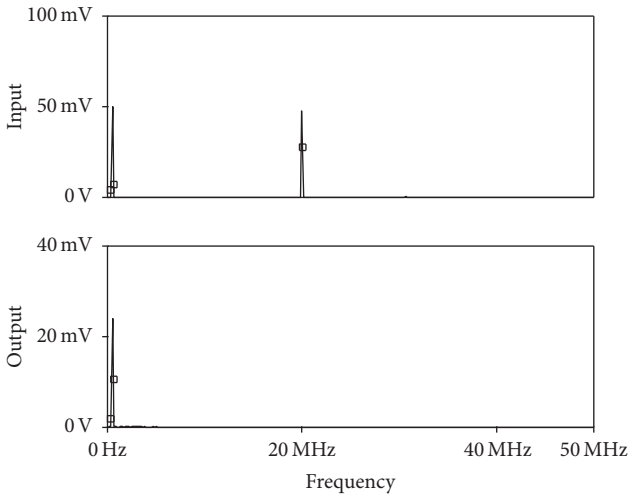

Figure 11: Frequency spectrum of input and output signals.

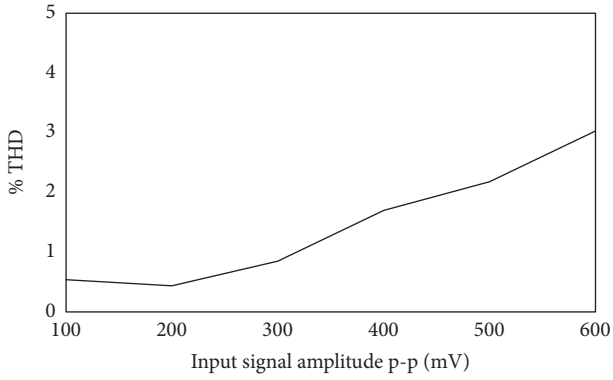

Figure 12: % THD variation with p-p input signal amplitude.

frequency is 4.99 MHz, which is very close to the theoretical cut-off frequency of 5 MHz. The electronic tunability of the filter through simulation is demonstrated in Figure 9 by varying bias current from 25 μA to 250 μA. Time domain analysis is studied by applying two signals of frequency 500 KHz and 20 MHz and of magnitude 50 mV at input. The transient response and its spectrum are shown in Figures 10 and 11, respectively. The proposed filter structure is also tested for total harmonic distortion at output and it is found that it is within acceptable limit of 3% up to 600 mV p-p signal of frequency 1 MHz as shown in Figure 12.

Noise analysis is also carried out for the proposed circuit by determining noise at output of the filter through simulation. The output noise variation within pass band frequencies is depicted in Figure 13 which shows that noise is in acceptable limit of nanovolt range. To examine effect of temperature variation on proposed filter circuit, the circuit is simulated at five different temperatures, 10°C, 25°C, 27°C, 50°C, and 100°C, and the results are depicted in Figure 14. The values of cut-off frequency for these temperatures are listed in Table 2. It is observed that cut-off frequency shifts towards lower frequencies as temperature decreases. This is due to the fact that the transconductance decreases with increases in temperature due to decrease in mobility. This shifting in cut-off frequency can be compensated through bias current

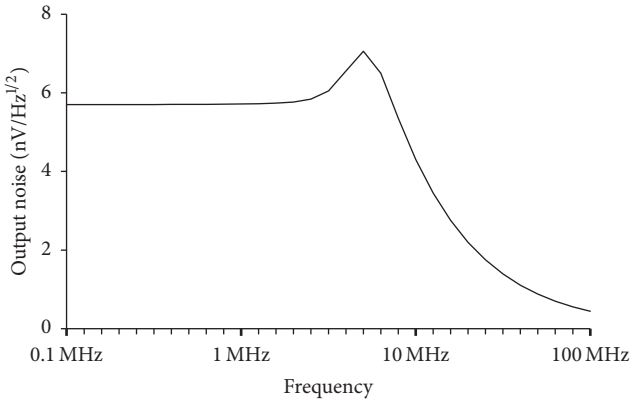

Figure 13: Output noise variation of proposed filter with frequency.

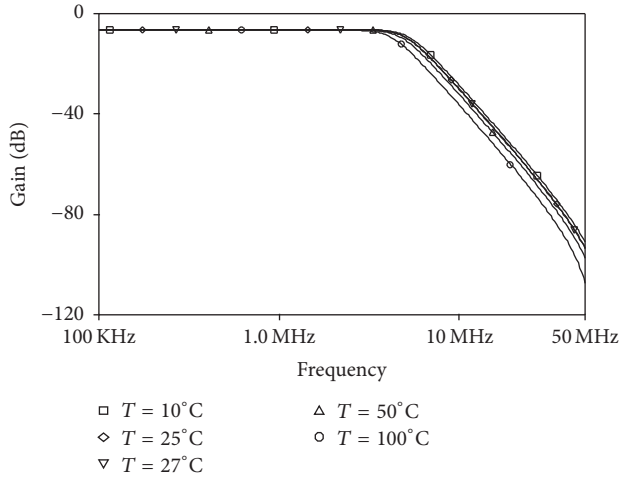

Figure 14: Demonstration of effect of temperature on proposed filter.

Table 2: Cut-off frequency at various temperatures.

Temperature	Cut-off frequency
10°C	5.2 MHz
25°C	5 MHz
27°C	4.98 MHz
50°C	4.7 MHz
100°C	4.17 MHz

variation from 104 μA (for f_0 = 4.17 MHz at 100°C) to 164 μA (for f_0 = 5.2 MHz at 10°C).

All the key parameters of the proposed filter structure are summarized in Table 3. The total power dissipated and output noise in simulation of the prototype filter are 2.16 mW and 5.7 $\times 10^{-9}$ V/Hz$^{1/2}$, while simulated values of these parameters for the VDTA implementation of the same-order filter using wave active method are 6.48 mW and 1.65 $\times 10^{-8}$ V/Hz$^{1/2}$ [20].

Experimental verification is carried out for proposed circuit through commercially available IC LM13700/NS. The

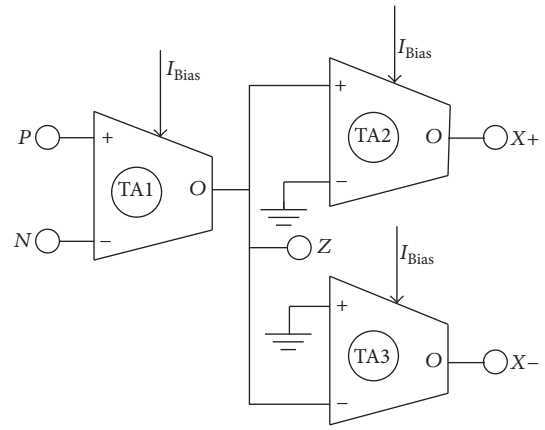

Figure 15: VDTA implantation using OTA.

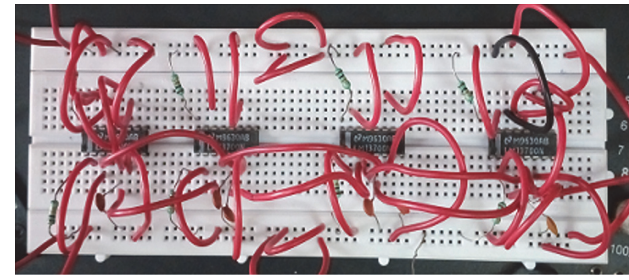

Figure 16: Bread-boarded circuit of Figure 7.

Table 3: Key parameters of simulated 4th-order low pass ladder filter.

Bias current	150 μA
VDTA transconductance, g_m	627 μS at bias current of 150 μA
Theoretical cut-off frequency	5 MHz
Simulated cut-off frequency	4.99 MHz
Roll-off rate	80 dB/decade
Total power consumption	2.16 mW
Total output noise voltage	5.7 nV/Hz$^{1/2}$
% THD	<3% for input signal up to 600 mV p-p

VDTA implementation using IC LM13700/NS is shown in Figure 15. The circuit of Figure 7 is bread-boarded as shown in Figure 16 for experimental testing. Supply voltage of ±15 V is used. The bias current of 1.35 mA is set to obtain the transconductance of 24.89 mA/V. The capacitor values are selected as $C_{v1} = C_{v4}$ = 10 nF and $C_{v2} = C_{v3}$ = 25 nF for cut-off frequency of 303 kHz. The measured magnitude response along with simulated response is depicted in Figure 17. The experimental cut-off frequency is observed to be 292 kHz.

5. Conclusion

The paper presents a systematic methodology for active implementation of operational simulation of LC ladder filter. To explain the outlined approach, a 4th-order Butterworth

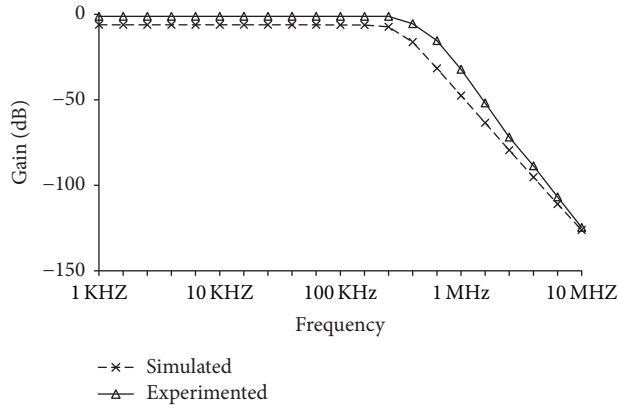

Figure 17: Simulated and experimented magnitude response of 4th-order low pass filter.

filter is taken as prototype, and, for active implementation, VDTA is used as an analog building block. The proposed implementation is resistorless and uses only grounded capacitors, which is suitable for IC implementation. The proposed structure also possesses electronic tunability of cut-off frequency. Workability of the proposed implementation is verified through PSPICE simulation using 180 nm TSMC technology parameters. The functionality of proposed LC ladder is also verified experimentally through IC LM13700/NS.

Competing Interests

The authors declare that they have no competing interests.

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