Hindawi
Active and Passive Electronic Components
Volume 2017, Article ID 9685685, 7 pages
https://doi.org/10.1155/2017/9685685

Research Article

Total Ionizing Dose Effects of Si Vertical Diffused MOSFET with SiO_2 and Si_3N_4/SiO_2 Gate Dielectrics

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Received 19 June 2017; Accepted 6 September 2017; Published 15 October 2017

Academic Editor: Gerard Ghibaudo

The total ionizing dose irradiation effects are investigated in Si vertical diffused MOSFETs (VDMOSs) with different gate dielectrics including single SiO_2 layer and double Si_3N_4/SiO_2 layer. Radiation-induced holes trapping is greater for single SiO_2 layer than for double Si_3N_4/SiO_2 layer. Dielectric oxidation temperature dependent TID effects are also studied. Holes trapping induced negative threshold voltage shift is smaller for SiO_2 at lower oxidation temperature. Gate bias during irradiation leads to different V_{TH} shift for different gate dielectrics. Single SiO_2 layer shows the worst negative V_{TH} at $V_G = 0$ V, while double Si_3N_4/SiO_2 shows negative V_{TH} shift at $V_G = -5$ V, positive V_{TH} shift at $V_G = 10$ V, and negligible V_{TH} shift at $V_G = 0$ V.

1. Introduction

Silicon power MOSFET, especially vertical diffused MOSFET (VDMOS), is widely used for high power application due to its mature technology and cost efficiency. Nowadays, VDMOS is often used under harsh environment such as space, where it suffers from cosmic radiation [1–4]. To operate normally in space environment, Si VDMOSs must be able to withstand ionizing radiation such as total ionizing dose (TID). In this paper, we investigate TID effects in Si VDMOS with different gate dielectrics including single SiO_2 layer and double Si_3N_4/SiO_2 layer, different oxidation temperatures of SiO_2, and different gate bias during irradiation.

2. Experiment Set-Up

The Si VDMOSs considered here are devices with well-known standard fabrication process except the gate dielectric deposition condition. Different silicon dioxide deposition conditions are carried out including different oxidation temperature from 800°C to 1000°C and with and without postoxidation annealing. In particular, double gate dielectric layer Si_3N_4/SiO_2, having the same total thickness 50 nm (20 nm/30 nm) as that of single SiO_2 layer, is fabricated to evaluate its hardness towards TID.

The irradiation test is performed with unpackaged devices wire-bonded on the test board under Co^{60} gamma source at a dose rate of 50 rad (Si)/s at room temperature, and the devices are remeasured after a total dose of 100 Krad is reached after 33 minutes. Irradiation was performed with different gate voltages (V_G) of 10 V, 0 V, and −5 V, with source terminal grounded and drain terminal of small voltage to guarantee a small current of about 100 mA for $V_G = 10$ V and drain terminal of 200 V (rated breakdown voltage). The bias-stress-only test is also performed without irradiation to account for the electrical stress influence, such as V_{TH}, g_m. The bias-stress test is carried out by using the same biases (V_G of 10 V, 0 V, and −5 V) and time (33 minutes) comparable to those used in the irradiation experiments. Current-voltage characteristics are measured using Agilent 2902A parameter analyzer, and the measurements are carried out before and right after the irradiation/bias-stress.

3. Results and Discussion

Figure 1 shows I_D versus V_G characteristics of Si VDMOS with different gate dielectrics and different oxidation conditions

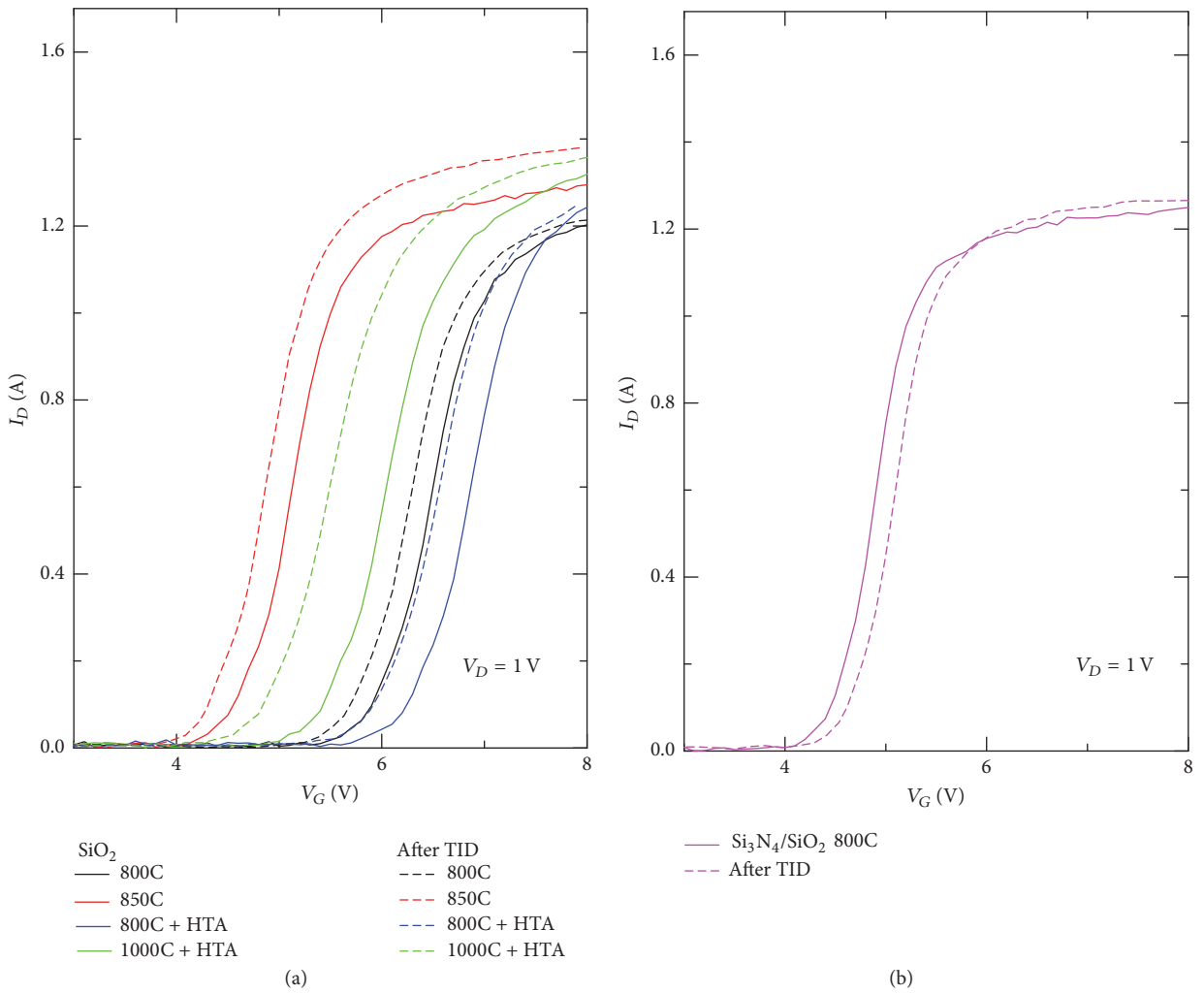

FIGURE 1: I_D-V_G characteristics of Si VDMOS with different gate dielectrics and different oxidation conditions before and after TID irradiation with V_G = 10 V (solid: before TID; open: after TID).

before and after TID irradiation with V_G = 10 V during irradiation. Two types of gate dielectrics with the same total thickness of 50 nm are investigated including normal SiO_2 layer (Figure 1(a)) and double Si_3N_4/SiO_2 layer (Figure 1(b)), which is claimed to be more TID tolerant [5–9]. It can be observed that the threshold voltage V_{TH} shifts negatively for single SiO_2 layer indicating a net holes' trapping during positive-bias irradiation, and ΔV_{TH} increases from 0.2 V to 0.71 with rising oxidation temperature from 800°C to 1000°C. The high temperature annealing (HTA) step after oxidation adds to the negative shift, suggesting a higher hole trapping ability. However, for double Si_3N_4/SiO_2 layer, V_{TH} shifts positively at V_G = 10 V with a smaller ΔV_{TH} = 0.14 V than that of SiO_2. It can be explained that, at positive-bias irradiation with V_G = 10 V, as shown in Figure 5(a), the irradiation created electrons in the SiO_2 layer are swept to the Si_3N_4 and trapped there, forming net electrons trapping by compensating with the irradiation created holes in Si_3N_4 [10–12]. The number of electrons trapped in the Si_3N_4 is higher than the holes trapped in the SiO_2, resulting in a net positive V_{TH} shift.

Figure 2 shows g_m versus V_G characteristics of Si VDMOS with different gate dielectrics and different oxidation conditions before and after TID irradiation with V_G = 10 V during irradiation. It can be observed that the devices with both single SiO_2 dielectrics and double Si_3N_4/SiO_2 dielectric (Figures 2(a) and 2(b)) have about the same g_m value both before and after a total dose of 100 Krad (Si), indicating excellent gate control. The device with double Si_3N_4/SiO_2 dielectric (Figure 2(b)) shows higher g_m of 1.6 S compared to that of single SiO_2 layer (1.3~1.4 S) at V_D = 1 V, which is due to a higher effective gate capacitance. The capacitance of Si_3N_4/SiO_2 gate dielectric is measured to have a gate capacitance of 1.6×10^{-9} F, while SiO_2 gate dielectric has a gate capacitance of 1.1×10^{-9} F due to a higher dielectric constant of Si_3N_4 with the same total thickness.

To exclude the electrical stress response from the bias irradiation test, the bias-induced degradation was separately

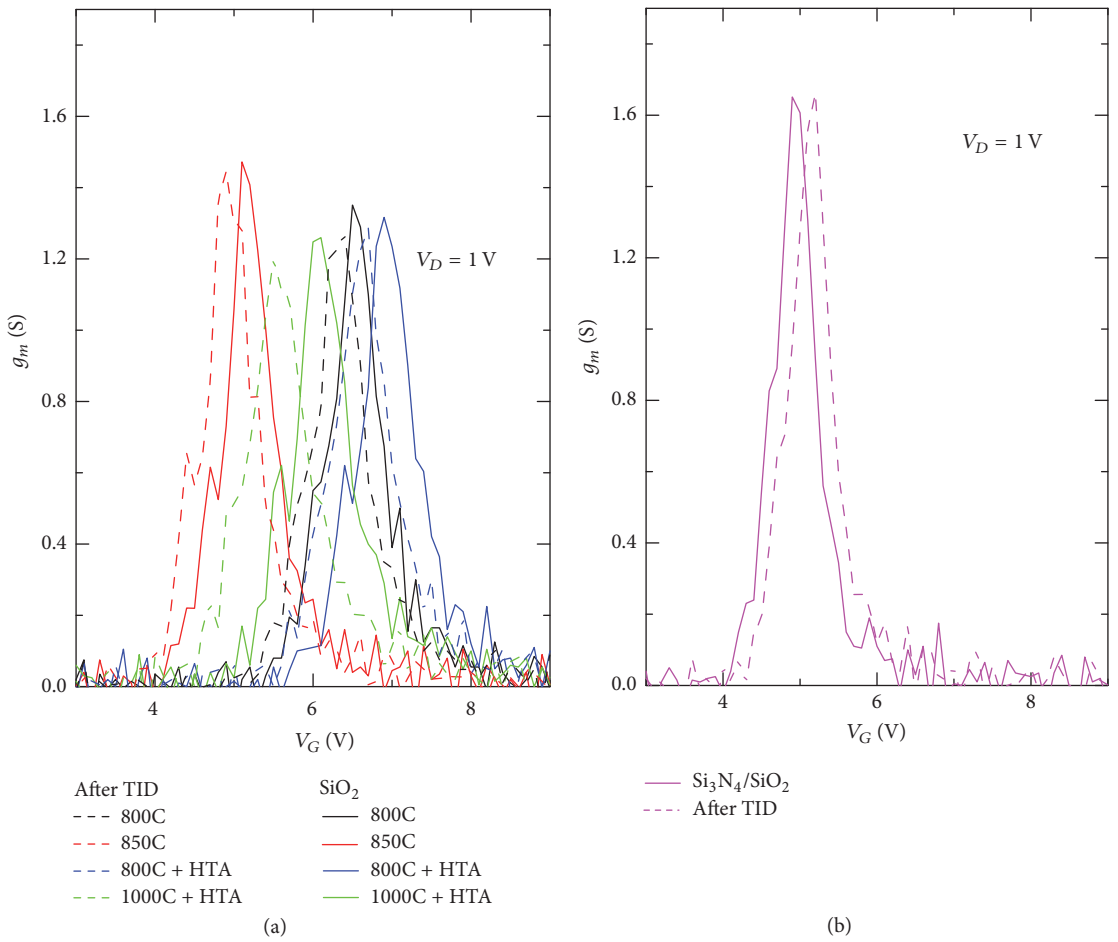

FIGURE 2: g_m-V_G characteristics of Si VDMOS with different gate dielectrics and different oxidation conditions before and after TID irradiation with V_G = 10 V (solid line: before irradiation; dashed line: after TID irradiation).

measured at biases and times compared to those used during irradiation. The results show that the electrical stress has trivial influence (<5%) on V_{TH} compared with the TID bias irradiation effects.

Figure 3(a) shows ΔV_{TH} of different gate dielectrics at different gate biases during irradiation including $V_G = -5$ V, $V_G = 0$ V, and $V_G = 10$ V. It can be observed that, for single gate dielectric SiO_2 with different oxidation conditions, V_{TH} shifts all negatively, and the SiO_2 layer fabricated at lower temperature presents a smaller V_{TH} shift at all gate biases during irradiation. It can also be observed that the threshold voltage V_{TH} shifts the most at irradiation bias of $V_G = 0$ V for single SiO_2 gate dielectric. It can be explained that, at $V_G = 0$ V, the irradiation created holes are freely dangling around in SiO_2, which are more easily trapped in the SiO_2, forming positive trapped charges, leading to negative V_{TH} shift. For irradiation bias of $V_G = -5$ V, there are similar chances that irradiation created holes can be trapped in the SiO_2, while, simultaneously, irradiation created electrons are swept to the SiO_2/semiconductor interface, forming more interface defects than in the case of irradiation bias of $V_G = 0$ V, which can be confirmed by calculating, respectively, the V_{ot} and V_{it} values by subthreshold midgap technique (SMGT) [12, 13], as is shown in Figure 3(b).

In an ideal device, the drain current and gate voltage are related by $I_D \sim \exp(V_G)$ in subthreshold regime. When plotted as $\log(I_D)$ versus V_G, the straight I-V characteristic can be extrapolated to a calculated midgap current. Comparing the preirradiation and postirradiation characteristics, the midgap voltage shift, ΔV_{mg}, as well as the change in subthreshold swing (inverse slope), ΔS, can be determined. The value of ΔV_{mg} is equivalent to ΔV_{ot} and ΔS is proportional to ΔV_{it}. The subthreshold charge separation technique has proven to be the easiest to perform and is the most widely used. The value of ΔV_{ot} is obtained from ΔV_{mg} assuming the following relation:

$$\Delta V_{ot} = \Delta V_{mg} = \frac{q\Delta N_{ot}}{C_{ox}}, \quad (1)$$

where

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}. \quad (2)$$

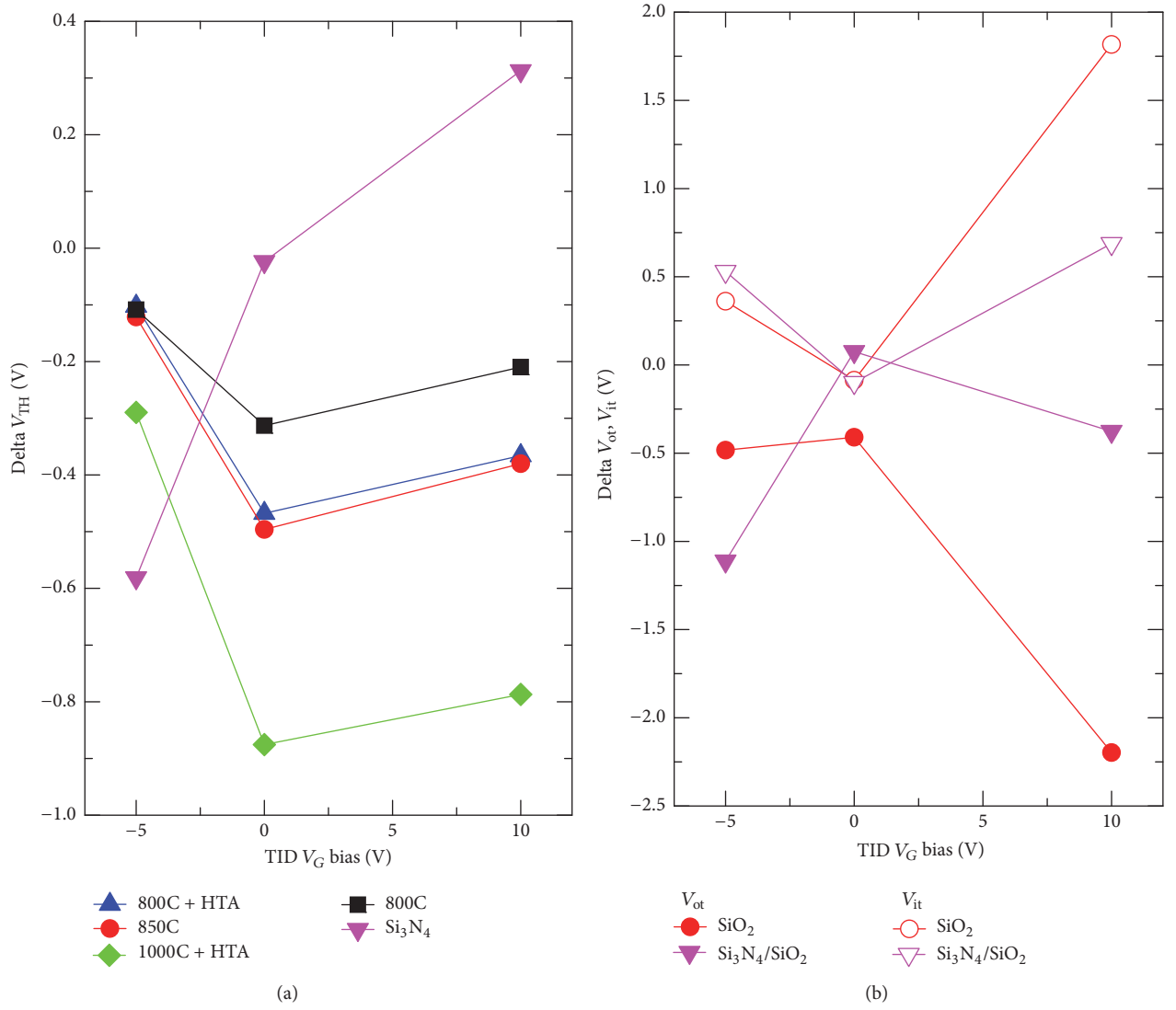

FIGURE 3: (a) ΔV_{TH} of Si VDMOS with different gate dielectrics after different TID bias irradiation; (b) ΔV_{ot} and ΔV_{it} characteristics of Si VDMOS with both single SiO_2 and double Si_3N_4/SiO_2 gate dielectrics after different TID bias irradiation.

The difference between the pre- and postirradiation subthreshold swings, ΔS, is calculated by the following relations:

$$\Delta S = \frac{kT}{q} \ln 10 \frac{\Delta C_{it}}{C_{ox}}$$

$$\Delta V_{it} = \frac{q\emptyset_B}{kT \ln 10} \Delta S \tag{3}$$

$$\Delta N_{it} = \frac{\Delta S C_{ox} \emptyset_B}{kT \ln 10},$$

where C_{it} stands for the interface trap induced capacitance, k is the Boltzmann constant, T is the temperature, and the Fermi potential $\emptyset_B$ can be calculated as follows:

$$\emptyset_B = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right). \tag{4}$$

Figure 3(b) shows ΔV_{ot} and ΔV_{it} calculated by SMGT method using (1) to (4) of both single gate dielectric SiO_2 and double gate dielectric Si_3N_4/SiO_2 at different gate bias including $V_G = -5$ V, $V_G = 0$ V, and $V_G = 10$ V. It can be observed that, for single SiO_2 dielectric, V_{ot} are similar in both $V_G = -5$ V and $V_G = 0$ V, while V_{it} is larger in $V_G = -5$ V than in $V_G = 0$ V, resulting in a compensation of V_{TH} effects.

The V_{TH} shifts negatively at all bias irradiation cases for single SiO_2 gate dielectric layer; for double gate dielectric Si_3N_4/SiO_2, however, V_{TH} shifts negatively in $V_G = -5$ V, and V_{TH} shifts positively in $V_G = 10$ V and barely shifts in $V_G = 0$ V. By calculating V_{ot} and V_{it}, respectively, it can be observed that, at $V_G = -5$ V, more holes are swept towards/to the Si_3N_4 layer, where they can be more easily trapped compared to SiO_2 [5]. For $V_G = 10$ V, irradiation created electrons are trapped in Si_3N_4, forming negative trapped charges, leading to positive V_{TH} shift.

Under bias irradiation, electron/hole pairs are being generated in a MOSFET. At $V_G = 0$ V, electrons/holes get more chances to recombine at first, forming less trapped holes

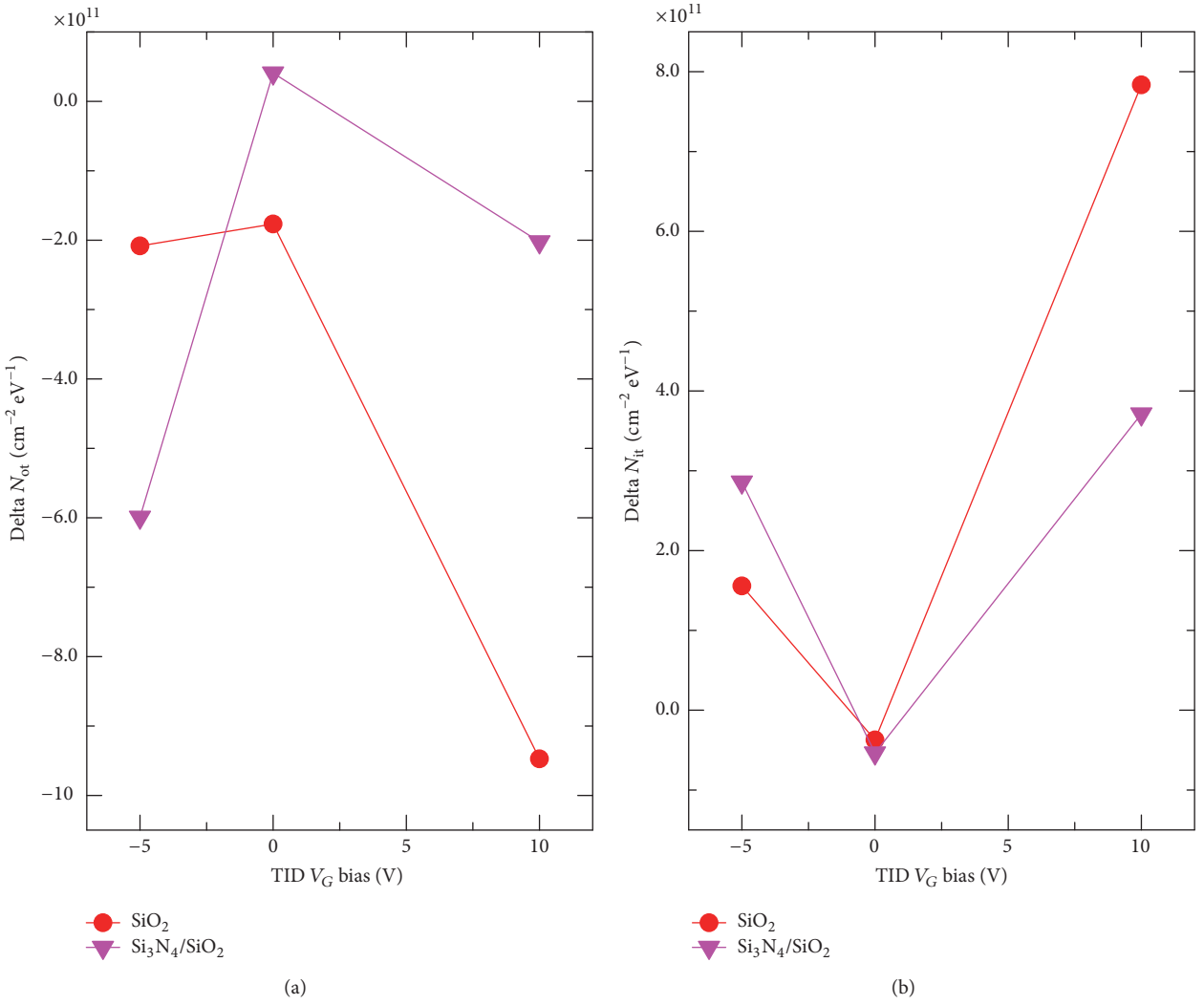

FIGURE 4: (a) ΔN_{ot} and (b) ΔN_{it} characteristics of Si VDMOS with both single SiO_2 and double Si_3N_4/SiO_2 gate dielectrics after different TID bias irradiation.

and interface defects. At $V_G = -5$ V or $V_G = 10$ V, less electrons/holes recombine at higher electric field, leading to more trapped holes and interface defects, as illustrated in Figure 4.

Figures 4(a) and 4(b) show the calculated ΔN_{ot} and ΔN_{it} values of both single gate dielectric SiO_2 and double gate dielectric Si_3N_4/SiO_2 at different gate bias including $V_G = -5$ V, $V_G = 0$ V, and $V_G = 10$ V. It can be observed that, at $V_G = 0$ V, single gate dielectric SiO_2 and double gate dielectric Si_3N_4/SiO_2 show similar value of N_{it}, indicating similar SiO_2/semiconductor interface, which is logical due to the same oxidation condition. With increasing absolute gate bias $|V_G|$, more interface defects are created for both dielectrics.

For single gate dielectric SiO_2, the oxide trapped charges N_{ot} increase with the absolute electric field $|E|$, with the least oxide trapped charges at $V_G = 0$ V due to recombination of more holes/electrons at the beginning. For double gate dielectric Si_3N_4/SiO_2, there are more net oxide trapped charges at $V_G = -5$ V than at $V_G = 10$ V, which can be explained as follows.

Under positive-bias irradiation, the charges in the SiO_2 are mostly due to holes trapping at the oxide/silicon interface. In contrast to this, the negative charges due to the electrons from the oxide layer and the positive charges due to the holes from the nitride compete to determine both the magnitude and the sign of the charges in the Si_3N_4, as illustrated in Figure 5(a). The electrons generated in the oxide layer are swept to the nitride layer easily because no electron barrier exists at the Si_3N_4/SiO_2 interface. The total number of holes generated in the oxide and escaping initial recombination is assumed to be approximately proportional to the oxide thickness, which is consistent with what is observed in Figure 4(a) with more N_{ot} in single SiO_2 layer than in double Si_3N_4/SiO_2 layer at $V_G = 10$ V.

For negative bias irradiation, Si_3N_4/SiO_2 shows negative V_{TH} shift, larger in magnitude than that for positive-bias irradiation. This occurs because the nitride/oxide interface

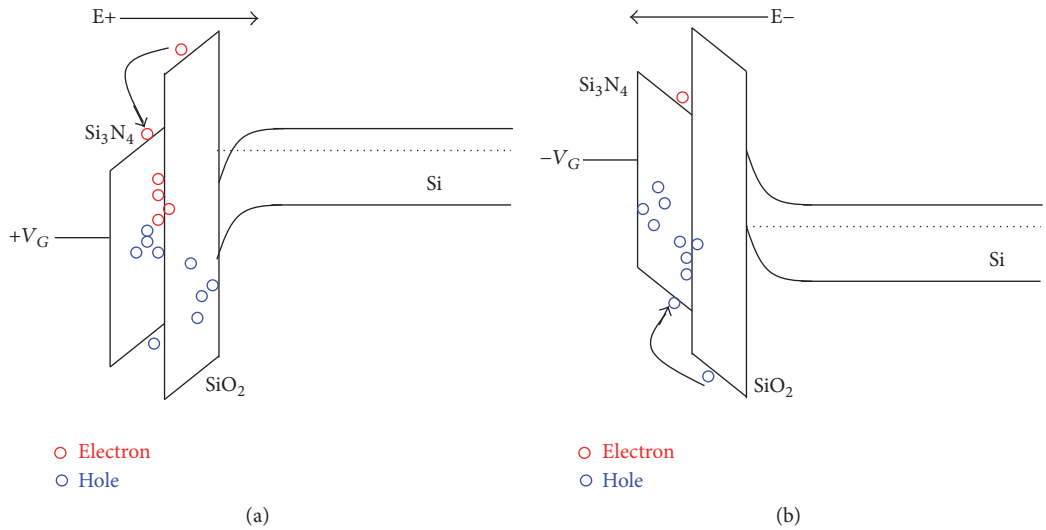

Figure 5: Schematic illustration of charge trapping during biased irradiation at both (a) positive and (b) negative gate biases.

has more trapped holes than trapped electrons due to the holes moving from the SiO_2 without hole barrier at the interface, as illustrated in Figure 5(b). Also, some of the holes generated in the oxide are trapped in the oxide. Due to the net trapping of holes in both the oxide and nitride, there is addition of charges for the negative bias case [10–13].

4. Conclusions

The gate dielectric effects and gate bias dependence of TID effects on Si VDMOS have been evaluated. Single gate dielectric SiO_2 presents negative V_{TH} shift at either positive or negative gate bias, which improves with lower oxidation temperature. Double gate dielectric Si_3N_4/SiO_2 shows negative V_{TH} shift at negative gate bias due to net holes trapping in Si_3N_4/SiO_2 and positive V_{TH} shift at positive gate bias due to net electron trapping.

These results provide insight into the mechanisms and magnitude of the TID responses of Si VDMOS with SiO_2 and Si_3N_4/SiO_2 gate insulators, and Si_3N_4/SiO_2 is proved to be more TID tolerant.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Authors' Contributions

Author Min Zhou has been added as coauthor and corresponding author with all authors' agreement. Dr. Min Zhou helps with the paper revision including paper writing and deep analysis about the microstructure of the defects responsible for trapping.

Acknowledgments

The research is supported by the National Natural Science Foundation of China (Grant 61604128), the Scientific Research Fund of Zhejiang Provincial Education Department (Grant Y201533913), and the Fundamental Research Funds for the Central Universities (Grant 2016QNA4025).

References

[1] J.-M. Lauenstein, A. D. Topper, M. C. Casey et al., "Recent radiation test results for power MOSFETs," in *Proceedings of the 2013 IEEE Radiation Effects Data Workshop, REDW 2013 - Held in Conjunction with the 50th IEEE Nuclear and Space Radiation Effects Conference, NSREC 2013*, San Francisco, CA, USA, July 2013.

[2] M. V. O'Bryan, D. Chen, M. J. Campola et al., "Recent single event effects compendium of candidate electronics for NASA space systems," in *Proceedings of the IEEE NSREC11 Data Workshop*, San Francisco, CA, USA, 2011.

[3] M. Hartwell, K. Ryan, S. Netherton, P. Milliken, and D. Kerwin, "Total ionizing dose testing of a RadHard-by-Design FET driver in a 0.35μm triple-well process," in *Proceedings of the 2006 IEEE Radiation Effects Data Workshop, NSREC*, pp. 94–100, Ponte Vedra, FL, USA, July 2006.

[4] K. Shenai, K. F. Galloway, and R. D. Schrimpf, "The effects of space radiation exposure on power MOSFETS: A review," *International Journal of High Speed Electronics and Systems*, vol. 14, no. 2, pp. 445–463, 2004.

[5] K. Watanabe, M. Kato, T. Okabe, and M. Nagata, "Radiation effects of double layer dielectric films," *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, pp. 1216–1222, 1986.

[6] C. D. Cress, J. J. McMorrow, J. T. Robinson et al., "Total ionizing dose-hardened carbon nanotube thin-film transistors with silicon oxynitride gate dielectrics," *MRS Communications*, vol. 1, no. 1, pp. 27–31, 2011.

[7] A. G. Stanley, "Comparison of MOS and metal-nitride-semiconductor insulated gate field-effect transistors under electron irradiation," *IEEE Transactions on Nuclear Science*, vol. NS-13, no. 6, pp. 248–254, 1966.

[8] D. Neamen, W. Shedd, and B. Buchanan, "Thin film silicon on silicon nitride for radiation hardened dielectric ally isolated misfet's," *IEEE Transactions on Nuclear Science*, vol. 22, no. 6, pp. 2203–2207, 1975.

[9] R. D. Schrimpf, D. M. Fleetwood, M. L. Alles, R. A. Reed, G. Lucovsky, and S. T. Pantelides, "Radiation effects in new materials for nano-devices," *Microelectronic Engineering*, vol. 88, no. 7, pp. 1259–1264, 2011.

[10] W.-C. Hsieh, H.-T. D. Lee, F.-C. Jong, and S.-C. Wu, "Charge retention improvement of nonvolatile radiation sensor using metal-oxide-nitride-oxide-silicon with Si-rich nitride and oxynitride as stack charge-trapping layer," *Sensors and Materials*, vol. 28, no. 9, pp. 1023–1033, 2016.

[11] J. R. Cricchi and D. F. Barbe, "Compensation of radiation effects by charge transport in metal-nitride-oxide-semiconductor structures," *Applied Physics Letters*, vol. 19, no. 3, pp. 49–51, 1971.

[12] V. A. K. Raparla, S. C. Lee, R. D. Schrimpf, D. M. Fleetwood, and K. F. Galloway, "A model of radiation effects in nitride-oxide films for power MOSFET applications," *Solid-State Electronics*, vol. 47, no. 5, pp. 775–783, 2003.

[13] N. A. Hastas, D. H. Tassis, C. A. Dimitriadis, and G. Kamarinos, "Determination of interface and bulk traps in the subthreshold region of polycrystalline silicon thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1991–1994, 2003.