Hindawi
Active and Passive Electronic Components
Volume 2017, Article ID 9703029, 10 pages
https://doi.org/10.1155/2017/9703029

Research Article

Investigation and Analysis of the Simultaneous Switching Noise in Power Distribution Network with Multi-Power Supplies of High Speed CMOS Circuits

Khaoula Ait Belaid,[1] Hassan Belahrach,[1,2] and Hassan Ayad[1]

[1]*Laboratory of Electrical Systems and Telecommunications, Department of Physics, Faculty of Sciences and Technology, Cadi Ayyad University, Marrakesh, Morocco*
[2]*Department of Electrical Engineering, Royal Air Academy (ERA), Marrakesh, Morocco*

Correspondence should be addressed to Khaoula Ait Belaid; aitbelaid.khaoula@gmail.com

Received 9 June 2017; Accepted 17 August 2017; Published 28 September 2017

Academic Editor: Gerard Ghibaudo

The paper studies a simultaneous switching noise (SSN) in a power distribution network (PDN) with dual supply voltages and two cores. This is achieved by reducing the admittance matrix Y of the PDN then calculating frequency domain impedance with rational function approximation using vector fitting. This paper presents a method of computing the simultaneous switching noise through a switching current, whose properties and details are described. Thus, the results are discussed and performed using MATLAB and PSpice tools. It demonstrated that the presence of many cores in the same PCB influences the SSN due to electromagnetic coupling.

1. Introduction

At present, there is an ever-greater integration in electronic circuits resulting from grouping in the same card the complex chips with different natures [1]. These electronic circuits are submitted to important electromagnetic disturbances. The majority of these disturbances is the result of the miniaturization of the components, the increase in the performances, increasing the frequency, and decreasing the supply voltages. Therefore, it becomes necessary to take into account these disturbances to predict the behavior of integrated circuits.

The current and voltage of the power source are generally cumbersome. Indeed, they often cannot be directly connected to the transistors presented within the integrated circuits. Thus, the currents will have cross interconnections, the power plans, and the bondings wires before supplying the transistors. All these elements have resistance, pure inductance, and possibly a capacitance. The currents, crossing these elements, will create voltage fluctuations on arrival. This phenomenon is called simultaneous switching noise (SSN). The SSN is due to mutual inductive coupling and interconnections of power delivery networks (PDNs). So, to analyze the SSN, it is necessary to model the behavior of these inductive coupling and interconnections at high frequencies.

In relation to the topic, several papers have discussed the issue of modeling PDNs. Therefore, there are different modeling methods, such as a finite difference time domain (FDTD) method [2], transmission line method [3, 4], and the transmission matrix method. The transmission line method, in particular, uses transmission line with two-dimensional array or distributed RLCG elements in SPICE, in addition to the cavity resonator process simulated in SPICE tool [5, 6]. Yet it is essential to mention that the transmission matrix method is based on a modeling cascade of elementary cell circuits RLCG in the package and board [7] which is more effective for analyzing PDNs.

One of the most important criteria in the design of PDNs is to ensure safe energy to the circuits when a sudden power occurs. Indeed, the elimination of SSN in multilayer PCB is a critical task in the phase of the design to assure signal integrity. Several methods have been used to reduce the harmful effects of noise transmission, such as integrated capacitors, which are used at high frequencies because of their low inductance [8, 9]. Another method to remove noise is the

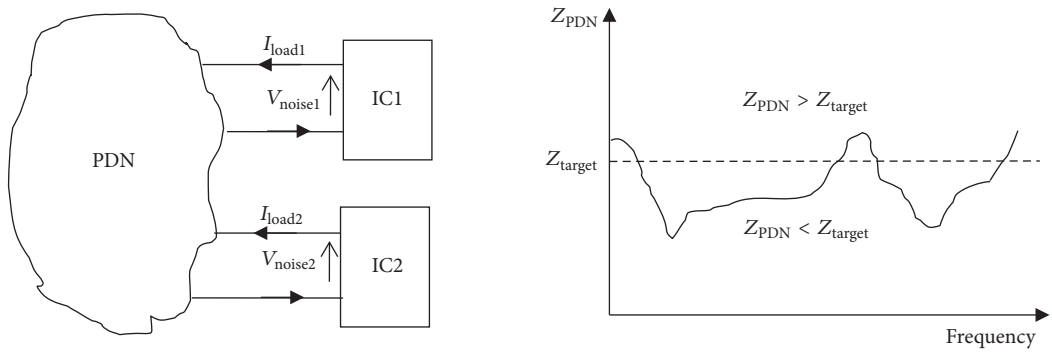

Figure 1: Example of PDN impedance versus frequency.

introduction of lossy components serving for the elimination of resonance based on the increase of the component loss [10]. Power islands are also used in the reduction of noise by isolating the components making noise on the power bus from sensitive devices [11].

In [12], there is a new method to model the simultaneous switching noise (SSN) for systems with a single integrated circuit. This method uses the rational function of the PDN impedance in the time domain based on measurements. Our work consists also of compute the SSN but for one system with two integrated circuits or cores. Since the objective is to analyze the coupling effects between them, our method uses firstly the rational function of the PDN impedance and then the principle of vector fitting (VF) to compute its parameters and finally the reduction of the PDN admittance matrix Y.

After the introduction, the second section presents the analysis of the approximation with a rational function. The third deals with a method of vector fitting. The fourth consists in the applications that analyze the effect of the presence of two cores. Finally, conclusions are drawn in the last part.

2. PDN Impedance Function in Time Domain

In general, the power distribution network (PDN) contains many networks of capacitors with several types and different values which allow obtaining the target impedance on the required frequency range of a PCB ground and power plans. So, the design of the PDN interconnections should carry its impedance $Z(j\omega)$ below the target impedance at high frequency [13]. In frequency domain, the example of PDN impedance as seen by the pads on the chip is illustrated by Figure 1.

The main objective in the design of the power distribution network is to provide the sufficient current for each transistor of the integrated circuit by ensuring that the power supply noise does not exceed the specified margin. Then, the target impedance Z_{target} can be defined as

$$Z_{target} = \frac{[(\text{Power supply voltage}) \cdot (\text{allowed ripple})]}{\text{Current}}. \quad (1)$$

In frequency domain, we can write

$$V_{noise} = Z_{PDN} \cdot I_{load}, \quad (2)$$

where (i) Z_{PDN} is the impedance of the PDN, (ii) I_{load} is the transient current, and (iii) V_{noise} is the voltage noise in the PDN.

The SSN waveform cannot be calculated directly with $Z_{PDN}(j\omega)$ because of the impedance function that cannot be extracted directly from the circuit model that contains power/ground planes and capacitors in time domain. Indeed, an impedance approximation with a rational function is necessary [12].

The impedance rational approximation in the frequency domain can be written [14] as

$$Z_{PDN}(s) \approx d + \sum_{n=1}^{N} \frac{r_n}{s - p_n}. \quad (3)$$

In (3), s represents the Laplace variable, p_n are the poles, and r_n are the residues, all of them can be either real or complex conjugate pairs. The term d is a real constant and N is the order of the approximation. Let us consider a weighting function $\sigma(s)$ defined as

$$\sigma(s) = \sum_{n=1}^{N} \frac{\overline{r}_n}{s - \overline{p}_n} + 1, \quad (4)$$

where $\overline{p}_n$ represent the poles of the function $\sigma(s)$ and $\overline{r}_n$ are the residues corresponding to $\overline{p}_n$.

By multiplying (4) with $Z_{PDN}(s)$ we import its rational approximation and we find

$$\sum_{n=1}^{N} \frac{r_n}{s - \overline{p}_n} + d \approx \left(\sum_{n=1}^{N} \frac{\overline{r}_n}{s - \overline{p}_n} + 1 \right) \cdot Z_{PDN}(s). \quad (5)$$

We note that $\sigma(s)$ has the same poles of $(\sigma(s) \cdot Z_{PDN}(s))$.

$Z_{PDN}(s)$ rational function approximation can be easily obtained from (5). So, we find

$$Z_{PDN}(s) = \frac{(\sigma Z_{PDN})_{fit}(s)}{\sigma_{fit}(s)} = \frac{\prod_{n=1}^{N+1}(s - z_n)}{\prod_{n=1}^{N}(s - \overline{z}_n)}, \quad (6)$$

where

$$(\sigma Z_{PDN})_{fit}(s) = \frac{\prod_{n=1}^{N+1}(s - z_n)}{\prod_{n=1}^{N}(s - \overline{p}_n)};$$
$$\sigma_{fit}(s) = \frac{\prod_{n=1}^{N}(s - \overline{z}_n)}{\prod_{n=1}^{N}(s - \overline{p}_n)}. \quad (7)$$

Equation (6) shows that the poles of $Z_{\mathrm{PDN}}(s)$ become the zeros of $\sigma_{\mathrm{fit}}(s)$. We observe that the starting poles are canceled in the process of division because the poles of $(\sigma Z_{\mathrm{PDN}})_{\mathrm{fit}}(s)$ are the same of $\sigma_{\mathrm{fit}}(s)$. In fact, it is enough to calculate the zeros of $\sigma_{\mathrm{fit}}(s)$ to obtain a good set of poles of $Z_{\mathrm{PDN}}(s)$ [14].

The calculation of the poles and the residues of the impedance rational approximation in the frequency domain can be achieved by the principle of vector fitting in two steps based on the starting poles. The first step involves the identification of the poles based on (5) which can be eventually written in this form:

$$\sum_{n=1}^{N} \frac{r_n}{s-\overline{p}_n} + d - \left(\sum_{n=1}^{N} \frac{\overline{r}_n}{s-\overline{p}_n} \right) Z_{\mathrm{PDN}}(s) \approx Z_{\mathrm{PDN}}(s). \quad (8)$$

Equation (8) can also be written for k frequency points as a linear problem:

$$[A] \cdot \{x\} = \{b\}, \quad (9)$$

where

$$[A] = \begin{bmatrix} \frac{1}{s_1-\overline{p}_1} & \cdots & \frac{1}{s_1-\overline{p}_N} & 1 & \frac{-Z_{\mathrm{PDN}}(s_1)}{s_1-\overline{p}_1} & \cdots & \frac{-Z_{\mathrm{PDN}}(s_1)}{s_1-\overline{p}_N} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \frac{1}{s_k-\overline{p}_1} & \cdots & \frac{1}{s_k-\overline{p}_N} & 1 & \frac{-Z_{\mathrm{PDN}}(s_k)}{s_k-\overline{p}_1} & \cdots & \frac{-Z_{\mathrm{PDN}}(s_k)}{s_k-\overline{p}_N} \end{bmatrix},$$
$$\{x\} = \left[r_1 \cdots r_N \; d \; \overline{r}_1 \cdots \overline{r}_N \right]^T, \quad (10)$$
$$\{b\} = \left[Z_{\mathrm{PDN}}(s_1) \cdots Z_{\mathrm{PDN}}(s_k) \right].$$

The vector fitting examined the problem of (8) by solving the problem of (9) using the least squares method and then passes to the calculation of the zeros by computing the eigenvalues of the matrix H:

$$[H] = [D] - \{c\} \{\overline{r}\}^T, \quad (11)$$

where $[D]$ is a diagonal matrix containing the starting poles, and $\{c\}$ is a column vector of ones, and $\{\overline{r}\}^T$ is a row-vector containing the residues of $\sigma(s)$.

The second phase of vector fitting consists of calculating the residues of $Z_{\mathrm{PDN}}(s)$ directly from (6).

The rational approximation with the vector fitting in frequency domain should respect several criteria such as passivity, causality, and stability. The passivity is satisfied when the eigenvalues of $\mathrm{Re}\{Z_{\mathrm{PDN}}(s)\}$ are strictly positive [15]. This leads to the optimization stage:

$$\Delta Z_{\mathrm{PDN}}(s) = \sum_{n=1}^{N} \Delta \frac{r_n}{s-p_n} + \Delta d \cong 0. \quad (12)$$

With

$$\mathrm{eig}\left(\mathrm{Re}\left\{ Z_{\mathrm{PDN}}(s) + \Delta d + \sum_{n=1}^{N} \frac{\Delta r_n}{s-p_n} \right\} \right) > 0. \quad (13)$$

The first part of (12) minimizes the variation in the impedance matrix elements, whereas the second imposes the criterion of passivity on the disturbed model [15]. The stability can be satisfied by controlling the rational approximation poles. The stability condition is, thus, equivalent to granting that the poles lie in the left-hand plane. Finally, the causality is satisfied when we reach $\mathrm{Re}(p_n) < 0$ [16].

After having respected these three criteria, $Z_{\mathrm{PDN}}(s)$ can be written in the frequency domain as

$$Z_{\mathrm{PDN}}(s) = d + \sum_{m=1}^{M} \frac{a_m}{s-b_m} + \sum_{n=1}^{N} \frac{2r_{nr}(s-p_{nr}) - 2r_{ni}p_{ni}}{(s-p_{nr})^2 + p_{ni}^2}, \quad (14)$$

where the N poles $(p_{nr} - jp_{ni},\ p_{nr} + jp_{ni})$ and their corresponding residues $(r_{nr} - jr_{ni},\ r_{nr} + jr_{ni})$ are complex conjugate pairs, and the M poles b_m and its corresponding residues a_m are real.

By performing the inverse Laplace transformation, the impedance in the time domain has the following form:

$$z_{\mathrm{PDN}}(t) = d\delta(t) + \sum_{m=1}^{M} a_m e^{b_m t} h(t) + 2 \sum_{n=1}^{N} \sqrt{(r_{nr}^2 + r_{ni}^2)} e^{p_{nr}t} \cos(p_{ni}t + \varphi) h(t), \quad (15)$$

where $\delta(t)$ is the Dirac impulsion, $h(t)$ is the unit step function, and $\varphi = ar\cos(r_{nr}/\sqrt{r_{nr}^2 + r_{ni}^2})$.

It is clear that the impedance function in the time domain can be easily obtained from the rational approximation in the frequency domain.

3. Simultaneous Switching Noise in Power Distribution Network

Once the impedance function in the time domain is determined from (2), the SSN waveform can be calculated as follows:

$$v_{\mathrm{noise}}(t) = \left[d\delta(t) + \sum_{m=1}^{M} a_m e^{b_m t} h(t) + 2 \sum_{n=1}^{N} \sqrt{(r_{nr}^2 + r_{ni}^2)} e^{p_{nr}t} \cos(p_{ni}t + \varphi) h(t) \right] * i_{\mathrm{load}}(t), \quad (16)$$

where $*$ denotes the convolution operation.

For digital signals at GHz, the pulse width of switching current is in the order of 0.1 ns, and the resonance period exceeds 1 ns for typical PDNs [12]. Thus, the current impulse can be seen like one with limited amplitude if the PDN

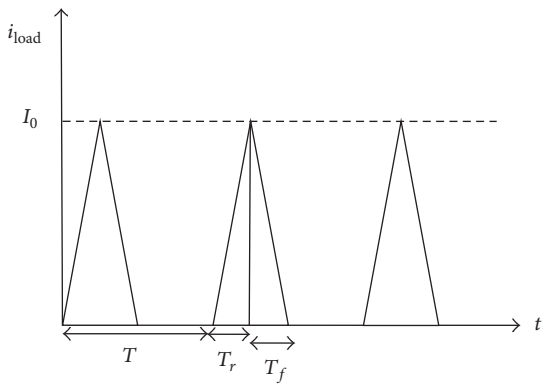

Figure 2: Switching current waveform.

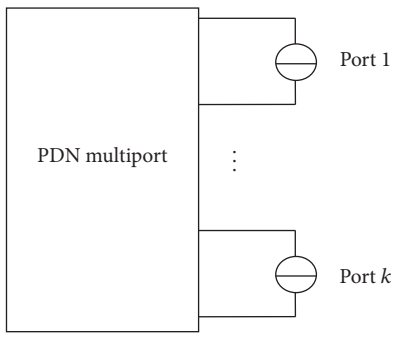

Figure 3: Example of PDN with multiport.

resonance period is very large compared to the impulse width of the current.

We assume that the switching current is a triangular periodic signal as indicated in Figure 2. The surface of the current impulse can be estimated by $S = I_0((T_r + T_f)/2)$; therefore it can be replaced by $i(t) = S\delta(t)$. The noise is periodic and it is given by the following formula:

$$v_{\text{noise}}(t) = d\sum_{l=0}^{\infty} i_{\text{load}}(t - lT) + S\sum_{l=0}^{\infty}\left[\sum_{m=1}^{M} a_m e^{b_m(t-lT)} + 2\sum_{n=1}^{N} e^{p_{nr}(t-lT)}\sqrt{\left(r_{nr}^2 + r_{ni}^2\right)}\cos\left(p_{ni}(t - lT) + \varphi\right)\right] \cdot h(t - lT). \quad (17)$$

In real circuit system, the PDN is a multiport system as represented in Figure 3.

So, the SSN of the qth port is calculated by

$$v_q(t) = \sum_{j=1}^{k} z_{qj}(t) * i_j(t), \quad (18)$$

where $i_j(t)$ is the switching current of the jth port and $z_{qj}(t)$ is the inverse Laplace transformation of $Z_{qj}(s)$ which represents the impedance between the jth port and the qth port and $z_{qq}(t)$ is the self-impedance of the qth port and k is the number of the ports.

4. Computational Example: The SSN of Power Distribution Network with Dual Supply Voltages

Multiple power supply voltages are often used in modern high performance ICs, like microprocessors, to decrease power consumption without affecting circuit speed. To maintain the power distribution network impedance below a specified level, multiple decoupling capacitors are placed at different levels of the power grid hierarchy as illustrated in Figure 4 [17].

In this section, a study of a system with two integrated circuits or cores in the same chip is presented. It comprised two equivalent circuits, one without the ground parasitic circuit return (Figure 5) and another with it (Figure 10). Our goal is to obtain the SSN through a detailed circuit analysis.

4.1. Analysis of the SSN for PDN Circuit without Ground Parasitic Circuit Return. A lumped circuit model of a PDN as depicted in Figure 5 is considered [18]. The package pins, PCB, and VRM are modeled using RL circuits. The parameters of decoupling capacitors to provide power to ICs and the noise parameters of the pins are shown by Figure 5. The integrated circuits activity is modeled by current sources. Each current source has a triangular form with an amplitude of 1 A, an impulse width of 0.2 ns, and a period of 2 ns. So, the bandwidth impedance is 3.5 GHz. The coupling between these circuits is modeled by series RLC circuits.

As already mentioned in the introduction, the model of a PCB can be extracted using different methods, such as FDTD and transmission matrix method.

The PDN is composed of several networks of decoupling capacitor, because no single decoupling capacitor network will provide a low enough inductance. Therefore, the real solution to the high-frequency decoupling problem lies in the use of multiple decoupling capacitors. The number of these capacitors and their type, values, and placement with respect to the IC are important in determining their effectiveness. Many approaches have been proposed such as the use of multiples capacitors all of the same value, the use of multiple capacitors of two different values, and the use of multiple capacitors of many different values, usually spaced a decade apart.

As already said in Section 2, to be an effective decoupling network, the impedance of the network must be kept below some target value over the range of interest. This impedance is required to compute the number of capacitors to be used in PDN, while being based on equation mentioned in [19]. After computing the number n of the capacitors, it is possible to calculate the value of the total capacitor from the value of the target impedance. Finding this value and dividing it by the number n allows finding the minimum value to be used for each capacitor network. And using one of the approaches cited earlier, the model to study can be built.

The values of all resistive, capacitive, and inductive elements of the circuit have been taken from the paper [12]. According to this paper, for system with a single core, these values represent a real PCB with dimensions of 80 mm ×

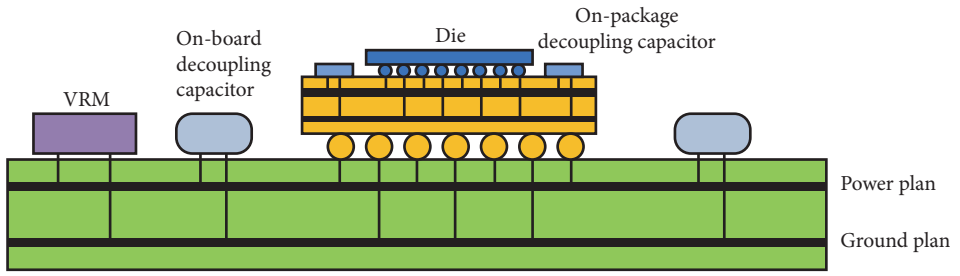

Figure 4: Cross section diagram of PDN.

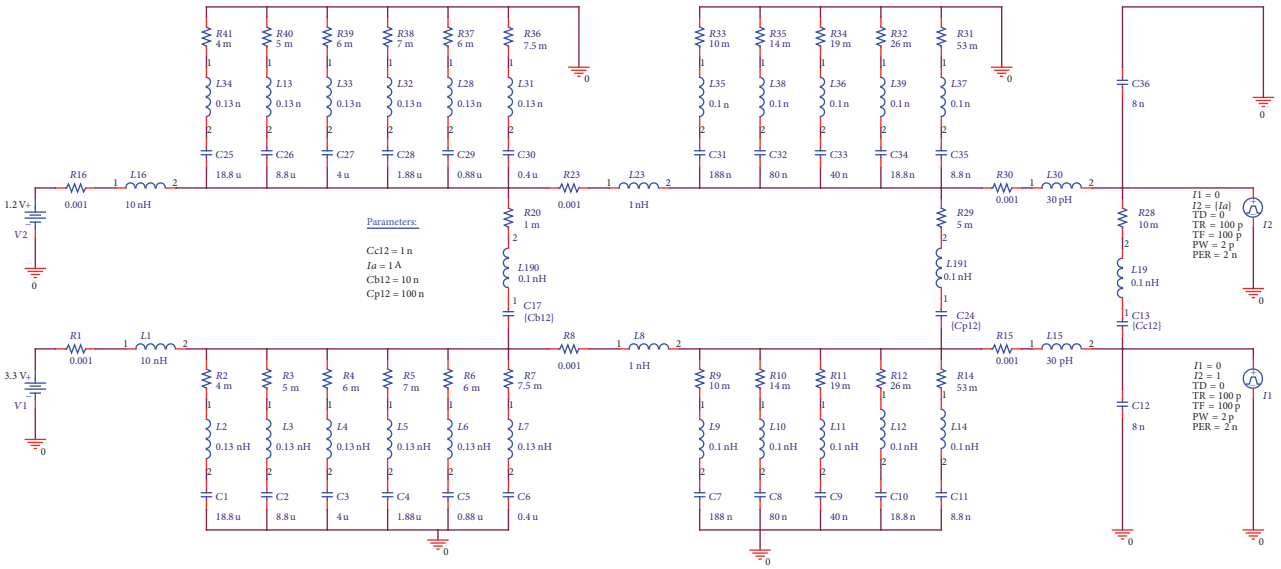

Figure 5: Lumped circuit of the PDN with dual supply voltages and two cores without circuit return.

100 mm. This PCB contains 8 global decoupling capacitors and 4 local capacitors. In our study, we need a PCB with dimensions of 160 mm × 100 mm. This PCB must contain 16 global decoupling capacitors and 8 local capacitors and must be divided into two parts by removing 100 μm of the copper constituting the upper surface of the circuit. This 100 μm presents the coupling between the two parts of PCB.

The circuit rational function parameters are calculated by the principle of vector fitting. But before this calculation, it is necessary to compute the values of this function in specific range of frequency. Obtaining these values is performed by the reduction method in which all elements of the matrix Y are found first, and then the reduction is applied in accordance with the principle explained below.

The circuit of Figure 5 is composed of 8 nodes where the nodes connected to the current sources are considered like two terminals.

So, the circuit admittance matrix $Y(s)$ in the frequency domain has a size 8 × 8 whose elements are calculated as follows [20]:

(i) The Y_{ij} elements present the admittance of the branch between node i and node j with a negative sign.

(ii) The Y_{ii} elements present the sum of the admittance of all branches connected to the node i.

The matrix $Y(s)$ is reduced in accordance with the two terminals 1 and 2. To do this, we write the matrix $Y(s)$ in the form of four submatrices as shown in

$$\begin{bmatrix} i_a \\ i_b \end{bmatrix} = \begin{bmatrix} Y_{aa} & Y_{ab} \\ Y_{ba} & Y_{bb} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \end{bmatrix}, \tag{19}$$

where "a" denotes the nodes 1-2-3-4 and "b" denotes the nodes 5-6-7-8, and Y_{aa} and Y_{bb} are square matrices. Since the current injection to nodes 5-6-7-8 is zero, we have $i_b = 0$, so we can extract v_a according to v_b from the second row in (19):

$$v_b = -Y_{bb}^{-1} Y_{ba} v_a. \tag{20}$$

Inserting (20) into the first row of (19) gives

$$i_a = \left(Y_{aa} - Y_{ab} Y_{bb}^{-1} Y_{ba}\right) \cdot v_a = Y_{\text{red}} \cdot v_a. \tag{21}$$

The matrix Y_{red} obtained has a size 4 × 4, but as we said previously we want to keep just the nodes of the terminals 1

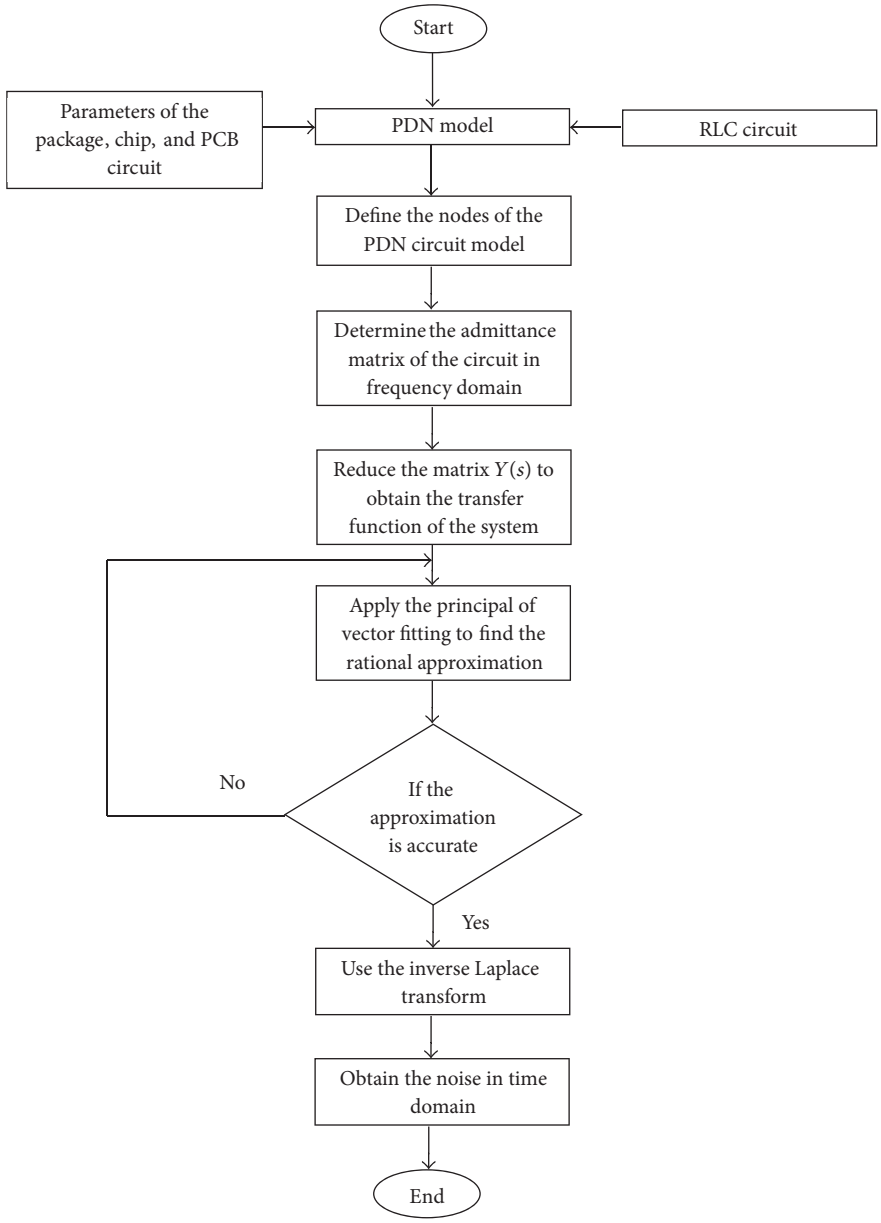

Figure 6: SSN analysis methodology.

and 2, so the matrix Y_{red} needs another reduction to obtain a new matrix of size 2×2. To find this matrix we follow the same procedure mentioned above, where we still decompose once Y_{red} into 4 submatrices Y_{AA}, Y_{AB}, Y_{BA}, and Y_{BB}, where "A" denotes nodes 1-2 and "B" denotes nodes 3-4, and Y_{AA} and Y_{BB} are square matrices.

After obtaining the reduced admittance matrix, the impedance matrix seen from terminals 1 and 2 is calculated by its inverse. Thus, the noise of the two ports is given by

$$\begin{aligned} v_{1\text{noise}}(t) &= z_{11}(t) * i_1(t) + z_{12}(t) * i_2(t), \\ v_{2\text{noise}}(t) &= z_{21}(t) * i_1(t) + z_{22}(t) * i_2(t). \end{aligned} \tag{22}$$

Figure 6 shows SSN methodology followed in this paper.

To make a comparison between the programmed theoretical calculation (VFM + reduction matrix Y) and numerical computation (real circuit), the simulations of this application are made using PSpice and MATLAB tools. During the simulations, there are two factors that influence noise. The first factor accounts for the activity of the second integrated circuit ($I_2 = 1\,\text{A}$ or $I_2 = 0\,\text{A}$), and the second factor is the influence of the coupling capacitor values between the two circuits (test of several values: Figures 7 and 8).

The comparison between the results given by our method and PSpice shows first that the vector fitting is very powerful in the calculation of the poles and residues of the rational function that approximates SSN, which is illustrated by the coincidence of the two curves. The results, also, show that the presence of a second active integrated circuit increases the

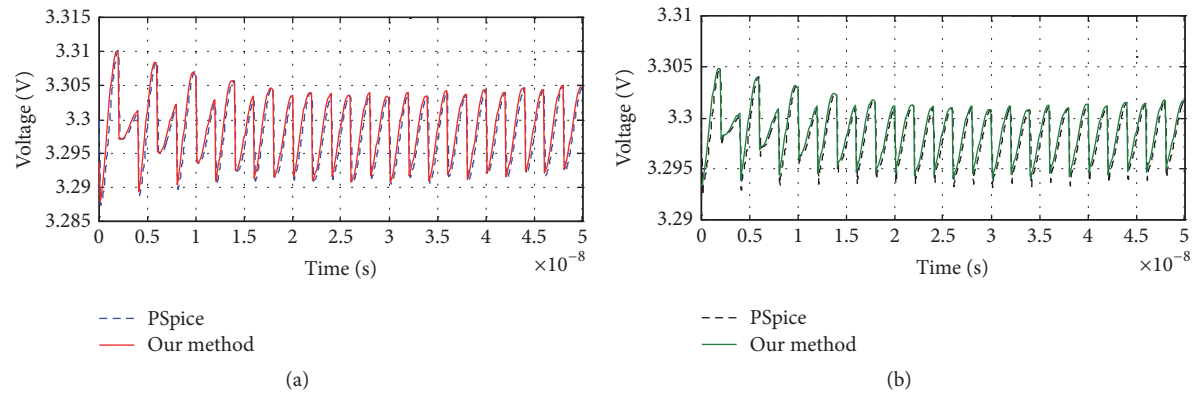

FIGURE 7: SSN waveform of the PDN near the first core; C_{b12} = 1 nF, C_{p12} = 10 nF, and C_{c12} = 100 nF. (a) I_2 = 1 A. (b) I_2 = 0 A.

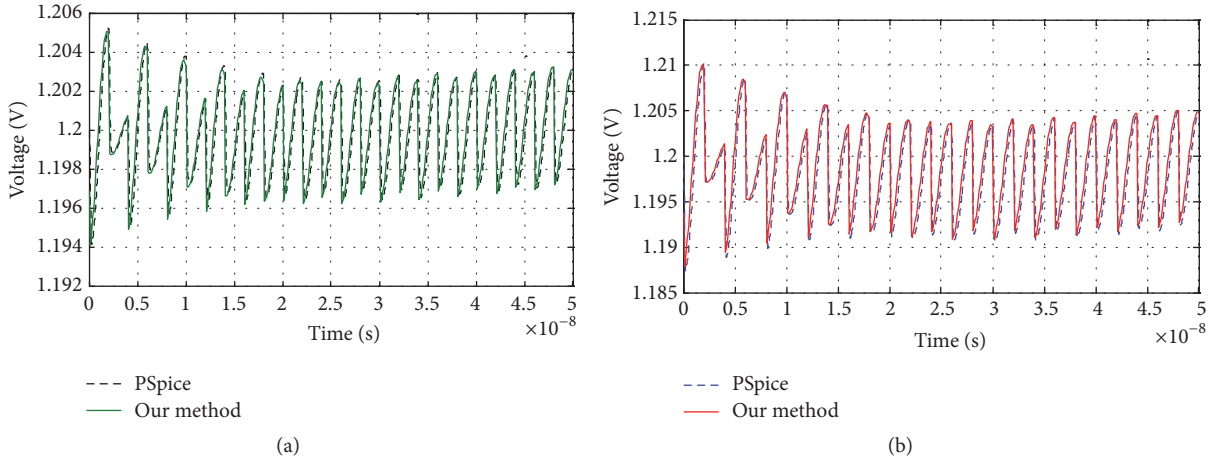

FIGURE 8: SSN waveform of the PDN near the second core; C_{b12} = 1 nF, C_{p12} = 10 nF, and C_{c12} = 100 nF. (a) I_2 = 0 A. (b) I_2 = 1 A.

rate of the SSN to core 1, that is shown in Figure 7, which shows that with I_2 = 1 A and the fluctuations are equal to 22 mV, while with I_2 = 0 A, they are equal to 12 mV.

Presently, by changing the value of coupling capacitance chip C_{c12} through 1 nF instead of 100 nF, we observe that the form of the SSN in the two cores in the case of I_2 = 1 A does not change. But, there are fluctuations in the second case when I_2 = 0 A increase in the first port, whereas they decrease in the second port as illustrated by Figure 9.

From the results of this section we can conclude that the presence of several integrated circuits in the same chip can increase the fluctuations of the simultaneous switching noise due to the existence of coupling between these circuits.

4.2. Analysis of the SSN for PDN Circuit with Ground Parasitic Circuit Return. This second application is for studying and calculating the simultaneous switching noise of the same PDN circuit (Figure 5) except that this time the circuit includes a ground parasitic circuit return (Figure 10), while containing the same component values with the two current sources. A reduction is made for the Y matrix through the previously presented method. The number of reductions done is always equal to two, except that the size of the last reduced matrix is 4 × 4. The simultaneous switching noise in this case is calculated by

$$v_{\text{noise}} = v_p - v_g, \tag{23}$$

where v_p and v_g are calculated by (18). The principle of the rational approximation with vector fitting is always used. The frequency domain noise obtained by PSpice tool is shown in Figure 11. The figure gives the noise for different values of the capacitance C_{c12} near of the two cores.

The study was performed again through the study of the effect of the current of the second core and the values of the coupling capacitors between the two cores.

The presence or the absence of the current of the second core has no effect on the SSN at core 1, whereas at the second core while current I_2 is zero, the degree of fluctuation is presented around 1.2 V. This is justified by the presence of the coupling between the two cores. But the fluctuations in the case of I_2 = 1 A are bigger than the fluctuations in the case of I_2 = 0 A. The simulations of these results are shown in Figure 12.

To study the effect of the coupling capacitance between the PDNs, we keep I_2 = 0 A in all simulations that follow and each time we change the capacitance values.

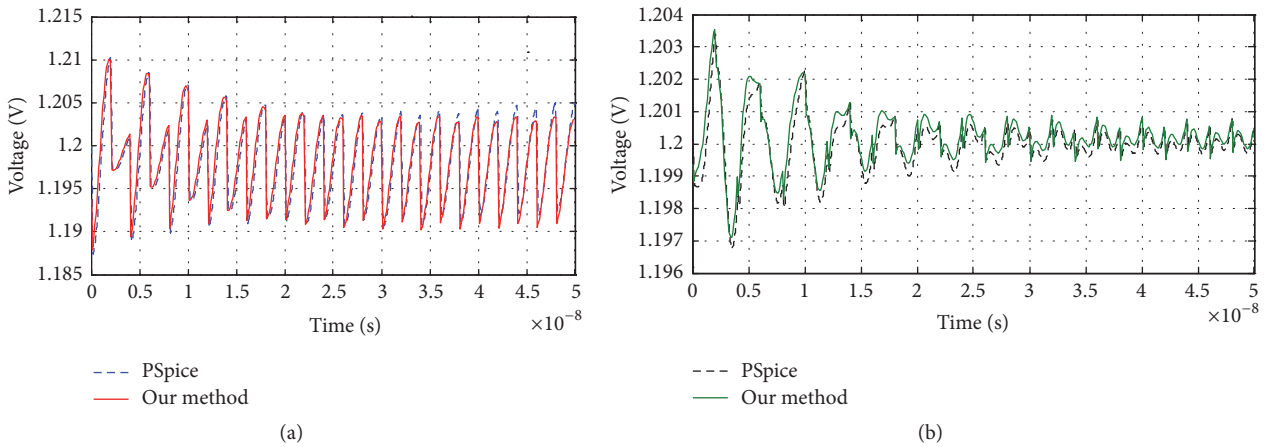

FIGURE 9: SSN waveform of the PDN near the second core; $C_{b12} = 1$ nF, $C_{p12} = 10$ nF, and $C_{c12} = 1$ nF. (a) $I_2 = 1$ A. (b) $I_2 = 0$ A.

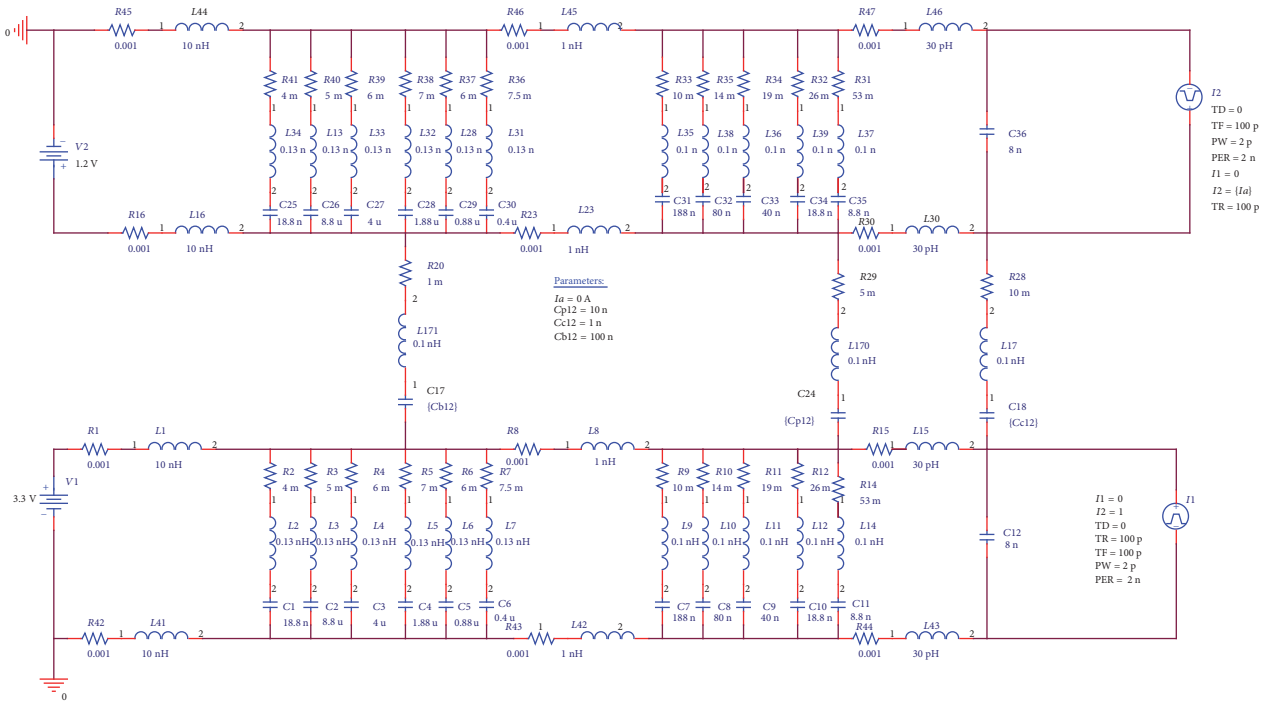

FIGURE 10: Lumped circuit of the PDN with dual supply voltages and two cores and with return circuit.

For the electrical coupling presented by the capacitance C_{c12}, an increase in its values of 1 nF (Figure 12(b)) to 100 nF increases (Figure 13) the fluctuations of the SSN around 1.2 V to almost 5 mV for $C_{c12} = 100$ nF and 2 mV for $C_{c12} = 1$ nF at the second core, while this increase does not have a great influence on the SSN at the first core. Figure 13 illustrates these results.

From these results, we can conclude that the addition of ground parasitic circuit influences the form of the SSN precisely at the second core and the fluctuations become more important. We can also conclude that the larger the coupling is beside the two cores, the more important the noise is.

5. Conclusions

In this paper, a study is made to analyze the simultaneous switching noise in power distribution network with dual supply and two cores. Unlike Ding and Li [12], this study is initiated by the calculation of noise in the time domain by an approximation of the impedance in the frequency domain with a rational function by vector fitting and reduction matrix techniques. Then, the SSN is calculated based on switching current. The results show that the presence of multiple cores in a single card influences the SSN by increasing their fluctuations due to electrical coupling between them. It has

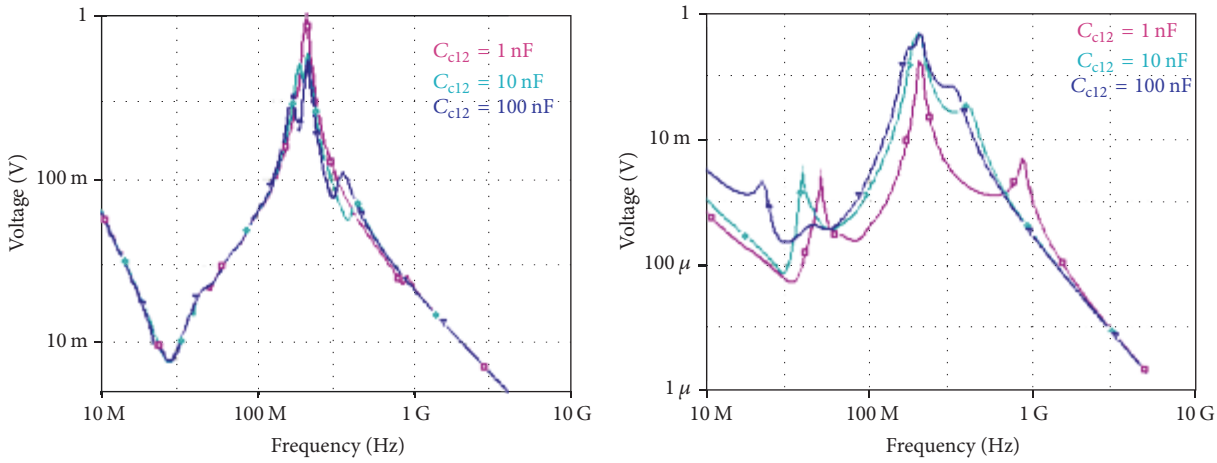

Figure 11: The frequency domain noise of the PDN for C_{b12} = 100 nF, C_{p12} = 10 nF, and C_{C12} = 1 nF, 10 nF, and 100 nF. (a) First core. (b) Second core.

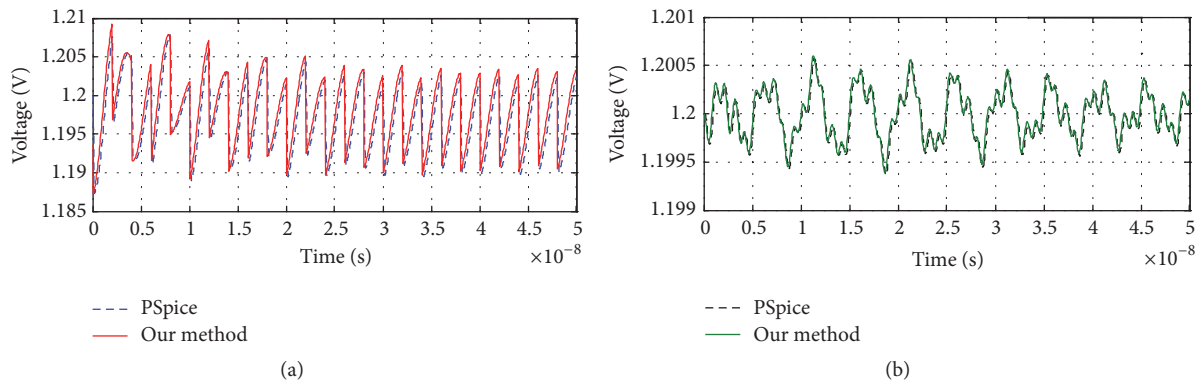

Figure 12: SSN waveform of the PDN near the second core; C_{b12} = 100 nF, C_{p12} = 10 nF, and C_{c12} = 1 nF. (a) I_2 = 1 A. (b) I_2 = 0 A.

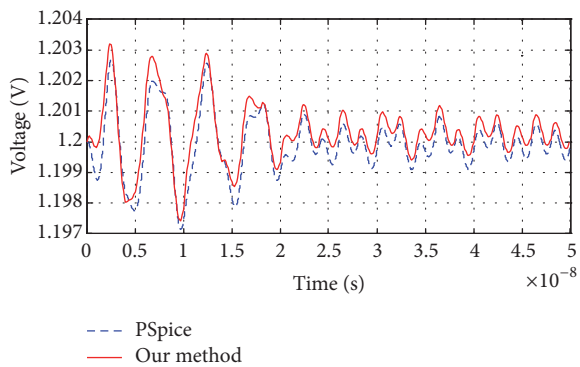

Figure 13: SSN waveform of the PDN near the second core; C_{b12} = 100 nF, C_{p12} = 10 nF, C_{c12} = 100 nF, and I_2 = 0.

been also found that even if a core is not active, a noise exists at its terminals that can disrupt normal operation. According to the latest results, it is found that, the ground parasitic circuit return influences the shape of the SSN. The greater the coupling is beside the cores, the more important the noise is.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

References

[1] R. R. Tummala, "SOP: what is it and why? A new microsystem-integration technology paradigm-Moore's law for system integration of miniaturized convergent systems of the next decade," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 241–249, 2004.

[2] B. Garben, R. Frech, and J. Supper, "Simulations of frequency dependencies of delta-I noise," in *Proceedings of the IEEE 10th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 199–202, Cambridge, MA, USA, 2001.

[3] I. Novak, "Lossy power distribution networks with thin dielectric layers and/or thin conductive layers," *IEEE Transactions on Advanced Packaging*, vol. 23, no. 3, pp. 353–360, 2000.

[4] L. Smith, T. Roy, and R. Anderson, "Power plane SPICE models for frequency and time domains," in *Proceedings of the IEEE 9th Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 51–54, Scottsdale, AZ, USA, 2000.

[5] S. Chun, J. Kim, N. Na, and M. Swaminathan, "Comparison of methods for modeling ALANs power plane structure," *Packag*, pp. 247–250, 2000.

[6] S. Chun, M. Swaminathan, L. D. Smith, J. Srinivasan, Z. Jin, and M. K. Iyer, "Modeling of simultaneous switching noise in high speed systems," *IEEE Transactions on Advanced Packaging*, vol. 24, no. 2, pp. 132–142, 2001.

[7] J.-H. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution planes using transmission matrix method," *IEEE Transactions on Advanced Packaging*, vol. 24, no. 3, pp. 334–336, 2001.

[8] H. Kim, Y. Jeong, J. Park et al., "Significant reduction of power/ground inductive impedance and simultaneous switching noise by using embedded film capacitor," in *Proceedings of the Electrical Performance of Electronic Packaging, '03*, pp. 129–132, Princeton, NJ, USA, 2003.

[9] J. M. Hobbs, H. Windlass, V. Sundaram et al., "Simultaneous switching noise suppression for high speed systems using embedded decoupling," *Proceedings - Electronic Components and Technology Conference*, pp. 339–343, 2001.

[10] R. Abhari and G. V. Eleftheriades, "Metallo-dielectric electromagnetic bandgap structures for suppression and isolation of the parallel-plate noise in high-speed circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 6, pp. 1629–1639, 2003.

[11] T.-L. Wu, S.-T. Chen, J.-N. Hwang, and Y.-H. Lin, "Numerical and experimental investigation of radiation caused by the switching noise on the partitioned dc reference planes of high speed digital PCB," *IEEE Transactions on Electromagnetic Compatibility*, vol. 46, no. 1, pp. 33–45, 2004.

[12] T.-H. Ding and Y.-S. Li, "Efficient method for modeling of SSN using time-domain impedance function and noise suppression analysis," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 3, pp. 510–520, 2012.

[13] L. D. Smith, "Power distribution system design methodology and capacitor selection for modem cmos technology," *IEEE Transactions on Advanced Packaging*, vol. 22, no. 3, pp. 284–291, 1999.

[14] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp. 1052–1061, 1999.

[15] B. Gustavsen, "Fast passivity enforcement for pole-residue models by perturbation of residue matrix eigenvalues," *IEEE Transactions on Power Delivery*, vol. 23, no. 4, pp. 2278–2285, 2008.

[16] P. Triverio, S. Grivet-Talocia, M. S. Nakhla, F. G. Canavero, and R. Achar, "Stability, causality, and passivity in electrical interconnect models," *IEEE Transactions on Advanced Packaging*, vol. 30, no. 4, pp. 795–808, 2007.

[17] M. Popovich and E. G. Friedman, "Decoupling capacitors for multi-voltage power distribution systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 3, pp. 217–228, 2006.

[18] B. Hassan and S. Mouloud, "Analysis and optimization of power integrity issues from high speed CMOS integrated circuit interactions in aeronautic systems," in *Proceedings of the 13th International Multi-Conference on Systems, Signals and Devices, SSD '16*, pp. 636–639, Leipzig, Germany, 2016.

[19] H. W. Ott, *Electromagnetic Compatibility Engineering*, John Wiley & Sons, Inc., Hoboken, NJ, USA, 2009.

[20] B. Gustavsen and H. M. J. De Silva, "Inclusion of rational models in an electromagnetic transients program: Y-Parameters, Z-Parameters, S-parameters, transfer functions," *IEEE Transactions on Power Delivery*, vol. 28, no. 2, pp. 1164–1174, 2013.