

## Research Article

# DRV Evaluation of 6T SRAM Cell Using Efficient Optimization Techniques

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An optimization based method which uses bisection search algorithm has been proposed to evaluate the accurate value of Data Retention Voltage (DRV) of a 6T Static Random Access Memory (SRAM) cell using 45 nm technology in the presence of process parameter variations. Further, we incorporate an Artificial Neural Network (ANN) block in our proposed methodology to optimize the simulation run time. The highest values obtained from these two methods are declared as the DRV. We noted an increase in DRV with temperature ( $T$ ) and process variations (PVs). The main advantage of the proposed technique is to reduce the DRV evaluation time and for our case, we observe improvement in evaluation time of DRV by  $\approx 46$ ,  $\approx 27$ , and  $\approx 8$  times at  $25^\circ\text{C}$  for  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variations, respectively, using ANN block to without using ANN block.

## 1. Introduction

Memory structures are now present not just as stand-alone memory chips but also an integral part of complex VLSI systems [1]. SRAM plays a major role in random access memory design, but its leakage currents reduction has become a major concern in past decade. Various architectures of SRAM cell have been also proposed in this regard [2, 3]. The most straightforward and easier approach for reducing the leakage power is to reduce the supply voltage ( $V_{dd}$ ) of the SRAM cell. Moreover, reducing it below a certain limit may result in the detrition of the stored data due to  $T$  and PVs. In SRAM cell, the critical  $V_{dd}$  above which a data-bit is retained reliably is called the DRV of the cell. Figure 1 shows the reduction of leakage current with the  $V_{dd}$ . Hence, operating the SRAM cell with the voltage higher than its DRV helps in reducing leakage current in standby mode [4]. However, some of the circuit mismatches result in the variation of the  $V_t$  of transistors, which causes shifts in the DRV value. Hence, accurate estimation of DRV is a major challenge in low power SRAM design [5, 6].

Qin et al. developed an analytical model for DRV to get a substantial reduction in leakage current by suppressing the

$V_{dd}$  to DRV [7]. The most straightforward method being used to obtain the DRV is by running Monte-Carlo (MC) simulations until a desired failure probability level is reached [8]. However, this method has many disadvantages.

Since obtaining the failure point is a rare event which makes MC simulation time-consuming [9]. Another issue is the time to find a large number of samples to get the accurate value of the tail of the DRV distribution as shown in Figure 2(a). Importance sampling (mixture importance and sequential importance) methods are developed to improve the speed of simulation. These methods have been proved to be more effective than MC samples in obtaining the failure point [10–12]. Wang et al. proposed two methods to evaluate DRV [13]. In the first method, they propose a statistical model for DRV evaluation which uses the relationship between DRV and SNM. Mean and variance of the SNM distribution have been obtained using MC simulations, and DRV is evaluated as the value of the  $V_{dd}$  at which SNM reaches zero. In the second method, a generic tail model from recursive statistical blockage has been proposed. Postfabrication methods are also developed which uses canary replica cells [14, 15] and built-in self-test [16, 17] to obtain DRV. However, the optimization based method proposed by G. Huang et al. [18] has been

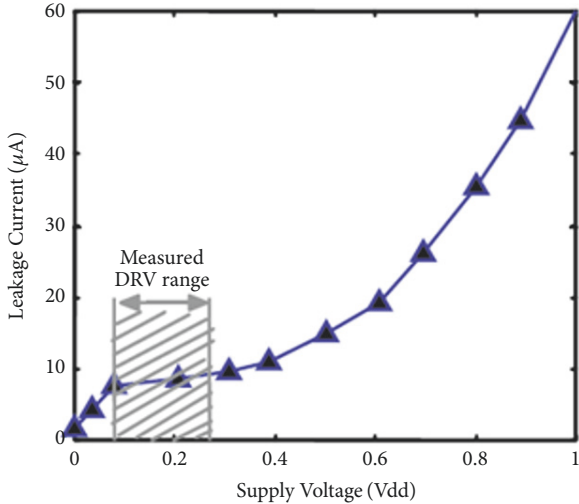


FIGURE 1: Graph showing leakage current versus  $V_{dd}$  [1, 4].

claimed to be the fastest evaluation method to obtain DRV. He formulated DRV as a time domain worst performance bound problem and then multistart point (MSP) optimization strategy is developed to evaluate the failure bound.

We use MATLAB tool (version 2015b) to evaluate DRV using optimization based method. A MATLAB code is written for the node voltage equations (Q, Q<sub>B</sub>) of MOSFET operating in the subthreshold region [19, 20]. Further, we use bisection search algorithm [21] to search the optimum  $V_{dd}$ , and SNM is evaluated using rotation algorithm [22]. PVs are incorporated by generating 5000 quasirandom samples for the Gaussian distribution of  $V_t$ . To reduce the time taken for evaluation, an ANN block is incorporated which predicts the value of SNM for a particular sample point. A set of DRV values are evaluated, and the corresponding histogram is plotted. The highest value of DRV obtained or the tail point of the histogram is considered as the DRV. The procedure used by us has not been claimed so far as per our knowledge. A basic 6T SRAM cell consists of two cross-coupled inverters and two access transistors (M5 and M6) are shown in Figure 2(b). M1 and M3 PMOS transistors are pull-up transistors while M2 and M4 NMOS transistors are known as pull-down transistors. During read or write operation word line (WL) is raised high (transistors M5 and M6 become on) while in hold mode (or retention mode) WL is made low (transistors M5 and M6 turn off) and SRAM store the data present in Q and QB nodes. The ability of the SRAM cell to hold the data in retention mode is determined by the SNM of the SRAM cell. The value of SNM is determined from the butterfly curve of the cell in hold mode. Butterfly curve is a plot of voltages (Q versus QB and QB versus Q), where Q and QB are the node voltages of SRAM cell as shown in Figure 3(a). SNM is evaluated as the length of the diagonal of the maximum square that can be incorporated in the butterfly curve. Figure 3(a) shows the butterfly curve plotted at  $V_{dd} = 1V$  and Figure 3(b) shows the butterfly curve drawn by varying  $V_{dd}$ . It can be observed from Figure 3(b) that the butterfly curve shrinks as the  $V_{dd}$  is reduced and the SNM of the cell reduces to zero at  $V_{dd} = 0.048 V$ .

## 2. Proposed Method

The block diagram used for DRV evaluation has been shown in Figure 4 with different colors. The evaluation procedure has four major blocks.

- (1) Bisection search algorithm is used for optimizing the value of  $V_{dd}$  (blue color in Figure 4).
- (2) Quasi MC sample generation block is used to incorporate process parameter variation or variation of the threshold voltage ( $V_t$ ) (red color in Figure 4).
- (3) Seevinck's rotation algorithm is used for SNM evaluation (green color in Figure 4).
- (4) ANN block is used to optimize simulation time (yellow color in Figure 4).

**2.1. Bisection Search Algorithm [21].** This algorithm helps to evaluate the accurate value of the DRV by searching an optimum solution of  $V_{dd}$  at which the SRAM cell fails. First, we define a rough range of  $V_{dd}$  from 0 to 1 V based on the initial guess of the DRV. Suppose, if the range is defined as  $V_{dd1}$  and  $V_{dd2}$ , the average between these two points is evaluated as  $V_{ddm}$  and this value is used in the analysis phase to evaluate the SNM of the SRAM cell. If the SNM point is evaluated as zero under PVs, it means that the failure has occurred, which implies that the DRV is situated above  $V_{ddm}$  and the point  $V_{dd1}$  is replaced with  $V_{ddm}$ . On the other hand, if the failure has not occurred, the DRV is located below  $V_{ddm}$  and  $V_{dd2}$  is replaced with  $V_{ddm}$ . The process is repeated as the  $V_{dd1}$  and  $V_{dd2}$  values get updated. It is continued until the difference  $\Delta = V_{dd2} - V_{dd1}$  evaluates to be less than a defined tolerance ( $Tol = 0.001$ ). Once this condition is met the process ends and the final value of  $V_{dd2}$  (or  $V_{dd1}$ ) is declared as the DRV. If the DRV is not located within the defined range, the process repeats for a new range. Table 1 represents the MOSFET constants assumed during the evaluation of SNM which is taken from the 45 nm Predictive Technology Model (PTM) [24].

**2.2. Quasi MC Sample Generation.** The value of DRV largely depends on  $V_t$  of the transistors,  $T$ , and channel length ( $L$ ). Variation of these parameters affects the value of SNM and hence the DRV. We do the DRV evaluation only by varying  $V_t$  of transistors M1, M2, M3, and M4 as shown in Figure 2(b). These values are defined in a Gaussian range with particular mean and variance, and their samples are combined with the Quasi MC samples to obtain the seed points. We take 5000 Quasi MC samples for evaluation to get the better accuracy. The SNM is evaluated for each of these seed points generated by Sobol sequence, and failure analysis is done accordingly. The variance of the Gaussian distribution is calculated by Pelgrom model [25, 26],

$$\sigma = \frac{1.8 \text{ mV} * \mu\text{m}}{\sqrt{W.L}} \quad (1)$$

where  $W$  is the width of MOSFET and  $L$  can be used from Table 1. Since during hold mode only transistors M1, M2, M3, and M4 are active, we have employed the variation only for these transistors, which is calculated in Table 2.

TABLE 1: MOSFET parameters used in MATLAB tool for SNM evaluation.

Parameter (unit)	NMOS value	PMOS value
$\mu_0$ , Mobility ( $A/V^2$ )	$\mu_{0n} = 0.04398$	$\mu_{0p} = 0.0044$
$t_{ox}$ , Thickness of oxide (nm)	$t_{oxn} = 1.75$	$t_{oxp} = 1.85$
$\epsilon_r$ , Relative permittivity	3.9	3.9
$n$ , Subthreshold slope factor	$n_n = 1.042$	$n_p = 1.042$
$W$ , Channel width ( $\mu m$ )	$W_n = 0.12$	$W_p = 0.14$
$L$ , Channel length (nm)	45	45
Mean of $V_t$ variation (V)	$V_{tn} = 0.466$	$V_{tp} = -0.4118V$

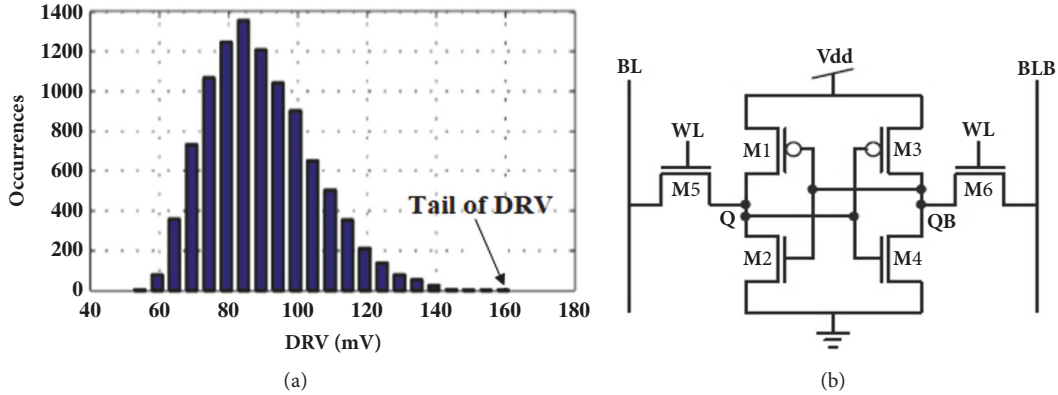


FIGURE 2: (a) DRV distribution obtained by statistical methods using 90 nm technology node for 10K-b SRAM [13]. (b) Schematic of conventional 6T SRAM cell [4].

TABLE 2: The variance of  $V_t$  variation ( $\sigma$ ) is calculated using (1).

Transistors	Variance of $V_t$ variation ( $\sigma$ )
NMOS	0.02449 V
PMOS	0.0226 V

2.3. *SNM Evaluation.* We use theoretical equations developed for node voltages (Q, QB) to calculate the SNM using butterfly curve. These equations have been derived by Calhoun et al. which evaluate the node voltages by considering the characteristics of MOSFETS operating in the subthreshold region. The equation for QB is given by [19]

$$\begin{aligned}
 QB = & V_{th} \frac{n_n n_p}{n_n + n_p} \left( \ln \left( \frac{I_{sp}}{I_{sn}} \right) \right. \\
 & + \ln \left( \frac{1 - \exp((-V_{dd} + Q)/V_{th})}{1 - \exp(-Q/V_{th})} \right) \left. \right) + \frac{n_n \cdot V_{dd}}{n_n + n_p} \\
 & + \frac{n_n \cdot n_p}{n_n + n_p} \left( \frac{V_{tn}}{n_n} - \frac{V_{tp}}{n_p} \right)
 \end{aligned} \quad (2)$$

where  $I_{sn}$  and  $I_{sp}$  are given by [27]

$$I_{sn} = \mu_{0n} \cdot C_{oxn} \cdot V_{th}^2 \cdot \left( \frac{W_n}{L} \right) \cdot (n_n - 1), \quad (3)$$

$$I_{sp} = \mu_{0p} \cdot C_{oxp} \cdot V_{th}^2 \cdot \left( \frac{W_p}{L} \right) \cdot (n_p - 1), \quad (4)$$

where  $V_{th} = kT/q$ , thermal voltage,  $n_n$ ,  $n_p$  are subthreshold slope factor for NMOS and PMOS transistors, respectively,  $I_{sn}$ ,  $I_{sp}$  are drain current (when  $V_{GS} = V_t$ ) for NMOS and PMOS transistors, respectively,  $V_{dd}$  is supply voltage,  $V_{tn}$ ,  $V_{tp}$  are threshold voltage of NMOS and PMOS transistors, respectively,  $\mu_{0n}$ ,  $\mu_{0p}$  are mobility of NMOS and PMOS transistors, respectively,  $C_{oxn}$ ,  $C_{oxp}$  are oxide capacitance of NMOS and PMOS transistors, respectively,  $W_n$ ,  $W_p$  are width of polysilicon for NMOS and PMOS transistors, respectively, and  $L$  is length of polysilicon.

The subthreshold slope factor  $n$  is evaluated using (5) by evaluating subthreshold slope ( $S$ ) [27],

$$S = n \cdot V_{th} \cdot \ln(10) \quad (5)$$

The value of  $S$  is found to be 60 mV/decade at room  $T = 25^\circ C$ . Its value for typical bulk CMOS can range from 70 to 120 mV/decade [28]. The value of  $n$  is evaluated as 1.042 using (5) at room  $T$ . The voltage at which node value Q equals QB is known as tripping voltage ( $V_m$ ). It is the point where curves (Q versus QB and QB versus Q) intersect, as shown in Figure 3(a). Here, we assume the identical cross-coupled inverters to evaluate  $V_m$ . The relation of  $V_m$  for an inverter is given by (6) (by ignoring the Drain Induced Barrier Lowering (DIBL) effects) as follows [29]:

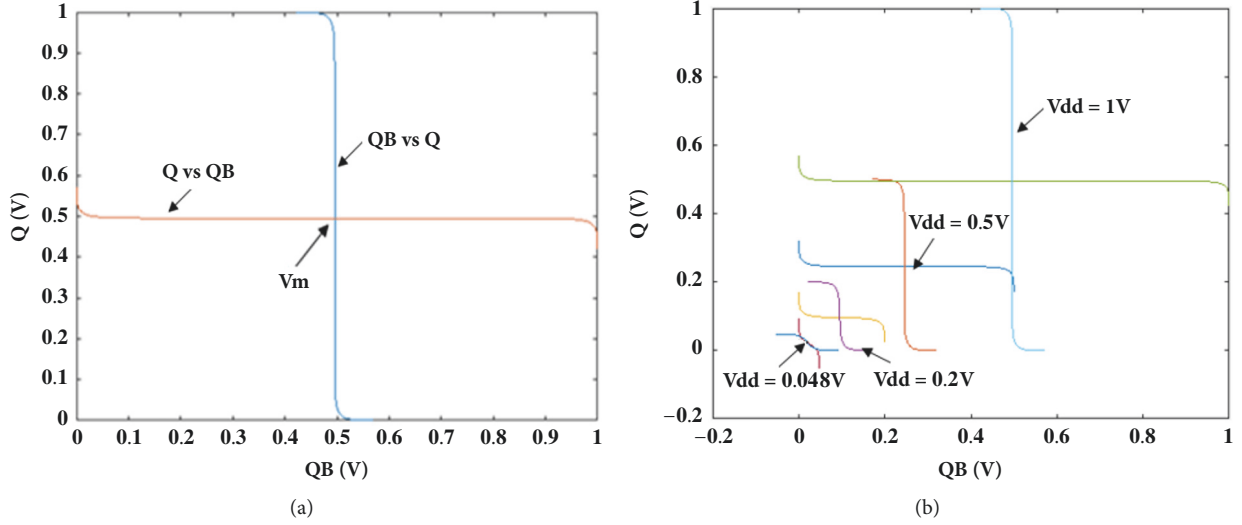


FIGURE 3: Butterfly curve to obtain the SNM of 6T SRAM cell in hold mode (a) at  $V_{dd} = 1V$  (b) by varying  $V_{dd}$ .

$$V_m = \frac{V_{dd} \cdot n_n}{(n_n + n_p)} + \frac{n_p \cdot V_{in} - n_n V_{tp}}{(n_n + n_p)} + \frac{n_n \cdot n_p \cdot V_{th} \cdot \ln\left(\frac{(W_p/L) \cdot I_{sp}}{(W_n/L) \cdot I_{sn}}\right)}{(n_n + n_p)} + \frac{n_n n_p \cdot V_{th} \cdot \ln\left(\frac{1 - \exp((-V_{dd} + V_m)/V_{th})}{1 - \exp(-V_m/V_{th})}\right)}{(n_n + n_p)} \quad (6)$$

All the notations used for (6) are same as mentioned for (2), (3), (4), and (5).

We use the graphical technique proposed by Seevinck [22] to calculate the SNM value as shown in Figure 5. The steps involved in this techniques are as follows:

- (1) Obtain Q and QB samples using (2). Figure 6 shows the butterfly curve which is plotted using Q and QB samples for  $V_{dd} = 0.5V$ .
- (2) Combine Q and QB set into a matrix, X.
- (3) Multiply X with rotation matrix, i.e.,  $[U \ V'] = Rot * [Q \ QB]$ , where \* indicates matrix multiplication and Rot is the rotational matrix,

$$Rot = \begin{bmatrix} \cos\left(\frac{\pi}{4}\right) & -\sin\left(\frac{\pi}{4}\right) \\ \sin\left(\frac{\pi}{4}\right) & \cos\left(\frac{\pi}{4}\right) \end{bmatrix} \quad (7)$$

New axis for the rotated curve is (U, V'). V1 is the matrix corresponding to V'.

- (4) Evaluate V2 as  $V2 = -V1 + (2 \cdot \sqrt{2} \cdot V_m)$ , where  $V_m$  is obtained using (6). (U, V1) is the rotated version of (Q, QB) and (U, V2) is the rotated version of (QB, Q). Figure 7(a) shows the rotated version of Figure 6.
- (5) Take the difference between V2 and V1 samples, i.e.,  $Z = V2 - V1$ .

- (6) Plot (U, Z) as shown in Figure 7(b), and obtain  $S1 = -\min(Z)$ ,  $S2 = \max(Z)$ , and  $S3 = \min(S1, S2)$ .

- (7) Finally, SNM is evaluated as  $SNM = S3/\sqrt{2}$ .

For a particular value of  $V_{dd}$  and each and every sample of Quasi MC seed, the SNM is evaluated.

**2.4. ANN Block.** Artificial neural networks (ANNs) are a family of learning models that are used to estimate functions that depend on a large number of inputs. ANN is generally presented as system of interconnected “neurons” which exchange messages between each other. This functions approximately as a brain. It consists of three layers input variables, hidden nodes, and outputs. Inputs can be of any number and are provided in the initial learning phase. Outputs are the ones which are obtained after the analysis. During the process, many intermediate hidden nodes are created that are essential for optimizing. However, the user does not have any control over them. The optimization process includes two important stages [23]:

- (i) Training or learning phase. This phase uses all the different input signals to predict the possible outcomes of outputs using cautious learning of previous experiments. These can be accomplished either by conducting a large number of experiments or by

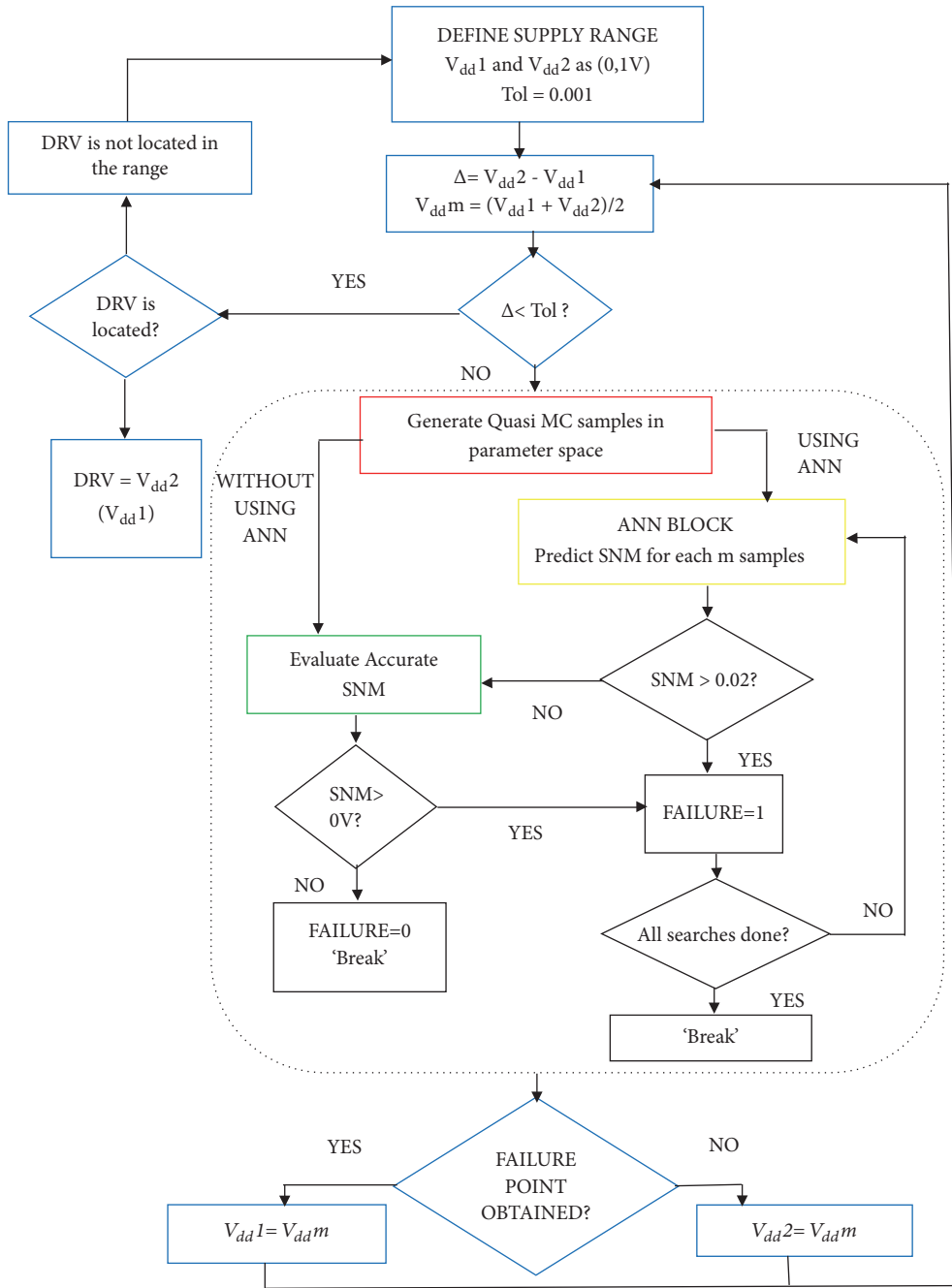


FIGURE 4: General block diagram for DRV evaluation using optimization based method.

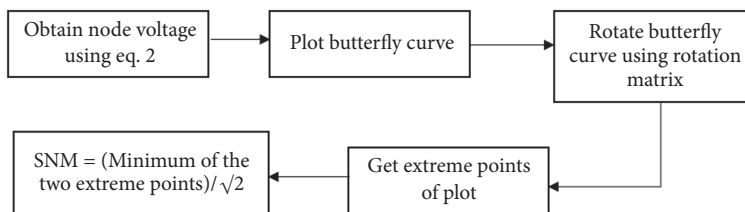


FIGURE 5: General block diagram to evaluate the SNM using optimization method.

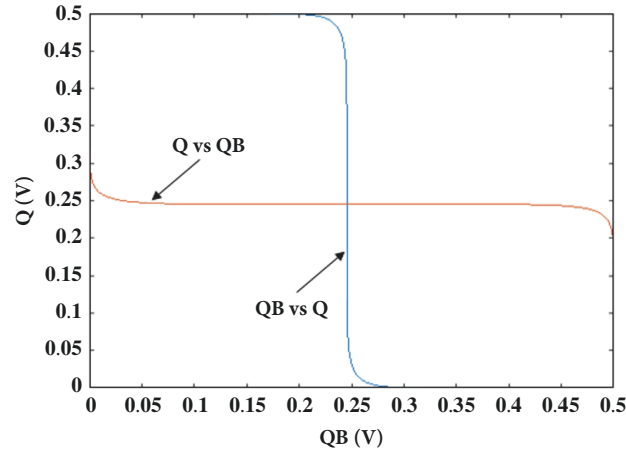


FIGURE 6: Butterfly curve for  $V_{dd} = 0.5V$  using optimization method.

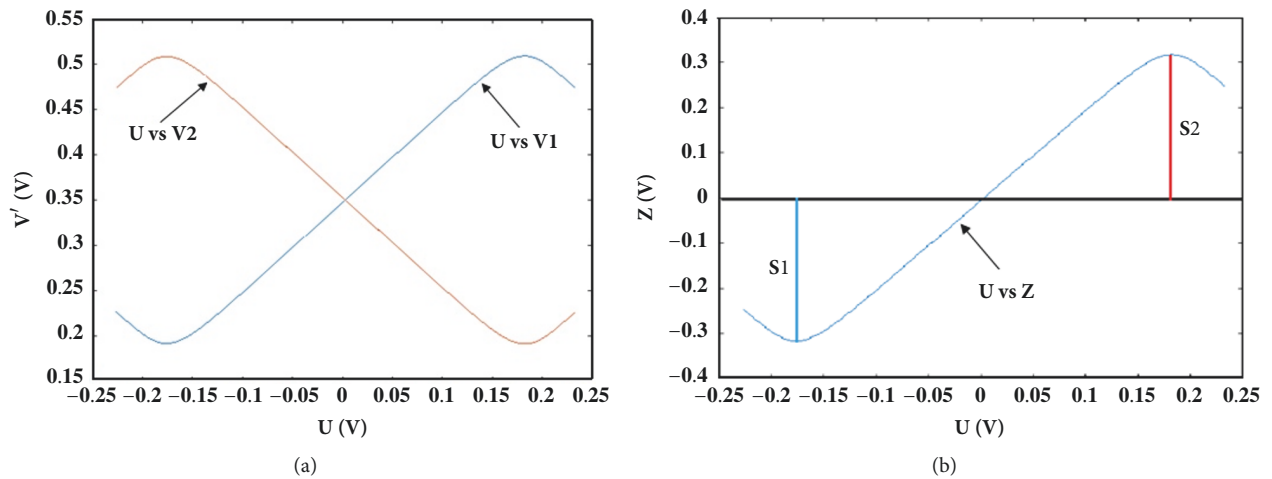


FIGURE 7: (a) Rotated butterfly curve at  $V_{dd} = 0.5V$ . (b) Plot of  $Z = V_2 - V_1$  with respect to  $U$ .

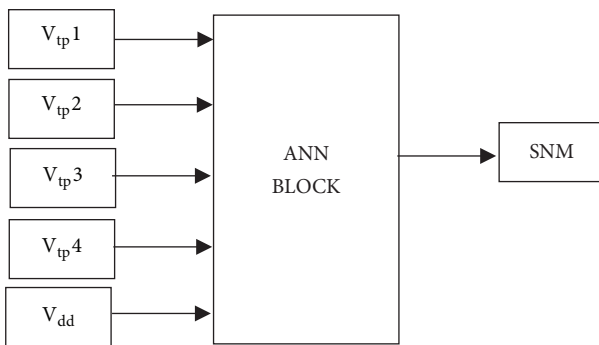


FIGURE 8: General block diagram of ANN block.

using values of the previously conducted experiments. These values will be stored and is used for the upcoming analysis phase.

- (ii) Analysis phase. After learning all the calculation procedure from the previous phase, the network is

now ready for successfully providing outputs for any inputs provided.

For a 5000-sample space as mentioned in Section 2.2, the process of SNM evaluation is time-consuming. Hence, an ANN block which has been trained to evaluate the SNM is used. This block evaluates the SNM for all the samples and then separates the samples having low SNM ( $SNM < 0.02V$ ). Only these samples are now sent to the actual analysis block where the accurate value of SNM is evaluated using rotation algorithm.

If the  $SNM = 0$ , the sample is declared as the failure sample. Input data set consists of  $V_t$  variations of M1, M2, M3, and M4 transistors and the  $V_{dd}$ . SNM is the output vector as shown in Figure 8. Fifty data sets are generated using SNM evaluation algorithm, and the network is trained using Radial Basis Function (RBF) network, which is explained in next subsection.

**2.4.1. RBF Network [23].** An RBF network uses nonlinear functions to map inputs to the outputs into a high dimensional feature space. A general RBF network consists of three



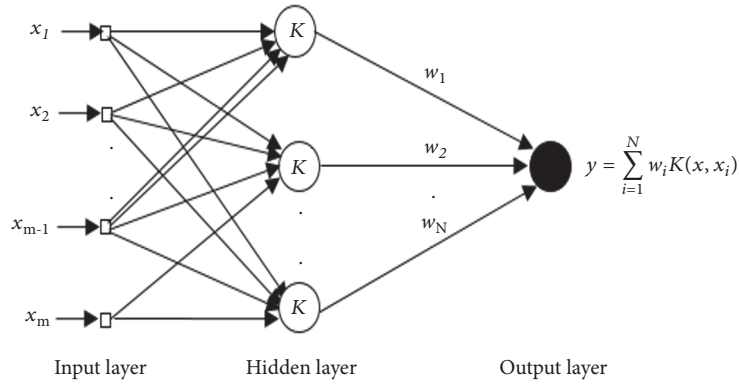


FIGURE 9: Schematic of RBF [23].

layers as shown in Figure 9. The input layer with inputs  $x_i$  ( $i = 1, 2, \dots, m$ ) where  $m$  is a number of input parameters. The hidden layer is generated by one-to-one correspondence between the training input data  $x_i$  and the kernel function  $K(x, x_i)$  for  $i = 1, 2, \dots, N$ , where  $N$  is the number of training samples [23]. In the third layer, the output is evaluated as the linear weighted sum of the kernel functions generated in the hidden layer. The following equations are used by the network:

(i) To evaluate kernel function  $K(x_i, x_j)$ ,

$$K(x_i, x_j) = e^{|x_i - x_j|/2\sigma^2} \quad (8)$$

where  $x_i, x_j$  represent input vectors with  $i, j = 1, 2, \dots, m$ . Here,  $\sigma'$  denotes the Gaussian bandwidth.

(i) Weight vector  $w$  is calculated by

$$(\mathbf{K} + \lambda \mathbf{I}) w = y_d \quad (9)$$

Here  $\mathbf{K}$  is the kernel matrix,  $\mathbf{I}$  is the identity matrix of order  $N$ ,  $\lambda$  is called the regularization parameter, and  $y_d$  is the desired response vector.

(ii) To evaluate output of the network  $y$ ,

$$y = \sum_{i=1}^N w_i K(x, x_i) \quad (10)$$

$w_i$  is the  $i^{\text{th}}$  ( $i = 1, 2, \dots, N$ ) element of the weight vector  $w$  and  $K(x, x_i)$  is the kernel function.

Kernel used for the control technique is an Exponential Radial Basis Function (ERBF). By considering this ANN block, a considerable reduction in the evaluation time is observed. Four different ANN blocks are generated to evaluate the DRV for  $T = 15^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $50^\circ\text{C}$ , and  $100^\circ\text{C}$ , respectively.

### 3. Result and Future Work

In this section, we present the results of an optimization based method which evaluates the DRV of a 6T SRAM cell incorporating the process parameter variation by considering the variation of  $V_t$  of four transistors.

DRV varies within a range and changes with each run of the experiment. It depends on the samples generated by

Quasi MC simulation. To obtain the actual DRV, we conduct the experiment for 25 runs and the highest value obtained is considered as the DRV. After getting the DRV value from 25 experiments the corresponding histogram is plotted for two cases, (i) by considering the ANN block and (ii) by ignoring the ANN block. Table 3 indicates the  $V_t$  variation range for PMOS and NMOS transistors for  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variation.

Table 4 represents the DRV obtained at  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variation for  $T = 15^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $50^\circ\text{C}$ , and  $100^\circ\text{C}$ , respectively, using the parameter specifications shown in Table 1 and the methodology followed in Section 2. From Table 4 we can observe that DRV increases with  $T$  slightly, while it increases significantly with the variation of  $V_t$ . To compare the time taken for DRV evaluation using with and without ANN block we run the MATLAB code at  $25^\circ\text{C}$  for  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variations and note the corresponding time taken for the highest value of DRV for 25 runs as shown in Table 5. Figure 10 represents the corresponding bar chart. The histogram to obtain the DRV at  $T = 15^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $50^\circ\text{C}$ , and  $100^\circ\text{C}$  for  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variation follows the distribution shown in Figure 2(a) and has been presented in Appendix.

However, the time taken for evaluation depends on the version of MATLAB tool, the machine on which the program is executing and how fast the failure sample is obtained out of the 5000 Quasi MC samples generated. From Table 5, we can observe that ANN block helps in reducing the time taken for DRV evaluation. Since the evaluation, time varies randomly for each run so the comparison of evaluation time cannot be generalized. The method can be extended to evaluate DRV for a memory chip with complex circuit structure. The modification can be made in the algorithm, to obtain the more accurate DRV results with better simulation time. Instead of obtaining the node voltage values using theoretical equations, practical SPICE-level simulation can be used to evaluate the SNM for a given  $V_{dd}$  and  $V_t$ . Optimization algorithms can be implemented for the node voltages generated by the circuit. The procedure can be extended for other technology nodes by considering other process parameter variations like  $T$  and geometry variations in  $W$  and  $L$  for other cell topologies.

### Appendix

See Figure 11.

TABLE 3:  $V_t$  variation range used for PMOS and NMOS.

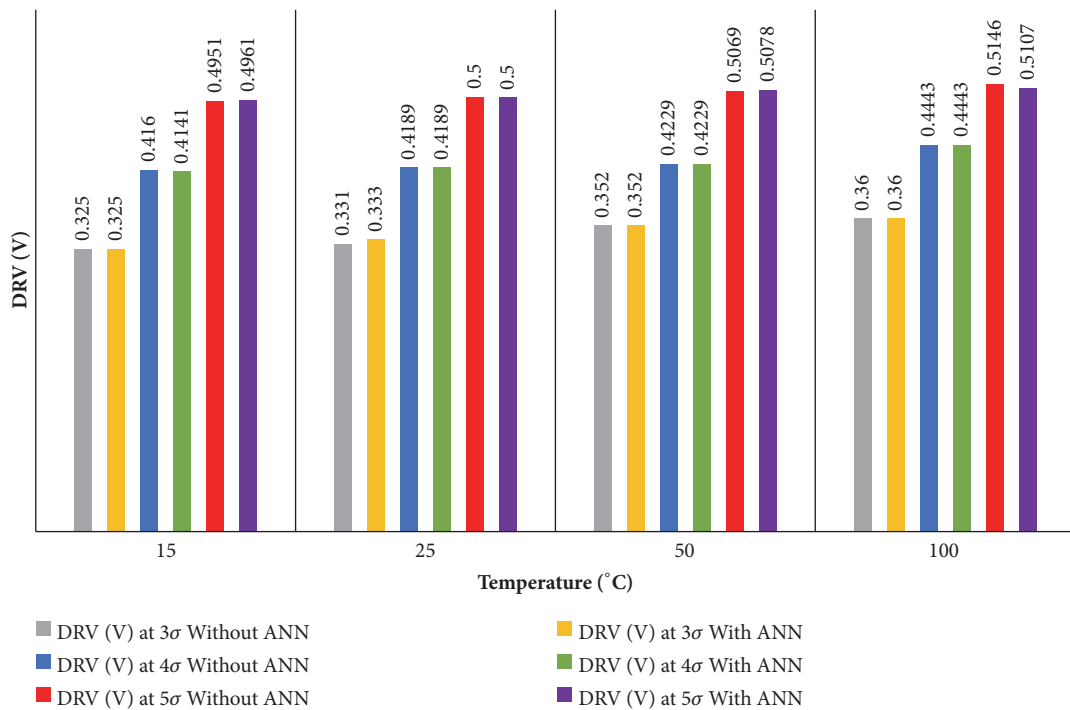
Variation	Range for PMOS	Range for NMOS
$3\sigma$	-0.4796V to -0.344V	0.39253V to 0.53947V
$4\sigma$	-0.5022V to -0.3214V	0.36804V to 0.56396V
$5\sigma$	-0.5248V to -0.2988V	0.34355V to 0.58845V

TABLE 4: DRV values with  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variation of  $V_t$  for  $T = 15^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $50^\circ\text{C}$ , and  $100^\circ\text{C}$ .

Temperature ( $^\circ\text{C}$ )	DRV Without ANN (V)			DRV With ANN (V)		
	$3\sigma$	$4\sigma$	$5\sigma$	$3\sigma$	$4\sigma$	$5\sigma$
15	0.325	0.416	0.4951	0.325	0.4141	0.4961
25	0.331	0.4189	0.5	0.333	0.4189	0.5
50	0.352	0.4229	0.5069	0.352	0.4229	0.5078
100	0.36	0.4443	0.5146	0.36	0.4443	0.5107

TABLE 5: Time elapsed for DRV evaluation at  $25^\circ\text{C}$  for  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variations.

Temperature ( $25^\circ\text{C}$ )	DRV Without ANN (V)			DRV With ANN (V)		
	$3\sigma$	$4\sigma$	$5\sigma$	$3\sigma$	$4\sigma$	$5\sigma$
DRV	0.331	0.4189	0.5	0.333	0.4189	0.5
Time (s)	459	649	783	10	24	103

FIGURE 10: Plot of DRV for  $3\sigma$ ,  $4\sigma$ , and  $5\sigma$  variation at  $T = 15^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $50^\circ\text{C}$ , and  $100^\circ\text{C}$ .



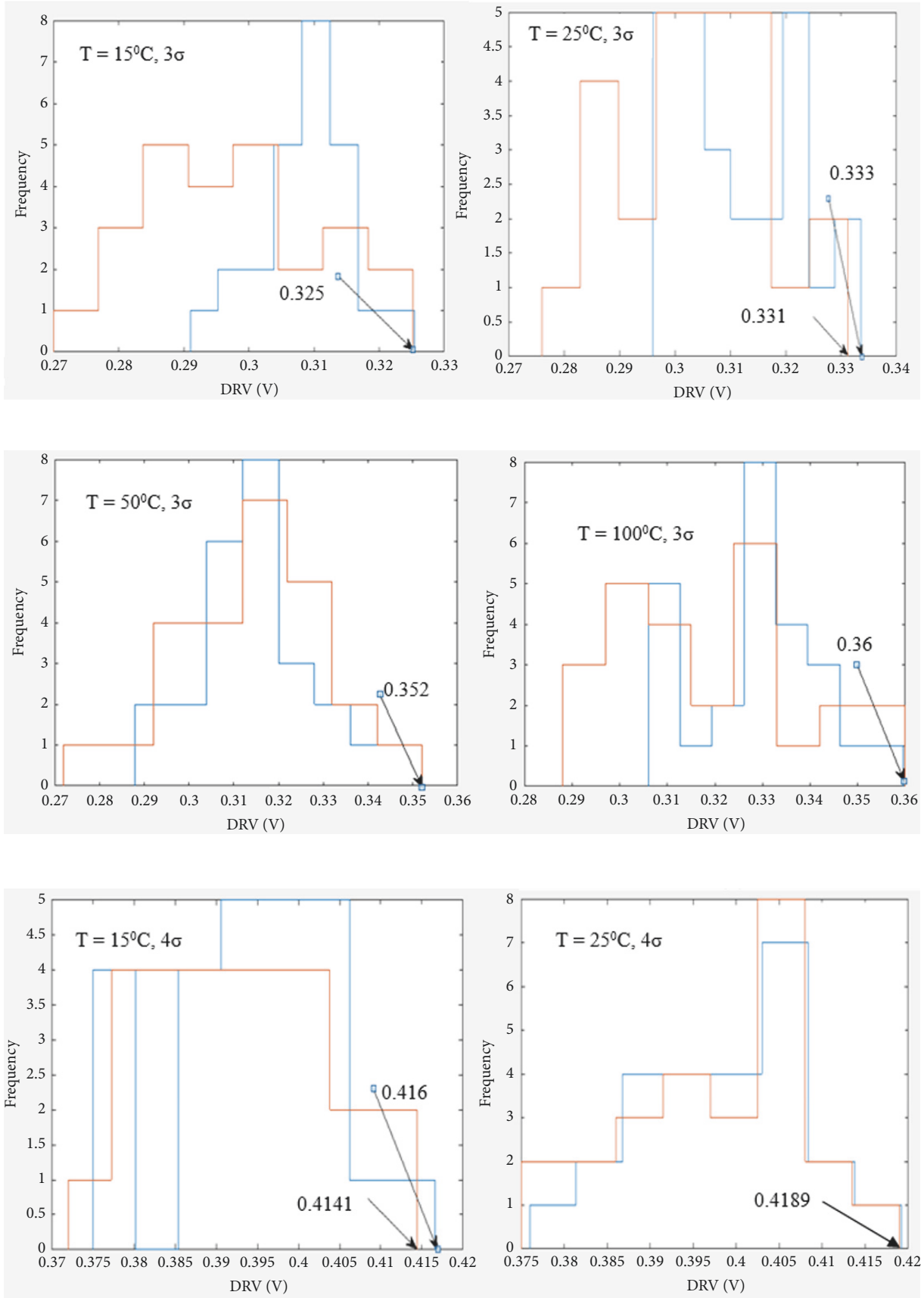


FIGURE II: Continued.

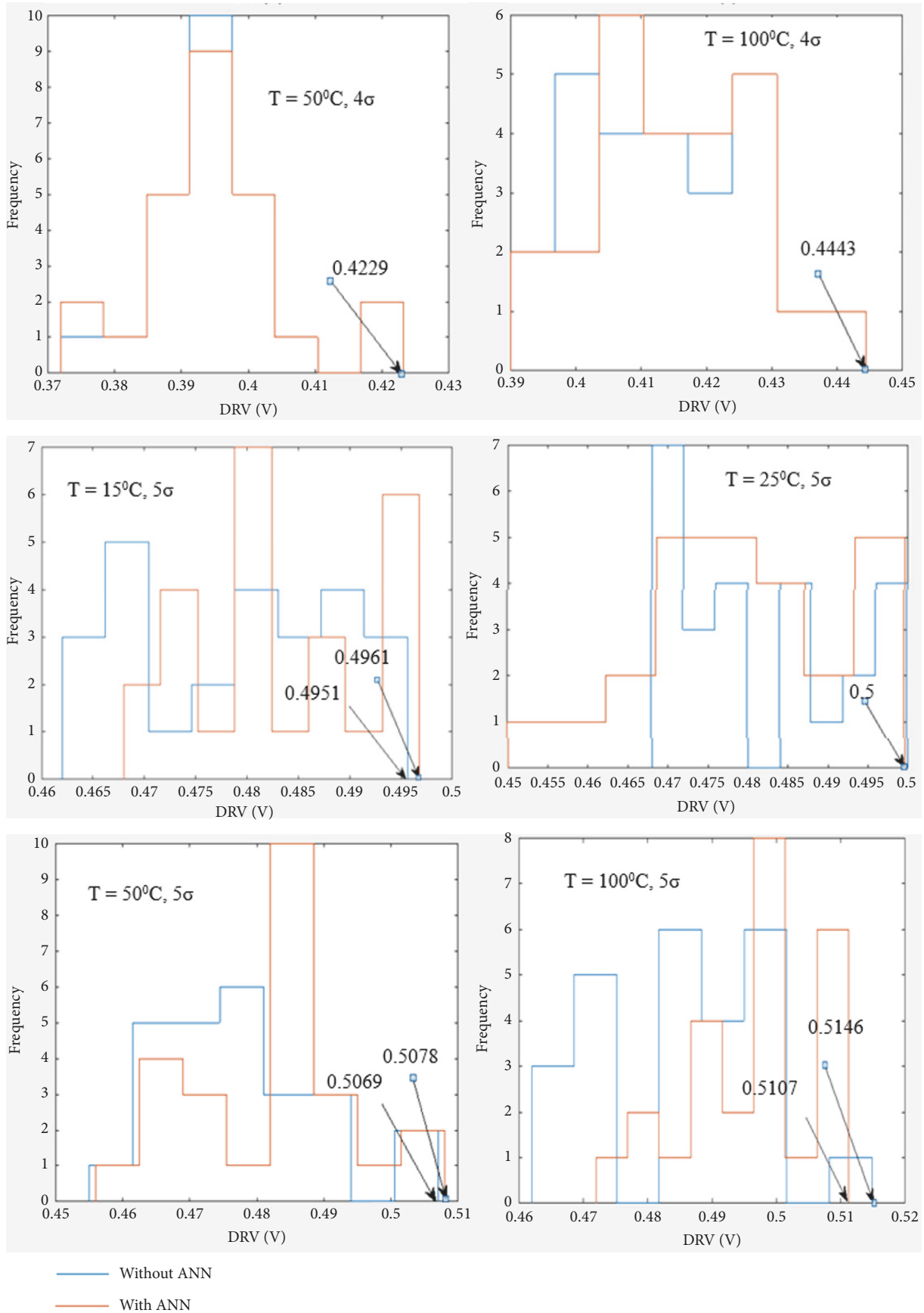


FIGURE 11: DRV for 3  $\sigma$ , 4  $\sigma$ , and 5  $\sigma$  variations at  $T = 15^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $50^\circ\text{C}$ , and  $100^\circ\text{C}$  with and without ANN block.

## Data Availability

The data used to support the findings of this study are included within the article.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

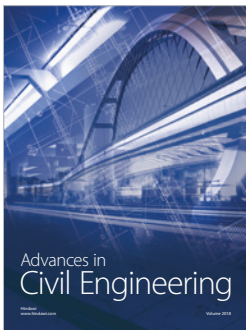
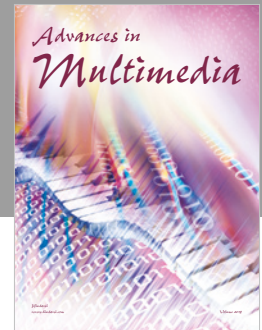
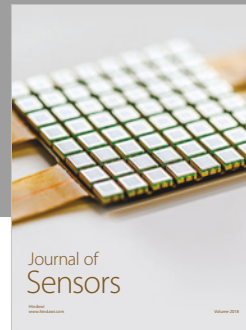
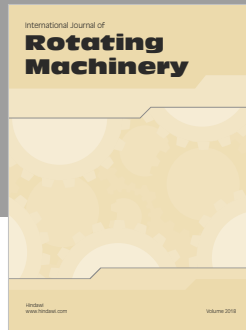
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