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Research Article

Design Tradeoff of Hot Carrier Immunity and Robustness in LDMOS with Grounded Gate Shield

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LDMOS devices with grounded gate shield structures variations were simulated and tested, aiming to address hot carrier immunity and robustness concurrently. Optimal configuration of grounded gate shield structure was found to reduce local electrical field strength at gate-to-drain overlap for better hot carrier immunity, and to achieve uniform E-field distribution on drain side for robustness as well. Design trade off of hot carrier immunity (HCI) and robustness is analyzed by simulation and silicon data.

1. Introduction

Research on HCI were forces on improving the silicon oxide interface quality and reducing the impact ionization near the interface [1]. Recently, LDMOS devices with various configurations, i.e., drain extension, LOCOS, STI, SOI, super junction, floating field plate, and body buried layer, have been comprehensively reviewed [2]. Field plate or gate shield has been a common reduced surface field (RESURF) technique, were first applied to VDMOS device [3], then introduced to the LDMOS device [4]. Several papers have illustrated the HCI mechanism with floating field plate to push the flowing current paths away from the device surface [5, 6].

Robustness is the ability of LDMOS to withstand the power from output mismatched or the power from electrostatic discharge. Robustness of LDMOS can be correlated to the inherently present parasitic bipolar NPN transistor [7], and more body doping to reduce body resistance was suggested. The device could fail because of formation of early filament [8, 9], deep implant drain [10], and ESD implant at drain side [11] were suggested to address the formation of early filament issue. These techniques modify the electric field distribution at the channel and drift region, and have effect on hot carrier injection.

Hot carrier injection reliability and robustness have been two most important reliability issues of LDMOS [8, 9, 12–14], and were discussed separately before. In this paper, HCI and robustness of LDMOS with different grounded gate shield structures were analyzed; the mechanism of trade-off between HCI and robustness were revealed.

2. Device Structure and Design Consideration

The gate shield reduces the electric field peaks at the gate side of the drift region, more than one shield lay out in staircase will result in more ideal constant lateral field distribution. However, more shields could result in more drain capacitance and less drain current. The shield structures, such as the number of shields, the length of shield, the oxide thickness between silicon and shield, are designed to obtain constant lateral field distribution, to trade off design between robustness, reliability, and performance. The complexity of the configuration depends on the application of device. In general, two shields structure is better for LDMOS working at 28 V; however, for LDMOS working at 48 V or more, three shields laid out in staircase could be better.

The structure of the LDMOS device is illustrated in Figure 1. Double grounded gate shields locate above the drift region, connecting to the source by contact via. The one closer to the gate is the first grounded gate shield, the other one with thicker oxide is the second grounded gate shield, which enhance the RESURF effect. The name of these two gate shields are abbreviated as Gsh1 and Gsh2. The original device dimensions are illustrated in Figure 1, the length of Gsh1 is 0.8 μm, it is close

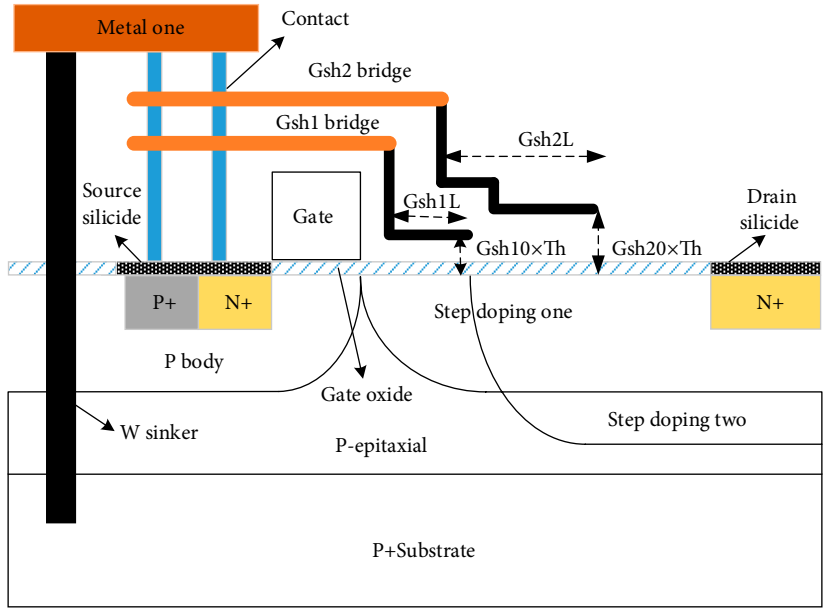

Figure 1: Structure of LDMOS device.

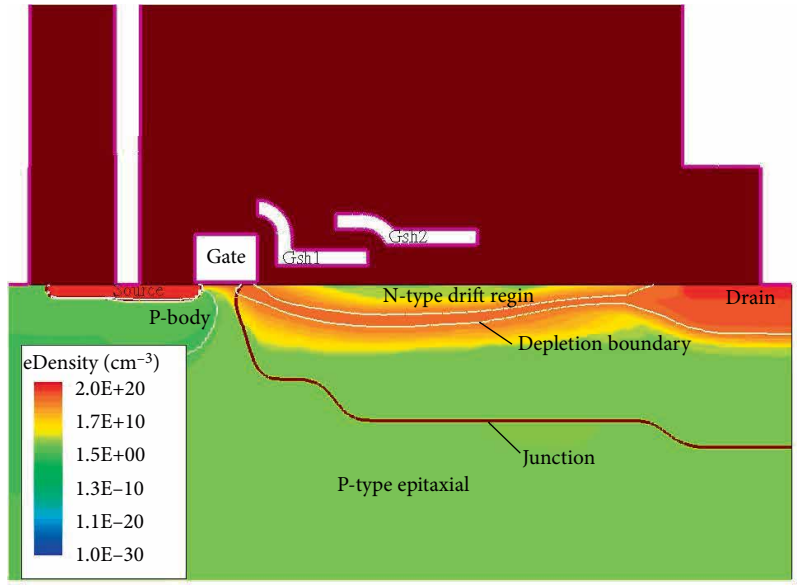

Figure 2: Electronic density at HCI stress condition.

to the right side of poly gate; the length of Gsh2 is 1.3 μm, it is 0.6 μm to the right side of poly gate; the thickness of the oxide between Gsh1 and silicon is 0.12 μm, the thickness of the oxide between Gsh2 and silicon is 0.26 μm. The gate shields do not overlay the poly gate, except the bridges, which connect the gate shields and metal one with contact; the gate shield bridges are the same material as gate shields, the metal one connects the substrate through W-sinker [15]. The contact also connects metal one and source silicide; however, the contact which connects gate shield will not through gate shield to the source silicide.

The resistivity of the substrate is 0.01–0.02 ohm$*$cm, the thickness of the epitaxial layer on the substrate is 5 μm with the resistivity of 1–2 ohm$*$cm. The maximum working voltage of the device is 32 V with the poly gate length of 0.4 μm.

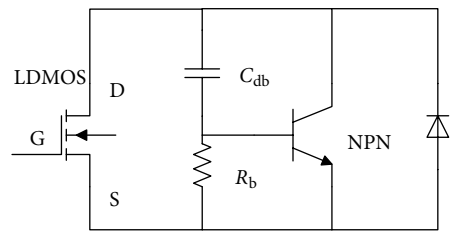

Figure 3: Electric scheme of LDMOS with parasitic NPN transistor.

The length of drift region is 2.8 μm, it is formed with two step doping, the first step starts from poly with phosphorus concentration of 2E12 cm^2, and the second step doping starts

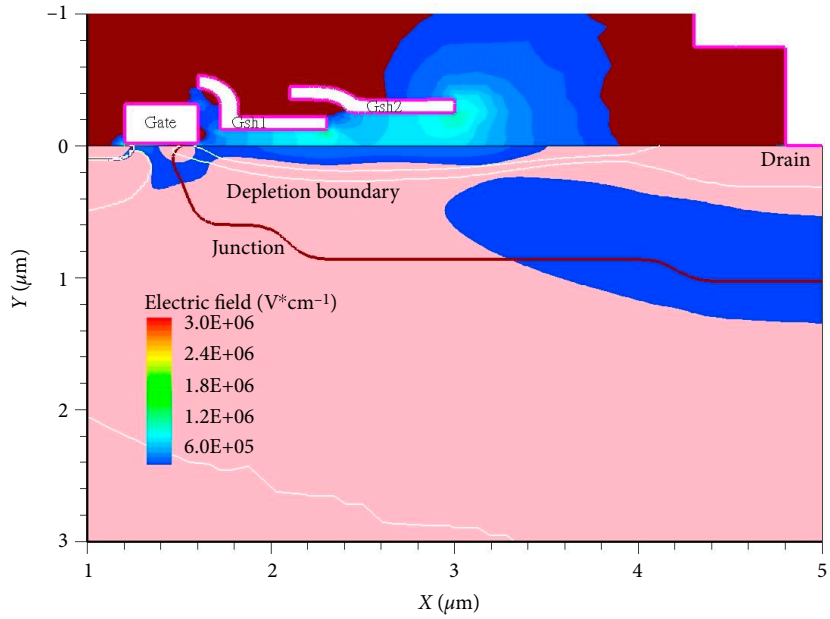

FIGURE 4: Electric field distribution at HCI tested condition.

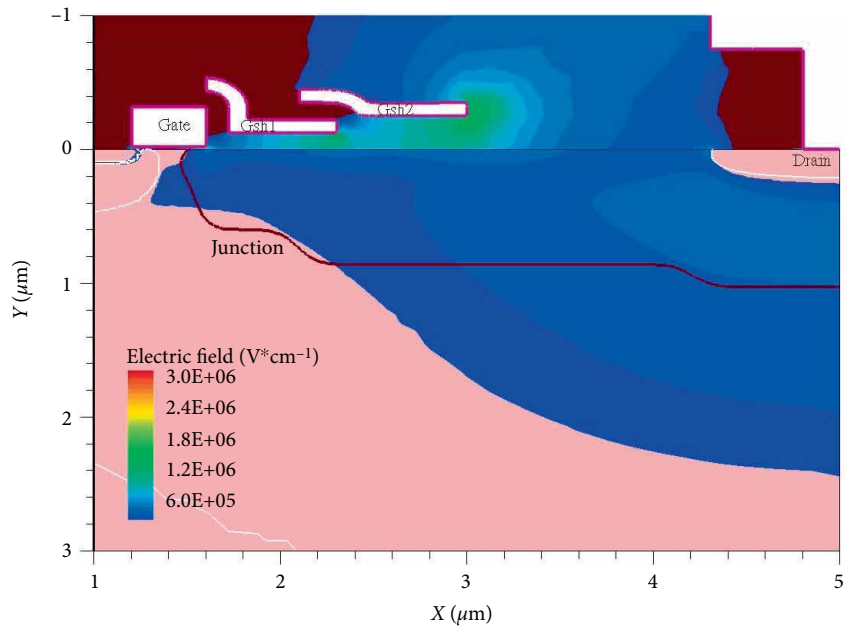

FIGURE 5: Electric field distribution at $V_{ds} = 65$ V and $V_{gs} = 0$ V.

0.6 μm from poly with phosphorus concentration of 1E12 cm^2.

Under strong local electric field, some lucky carriers with enough kinetic energy hit the silicon oxide interface, leaving new interface trapped charges or new ionic bonds. Leading to degradation of on resistance, threshold voltage and saturation current, this is a common understanding of HCI. As illustrated in Figure 2, the drift region under the Gsh1 and Gsh2 is depleted, hence the current under the Gsh1 and Gsh2 is pushed away from the interface, and gathered to the interface near the gate and Gsh1, where horizontal and vertical electric fields are both stronger, which could result in worse HCI. Hence, impact ionization and electric field distribution at the drift region near the gate of different shield structures are simulated to evaluate the HCI reliability.

The electrical equivalent circuit corresponding to the robustness is given in Figure 3, by TCAD simulation, the drain to base capacitance C_{db} is 1.2 fF/mm at 28 V drain voltage, the base resistance R_b is 1.9 ohm$*$mm. Power from output mismatch will reflect to the LDMOS drain, resultings in high drain voltage and strong electric field at the drift region. Then electron-hole pairs will be generated and the hole current may

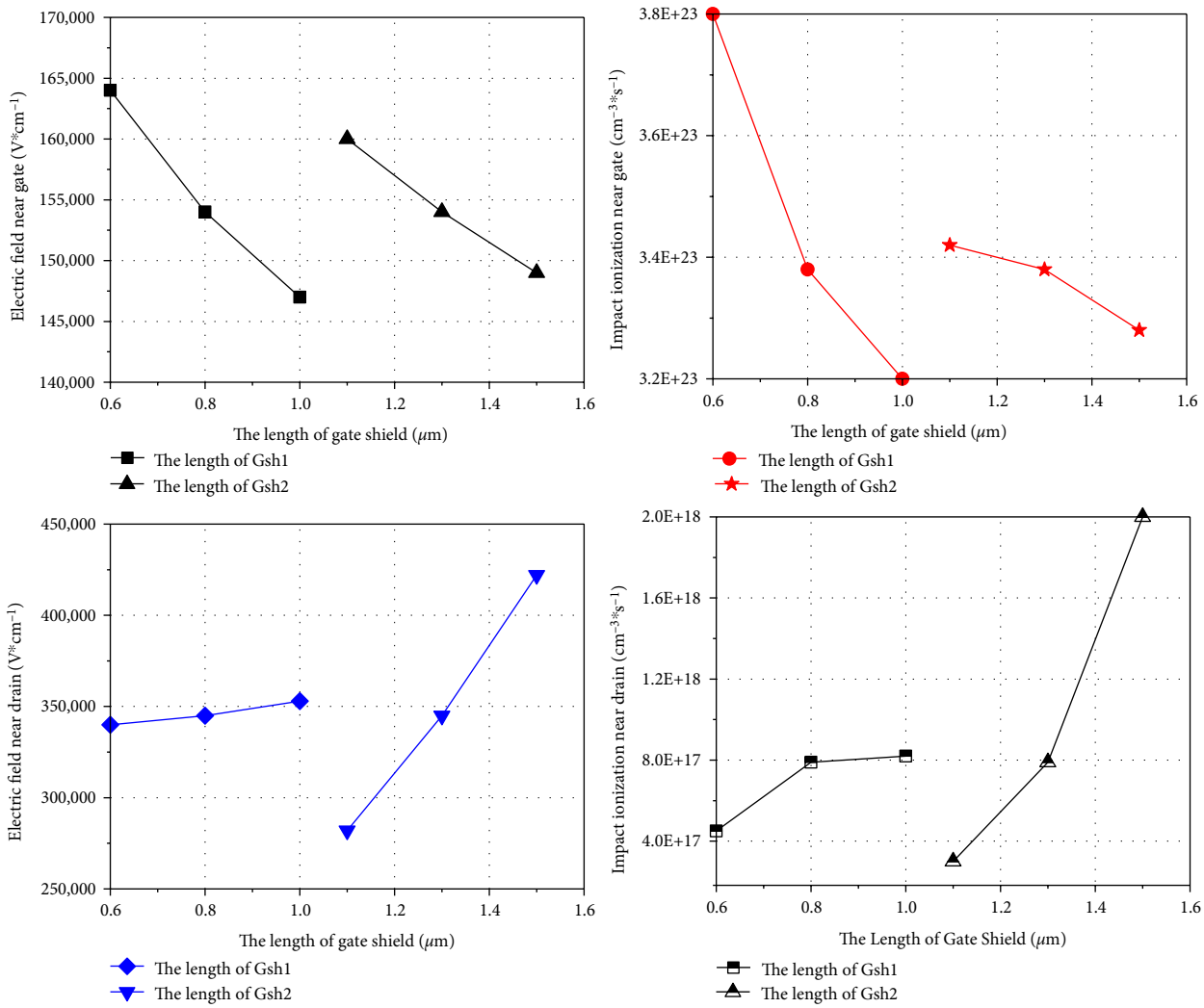

FIGURE 6: The relationship between peak electric field, impact ionization and the length of gate shield.

trigger parasitic NPN transistor, causing the formation of early filament [8, 9], and failure of device. During this power discharging process, the highest electric field happens at the drift region near the drain because of kirk effect [16]. To improve the robustness and HCI reliability, the electric field of drift region near the drain and near the gate has to be designed carefully. For a device with given breakdown voltage, better electric field distribution near the drain means worse near the gate and vice versa. This leads to a trade-off design in HCI reliability and robustness of LDMOS. The next part will be TCAD simulation and observation of different configuration of gate shield.

3. TCAD Simulation and Observation

For the HCI stress condition in this paper, the drain is biased at 32 V and the gate is biased at the voltage where the drain current is 8 mA/mm. This stress condition is used because the maximum working voltage is 32 V and the static drain current is 8 mA/mm. The electric field distribution and impact ionization at HCI stress condition are simulated with TCAD, as illustrated in Figure 4. To reveal the relationship between robustness and electric field distribution, device is biased with gate grounded and V_{ds} equal 65 V, and simulated, as illustrated in Figure 5.

It is observed that, peak electric field located near the gate and the gate shield at HCI stress condition, compared with the current path in figure, drift region near the gate can be the region where hot carrier injected. The peak electric field located near the drain when device biased with gate grounded and V_{ds} equal 65 V, the peak electric field should be low enough to ensure the robustness. To reveal more information, devices with different shield structures are simulated.

The peak electric field and impact ionization of devices with different gate shield length are summarized in Figure 6. The electric field and impact ionization near gate of HCI stress condition decrease as the length of gate shield increase, while the electric field near drain of 65 V condition increase as the length of gate shield increase. Indicating device with longer gate shield has better hot carrier immunity, but worse robustness and less breakdown voltage, as illustrated in Figure 6 and Table 1. For electric field near the drain, the length of gate

Table 1: DC data from simulation.

Shield structure	Off state breakdown voltage (V)	V^{th} (V)	R_{dson} (ohm∗mm)	I_{dsat} (A/mm)
Base line	72.05	1.361	13.083	0.184
Length of Gsh1 −0.2 μm	72.43	1.361	13.056	0.189
Length of Gsh1 +0.2 μm	70.97	1.361	13.106	0.18
Length of Gsh2 −0.2 μm	74.08	1.361	13.065	0.189
Length of Gsh2 +0.2 μm	67.49	1.361	13.099	0.18
Oxide thickness of Gsh1 −0.02 μm	70.37	1.361	13.295	0.172
Oxide thickness of Gsh1 +0.02 μm	72.53	1.361	12.943	0.193
Oxide thickness of Gsh2 −0.02 μm	69.84	1.361	13.092	0.182
Oxide thickness of Gsh2 +0.02 μm	72.39	1.361	13.077	0.185

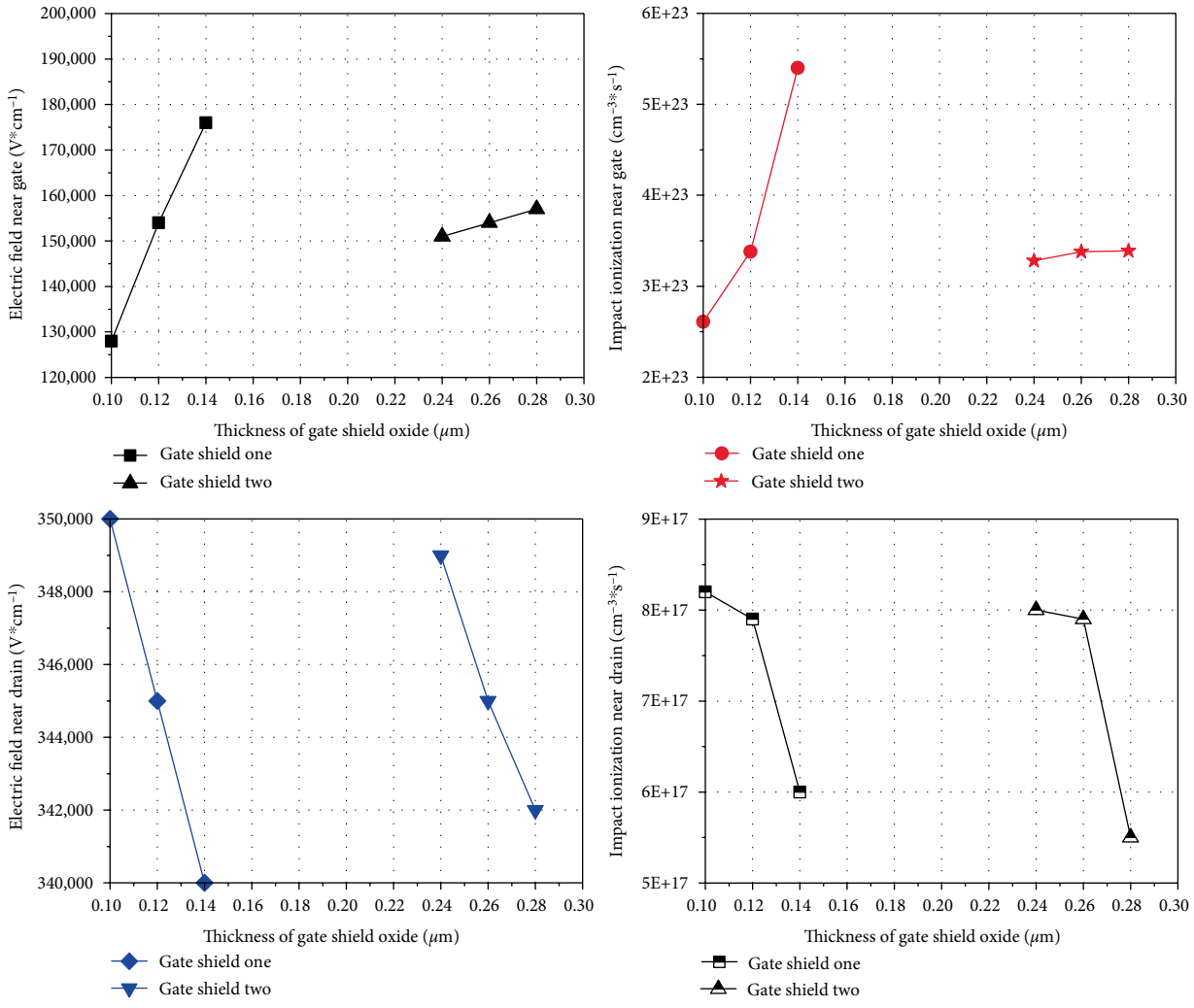

Figure 7: The relationship between peak electric field, impact ionization and the thickness of gate shield oxide.

shield 2 is more significant than gate shield 1. For electric field near the gate, the length of gate shield 1 is more significant than gate shield 2. Similar observation can be obtained with decreasing the thickness of the gate shield oxide, as illustrated in Figure 7 and Table 1.

It can be summarized that devices with longer shield have less impact ionization and lower electric field near the gate, which may resultings in better hot carrier immunity, but higher electric field distribution near the drain may results in worse robustness. This can be explained as the electric field distribution changed by the longer part of shield. Since the shield is grounded, more electric field lines are terminated to the shield near the drain and less to the drift region near the gate with longer shield. More importantly, current path is

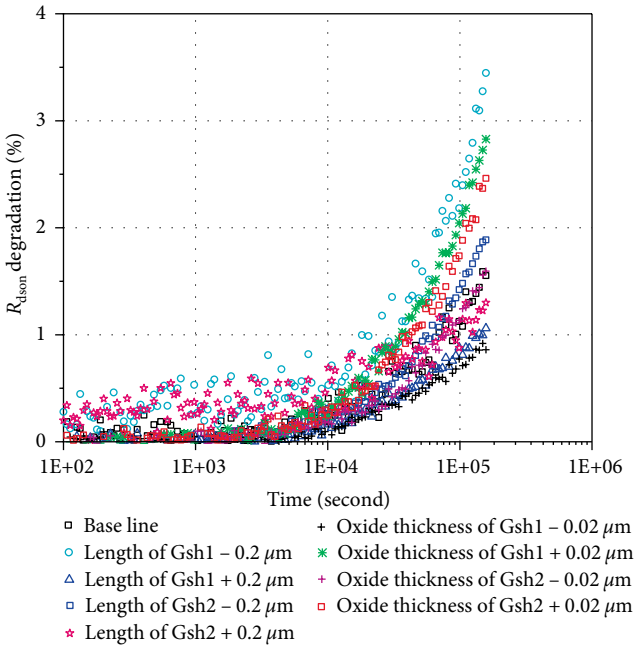

Figure 8: On resistance degradation during HCI testing.

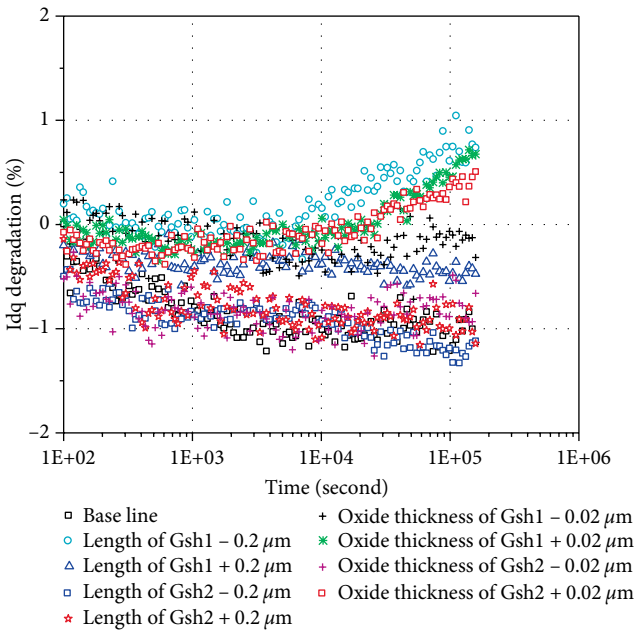

Figure 9: Static bias current degradation during HCI testing.

pushed deeper into silicon by the gate shield, results in better hot carrier immunity but less saturation current as illustrated in Table 1. Similar explanation can be applied to the thickness of oxide between gate shield and silicon. To verify the simulation, devices with different grounded gate shield structure are implanted and tested. Both longer gate shield and thinner oxide enhance the depletion of silicon by gate shield, resulting in more ionized charge; according to the electric charge and electric field relationship of Maxwell's equations, this will reduce local electric field peak; however, the electric field peak near drain will increase under the same drain voltage.

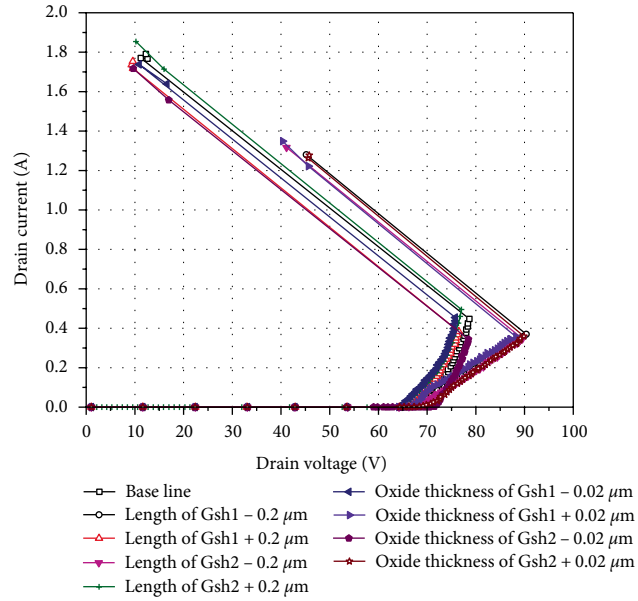

Figure 10: TLP test results of different gate shield structures.

4. Measurement and Discussion

Figures 8 and 9 illustrate on resistance and drain current degradation of different gate shield structures at the HCI stress condition versus time. The initial drain current was 8 mA/mm under drain voltage of 32 V, and on resistance was tested at V_{gs} equals 5 V and V_{ds} equals 0.1 V.

It can be observed that the tested data match with TCAD simulation, the stronger the electric field near the gate, the worse the resistance and drain current degradation. It is observed that the device with the worst on resistance degradation is accompanied by positive drain current degradation, while the other is with negative drain current degradation. This can be explained by the strongest impact ionization near the gate, causing hot carrier injection happening at the silicon oxide interface under the gate and the drift region. The electric field peak concentrated in the gate oxide near drift region, may reduce the reliability problem such as tunneling or gate oxide breakdown. The tunneling effect can be detected by gate leakage current, while gate oxide reliability can be verified by high temperature gate biased test (HTGB).

Figure 10 illustrates the TLP result of devices with different gate shield structures. It is observed that device with 0.2 μm shorter Gsh1 and Gsh2, 0.02 μm thicker Gsh1 oxide and 0.02 μm thicker Gsh2 oxide can withstand higher drain voltage when generating the same current than other structures, indicating more power can be discharged with better robustness. Looking back to the simulation, electric field distribution near drain of devices with shorter shield and thicker oxide is more uniform, and the peak electric field is lower, this is the reason that they have better robustness.

DC data of devices are listed in Table 2, all the devices have an approximate breakdown voltage except for conditions E and H, the reason is that electric field distribution of these two devices are less uniform. The length and oxide thickness of second gate shield are a significant factor to breakdown voltage. The on resistance is tested at very low drain voltage, almost

Table 2: DC data from test key.

Shield structure	Breakdown voltage (V)	V^{th} (V)	R_{dson} (ohm∗mm)	I_{dsat} (A/mm)
Base line	67.82	1.425	14.239	0.163
Length of Gsh1 −0.2 μm	67.94	1.411	14.342	0.164
Length of Gsh1 +0.2 μm	67.81	1.421	14.276	0.163
Length of Gsh2 −0.2 μm	68.01	1.412	14.238	0.167
Length of Gsh2 +0.2 μm	66.94	1.429	14.192	0.162
Oxide thickness of Gsh1 −0.02 μm	68.13	1.43	14.343	0.159
Oxide thickness of Gsh1 +0.02 μm	68.33	1.408	14.117	0.169
Oxide thickness of Gsh2 −0.02 μm	67.59	1.427	14.222	0.162
Oxide thickness of Gsh2 +0.02 μm	68.32	1.419	14.272	0.164

not affected by the gate shield, so all the devices have an approximate on resistance. The shield will push the current into silicon, thus the saturation current of conditions E, F, and H is less than that of the other condition.

It can be summarized that, first of all, shorter gate shield or thicker oxide between silicon and shield will result in stronger electric field distribution near the gate, leading to worse HCI reliability, and the first gate shield is more significant than the second one. Secondly, shorter gate shield length device or thicker oxide between silicon and shield will result in more uniform electric field distribution near the drain, leading to better robustness and higher breakdown voltage, and the second gate shield is more significant than the first one, especially for breakdown voltage. Finally, HCI reliability and robustness have to be trade off in the LDMOS, it can be realized by a careful selection of grounded gate shield structure.

Different structures of grounded gate shield impact the HCI reliability and robustness by changing the electric field distribution in different area of drift region. With longer shield, or thinner oxide, more electric field lines from drain are terminated to the shield, decreasing the electric field near the gate, which is good for HCI reliability but bad for robustness. In another case, shorter shield or thicker oxide make more electric field lines terminated to the gate or source, increasing the electric field near the gate, which is bad for HCI reliability but good for robustness.

Actually, the configuration of gate shield will change the depletion near silicon interface, thus change the local electric field, according to electric charge and electric field relationship of Maxwell's equations. As discussed in previous paragraphs, increasing of electric field peak near gate can result in worse HCI, while increasing of electric field peak near drain can result in worse robustness. In the condition of drain output mismatch or drain electrostatic discharge, power reflected to the drain, leading to an increase in the electric field near drain, results in the generation of electron-hole pairs; the hole current increases the voltage drop on R_b, which may trigger the turn on of NPN transistor. This is the process of ESD, and drain output mismatch. With the configuration gate shield, the electric field peak near drain is optimized, resultings in a higher second breakdown voltage, thus more power can be discharged before the NPN transistor turns on, with better robustness.

5. Conclusion

In this paper, trade off design of HCI and ESD robustness in LDMOS was analyzed. Uniform distribution of electric field near the drain results in better robustness and breakdown voltage, while better HCI reliability can be obtained by uniform distribution of electric field near the gate. The best HCI and robustness trade off can be obtained by carefully selection of grounded gate structure. At the same time, kirk effect should be released with more uniform electric field distribution at the drift region, hence device will saturate at higher voltage with better linearity.

Data Availability

Experimental results provided in the article were obtained in the System Integration and IC Design Division of Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences in 2018.

Conflicts of Interest

The authors declare that they have no conflicts of interests regarding the publication of this paper.

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