Series resistance effect on the output parameters of buried emitter silicon solar cells

Gamal M. Eldallal,[1] Mohamed Y. Feteha,[2] and Mostafa E. Mousaa[3]

[1] *Eng. Math.& Physics Dept., Faculty of Engineering, Alexandria University, 21544, Alexandria, Egypt*

[2] *Institute of Graduate Studies and Research, Alexandria University, P.O.B. 832, Alexandria, Egypt*

[3] *Air Defence College, Alexandria, Egypt*

ABSTRACT. A realistic distributed equivalent circuit for the buried emitter silicon solar cell is presented taking into consideration the carriers paths through the planar and vertical junctions. In addition, a new theoretical model for the cell characteristics including the cell's mismatching, series resistance, different junctions (planar and vertical) and junctions geometry is considered in this work. The results are compared with the published data.

1. INTRODUCTION

Since the efficiency is an important economical factor in photovoltaic arrays, making higher efficiency silicon solar cells—at no higher cost—is an important way of making energy production by solar cells more competitive [1–5]. The multijunction cells have better efficiency than that obtained in conventional cells [2] due to their high internal quantum efficiency. The Buried Emitter Solar Cell (BESC) proposed by Bouazzi *et al.* [1] is presented in Figure 1 which is consisted of planar and vertical junctions. The vertical junction is potentially a more efficient device compared to the conventional junction (planar) due to its high collection at different wavelengths and high radiation resistance [6–11].

One of the important ways for achieving high efficiency for the solar cell is to reduce the effect of the series resistance. The different series resistance components come from semiconductor bulk, metal bulk, contact resistance, and lead connections [12].

The modeling of the BESC performance was investigated in different works [1, 2, 13]. In [1], the effects of the loading between the cells and the series resistance are neglected and as a consequence, an overestimated performance for the cell was obtained. On the other hand, a proposed model taking into consideration the effect of the internal loading was presented in [2] but still a little bit far from the realistic performance. In this work, we propose a new theoretical model for BESC performance considering the effects of the internal loading and the series resistance and in addition, the effect of the planar and vertical junctions. The effects of the series resistance and the internal mismatching on the different current components of the different junctions and their relations to the different cell's thickness are studied.

2. ANALYSIS

A cross-section area for the proposed symmetrical BESC structure is shown in Figure 1 with its four cells. Each cell consists of one planar junction and two vertical junctions. The light (AM0) enters through
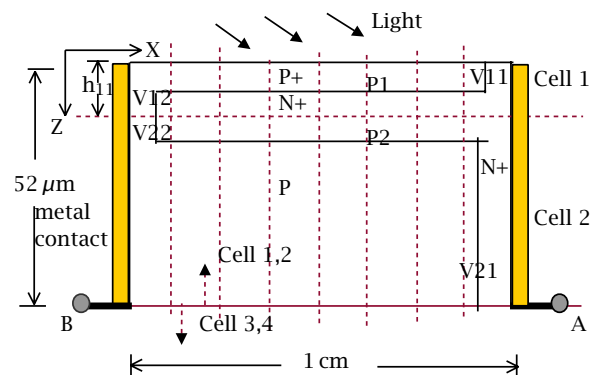

Figure 1. *P1(P+ N), V11, V12, P2(N+ P), V21 and V22 are the planar and the vertical junctions of cell 1 and cell 2, respectively. h_{11} and $(52\,\mu m - h_{11})$ are the thicknesses of cells 1 and 2 respectively.*

the P+ layer in the Z-direction and as a consequence the generated carriers can be collected by the planar and vertical junctions in each cell. The total output current from each cell is a summation of the different current components from the different junctions. It is clear from Figure 1 that the four different cells are connected in parallel, so the total current from the whole cell is a summation of the currents from each cell. To get an expression for the current in each cell, we have to solve the carriers continuity equation for each cell with suitable boundary conditions [2, 6, 7, 14]. It was solved for planar junctions [2] but for the vertical junction, the continuity equations [7, 8] are:

$$D_n \nabla^2 n(x) - \frac{n(x)}{\tau_n} + N(\lambda)\alpha(\lambda)\exp\left\{-\alpha(\lambda)z\right\} = 0, \quad (1)$$

$$D_p \nabla^2 p(x) - \frac{p(x)}{\tau_p} + N(\lambda)\alpha(\lambda)\exp\left\{-\alpha(\lambda)z\right\} = 0, \quad (2)$$

where $n(x)$ is the electron minority carrier in P-type, $p(x)$ is the hole minority carrier in n-type, D_n is the electron diffusion constant, D_p is the hole diffusion constant, τ_n is the electron lifetime, τ_p is the hole lifetime, $N(\lambda)$ is the spectral transmitted photons number, and $\alpha(\lambda)$ is the silicon absorption coefficient.

The above two equations can be solved by certain boundary conditions to get an expression for the current in the vertical junctions. The short circuit current (I_{sc}) equation [6] is as follows,

$$I_{sc} = (W_1 + W_2) q N_0 \eta_{coll} \eta_A, \qquad (3)$$

where W_1 is the P layer width, W_2 is the n layer width,

$$N_0 = \int_0^{\lambda_0} N(\lambda)\, d(\lambda), \qquad (4)$$

λ_0 equals 1.1 unit for silicon,

$$\eta_{coll} = \frac{W_1 \eta_{c1} + W_2 \eta_{c2}}{W_1 + W_2}, \qquad (5)$$

$$\eta_{c1} = \frac{L_n}{W_1} \tanh \frac{W_1}{L_n}, \qquad (6)$$

$$\eta_{c2} = \frac{L_p}{W_2} \tanh \frac{W_2}{L_p}, \qquad (7)$$

where L_n is the electron diffusion length in P-type, L_p is the hole diffusion length in n-type

$$\eta_A = \frac{1}{N_0} \int_0^{\lambda_0} N(\lambda) \Big[1 - \exp\left(-\alpha(\lambda) h_1\right) \Big] d\lambda, \qquad (8)$$

where h_1 is the depth of the P-layer (in case of cell 1)

The saturation current of the vertical junction is:

$$I_0 = q\, n_i^2\, h_1 \left[\frac{W_1 \eta_{c1}}{N_A \tau_n} + \frac{W_2 \eta_{c2}}{N_D \tau_p} \right], \qquad (9)$$

where n_i is the intrinsic concentration, N_A is the acceptor concentration, N_D is the donor concentration.

Therefore, the current-voltage equation is

$$I = I_{sc} - I_0 \left[\exp\left(\frac{q(v - IR_s)}{KT} \right) - 1 \right], \qquad (10)$$

where v is the applied voltage and R_s is the series resistance.

All the required data about the silicon (doping, resistivity, lifetime, ...) was taken from [1, 7, 15]. In addition, the surface area is 1 cm^2, the cell breadth is taken as 1 cm and the front surface recombination velocity is 10^4 cm/sec. In this work, we study the cell performance at two values for the first cell thickness (h_{11}) which are 3.5 μm and 7.5 μm. The value of the series resistance is estimated for the case of planar junctions and is calculated for the case of vertical junctions from the circuit diagram shown in Figure 2 [16, 17].

3. RESULTS AND DISCUSSION

The whole BESC structure shown schematically in Figure 1 consists of one planar junction and two vertical junctions for each cell. A distributed equivalent circuit model illustrated in Figure 2 is used to describe the complicated junctions' geometry. The circuit diagram is composed of parallel and series branches representing the planar and vertical junctions. Due to the device dimensions, the equivalent circuits are distributed
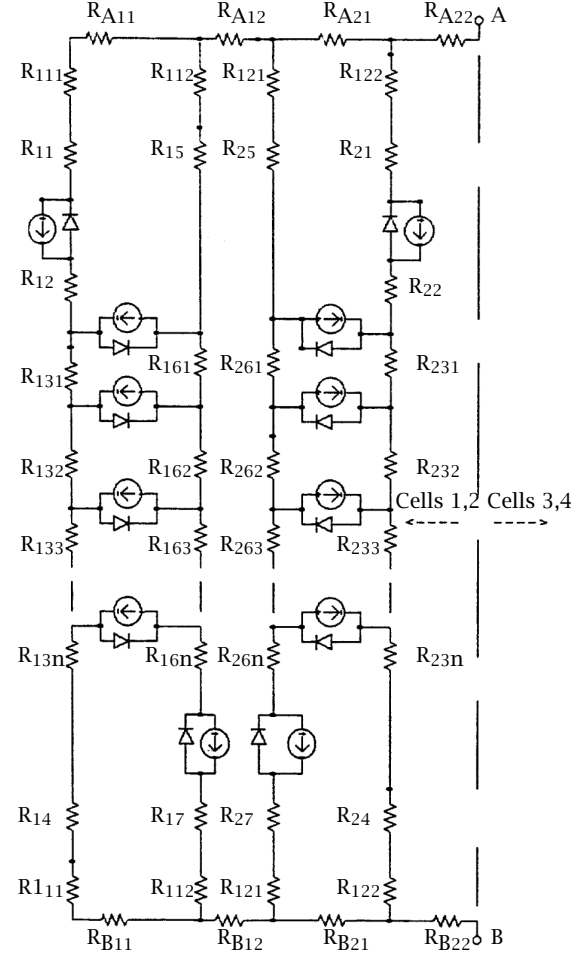

Figure 2. *The equivalent circuit of BESC.*

and lumped for planar and vertical junctions respectively. A distributed resistors for the interface between the metal and the semiconductor (R_I) and metal strip (R_A and R_B) are considered in the circuit.

Table 1 summarize the output currents (I_P and I_V) from planar and vertical junctions for each cell at different thickness h_{11}. In both thickness values, I_P decreases moving from cell 1 to cell 4 due to the reduction in the carriers generation. The same behavior for I_V has been obtained except cell 2 at h_{11} of 3.5 μm. In case of h_{11} of 3.5 μm, although cell 1 has a higher generation rate and lower thickness compared to cell 2, the I_V of cell 2 is bigger than the I_V of cell 1 due to its higher collection with the bigger thickness. On the other hand, in case of h_{11} equals 7.5 μm, cell 2 has a lower thickness and generation rate than the corresponding values for cell 2 in case of h_{11} equals 3.5 μm, therefore the current I_V decreases moving from cell1 to cell 2. It is clear, from Table 1, that the ratio (I_V/I_P) for each cell varies from 7% to 15%.

Figure 3 shows the different current-voltage (*I-V*) curves of each cell in case of h_{11} equals 7.5 μm. It is realized from this figure that there is a mismatching between the different cells. The calculated

Table 1. *The values of I_{sc} from planar and vertical junctions for the different cells at the first cell thickness values (h_{11}) of 3.5 and 7.5 μm.*

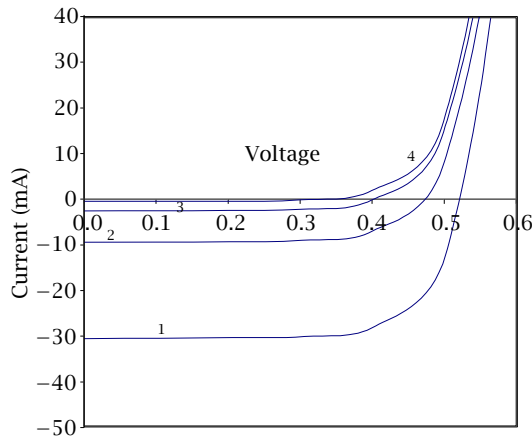| Thickness $h_{11}(\mu m)$	Cell number $I_{Sc}(mA)$	Cell 1	Cell 2	Cell 3	Cell 4
3.5	I_p	20.2	13.81	2.47	0.16
	I_v	1.5	2.1	0.375	0.015
7.5	I_p	28.47	8.5	2.27	0.42
	I_v	1.92	0.84	0.24	0.06

Figure 3. *Current-voltage curves for the four cells (cells 1, 2, 3 and 4) at 7.5 μm for h_{11}.*

series resistance (R_s) of cell 1 and cell 4 is around $0.15\,\Omega$ and for cell 2 and cell 3 is about $0.18\,\Omega$.

Figure 4 presents the *I-V* characteristics for the whole cell (case a and b) taking into consideration planar and vertical junctions. For cell a and b, R_s has a value of $0.41\,\Omega$ and $0.38\,\Omega$ respectively. The difference between the two resistance values can be considered as a result of changing of the mismatching factor due to the changing of h_{11} from 3.5 μm to 7.5 μm. In addition, the efficiency values are 13.83% and 14.81% for cell a and cell b.
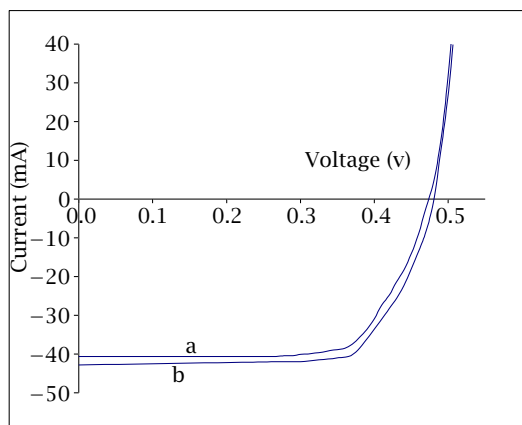

Figure 4. *Current-voltage curves for the whole cell at two cases: (a) h_{11} = 3.5 μm, (b) h_{11} =7.5 μm.*

For h_{11} of 3.5 μm, the published short circuit current (I_{sc}) values for BESC in [1, 2] are 46.91 mA and 36 mA respectively. The reduction in I_{sc} [2] is due to considering the internal loading effect. The calculated value for I_{sc} from our model taking into consideration the effects of both planar and vertical junctions and the series resistance is 40.62 mA. Our calculated efficiency is 13.83% compared to an efficiency of 12.43% in case of considering the whole cell as planar junction only as mentioned in [2]. Therefore, an increase of 10% in the theoretical efficiency could be gained.

4. CONCLUSION

A new theoretical model for the performance of the BESC taking into consideration the effects of the planar and vertical cell's junctions and series resistance is proposed. A realistic distributed equivalent circuit for the whole cell is presented in this work. The calculated results are compared with the previous published data. There is an increase in the efficiency by about 10% due to the effects of vertical junction on the cell's characteristics and the series resistance.

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