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Research Article

A Wide-Band High-Resolution Transmitter for Optical Isolation Amplifier

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A wide-band and high-resolution transmitter of optical isolation amplifier is proposed for switching power supply isolation and servo motor drive applications. The transmitter is based on the chopper-stabilized technique and sigma delta modulator. A built-in common-mode voltage circuit of switched capacitor is proposed to ensure the stability of input DC common mode. Meanwhile, the feedback capacitor is used to improve the driving ability, which helps to avoid a buffer with large input swing. The circuit is tapeout with GF CMOS 0.18 μm 1P6M process with 5 V power supply. The test results show that in 5 V supply voltage, the input swing of transmitter is 2 V and the effective signal bandwidth is 110 kHz. And the output resolution achieves 11 bit.

1. Introduction

As a branch of integrated circuits, photoelectric coupling technology is widely used in signal transmission, industrial control, and other fields. Especially in the application of servo motor drive, current induction of frequency converter, and feedback isolation of switching power supply, the frequency and amplitude of input signal vary widely. It is necessary to cut off the physical connection between transmitter and receiver and complete the process of "electro-optic-electric" conversion by photoelectric coupling, so as to ensure the high-resolution transmission of signals. At the same time, the damage to the backstage circuit will be also avoided. Therefore, the optical isolation amplifier has become the most important core circuit in the photoelectric coupling module [1–4].

Traditional optical isolation amplifier is based on transimpedance amplifier. The coupling signal is analog signal, which is still seriously disturbed by circuit and environmental noise [5–7]. Recently, the sigma delta modulator and the digital-to-analog converter (DAC) are adopted for the transmitter and the receiver, respectively. And, this trend has gradually become the mainstream development direction of the optical isolation amplifier.

But this kind of transmitter also faces the following problems. Firstly, in order to ensure the high-resolution output of the sigma delta modulator, the input common-mode voltage of the modulator must be stabilized. Since the range of input signal amplitude is uncertain, the internal common-mode voltage generator should be constructed, which can add the preset DC common mode to the input signal to ensure the operating point of the modulator. Secondly, when the structure of the sigma delta modulator is adopted, the input signal needs to drive the sampling capacitor of the first integrator. Generally, the driving ability of input signal is weak, which leads to the signal setup of integrator for a long time and reduces the circuit bandwidth to a certain extent. The traditional buffer based on feedback operational amplifier can effectively increase the current driving ability of input signal, but because the input signal amplitude has a large range of changes, it is necessary to design a large input swing transconductance amplifier, which not only increases its complexity but also increases the power consumption. Thirdly, the input signal frequency is

usually in the order of kHz, which is very vulnerable to the influence of low-frequency noise of the circuit and reduces the quality of output signal. So techniques such as correlation double sampling and chopper stabilization must be introduced to suppress low-frequency noise.

In view of the above design difficulties, this paper proposes a wide-band, high-resolution transmitter circuit. The core of circuit is based on the second-order feedback sigma delta modulator with double chopper-stabilized technique, which effectively reduces the impact of flicker noise. Meanwhile, a built-in common-mode voltage circuit of switched capacitor is proposed to add a preset DC common-mode voltage to input signal, which ensures the stability of input common mode of the sigma delta modulator. Furthermore, feedback capacitor retention technology is used to avoid using a buffer of large input swing, whose structure is also optimized while enhancing the driving ability of input signal.

2. Circuit Design

The transmitter diagram of optical isolation amplifier proposed in this paper is shown in Figure 1, which mainly includes a built-in common-mode voltage generator, a non-overlap clock generator, a buffer, a bias circuit, and a double chopper-stabilized second-order sigma delta modulator. Since the input may be a single-frequency sine wave or step signal and there is no definite DC common-mode voltage, before Vin enters the sigma delta modulator, the built-in common-mode voltage Vcm_bin, the input signal Vin_vcm carried by Vcm_bin, and the buffer output Vin_2 are generated by the built-in common-mode voltage generator. Vin2 is exactly the same as the input signal Vin. Its purpose is to form a buffer circuit with large input swing through feedback capacitor C1 and OPA. Non-overlap clock generator generates two-phase non-overlapping clocks (clk1 and clk2) and their reverse signals (clk1a and clk2a) for controlling chopper in buffer. The bias circuit consists of two modules: a chopper bandgap reference and a low dropout regulator (LDO), which output a common-mode voltage (Vcm) and a reference voltage (Vref) of the sigma delta modulator. Because of the need to drive sampling and feedback capacitors, the bandgap and LDO output are input to the sigma delta modulator after buffers. The double chopper-stabilized second-order feedback sigma delta modulator is the core part of the overall transmitter. In order to meet the design requirements of 11 bit resolution and 110 kHz bandwidth, the sigma delta modulator uses 64 times oversampling rate (clock frequency is about 14 MHz), and chopper-stabilized technique is introduced in both the input and the first integrator to suppress the flicker noise in low-frequency band of the circuit. At the same time, the second-order feedback structure has absolute stability, which ensures that the circuit can achieve high-quality output in a wide range of temperature and process corner.

2.1. Built-In Common-Mode Voltage Generator. The built-in common-mode voltage generator is demonstrated in Figure 2.

In circuit, the NMOS transistor MN1-MN8 and the PMOS transistor MP1-MP7 constitute the cascode current mirror structure. In the current source branch of R2/C2, a 1 V built-in common-mode voltage Vin_bin is output by dividing the resistance of R2 and MP5/MP7. C2 is used as charging capacitor to stabilize DC common mode. Meanwhile, Vin is input the circuit through a buffer consisting of a two-stage Miller-compensation operational amplifier. When clk1 is high and clk2 is low, four switches on the left side of capacitor C3 are on and four switches on the right side are off (two switches are connected in parallel because the conduction resistance can be reduced; on the other hand, the effect of channel charge injection is also alleviated), and Vin charges the bottom plate of C3. Because the parameters of transistors, resistors, and capacitors in current source branch MP4/MP6/R1/C1 and MP5/MP7/R2/C2 are identical, the current flowing through them is the same. The node X of buffer output is approximately DC grounding, so the voltage of node Y is equal to the built-in common-mode voltage Vin_bin. Therefore, it means Vin_bin charges the upper plate of C3. While clk1 is low and clk2 is high, four switches on the left side of capacitor C3 are off and four switches on the right side are on. So, the voltage of C3 upper plate equals the sum of the voltage of upper and bottom plate when clk1 is high. That is, Vin_vcm = Vin_bin + Vin. The built-in common-mode voltage is loaded into Vin by means of two-phase clock switched-capacitor control. And Vin2 is connected to the bottom plate of C3 and continuously outputs Vin.

2.2. Buffer Circuit. Because the amplitude of input signal varies widely and there is no definite DC common-mode voltage, in order to avoid using a buffer with large input swing, a simple and feasible circuit is designed by using the capacitor retention characteristic. As shown in Figure 1, the principle is as follows: the differential input VP and VN of buffer are actually input signals Vin. The buffer acts as a differential amplifier and the two input terminals are identical, so the signal passing through buffer to the output VO is approximately zero. At this time, capacitor C1 plays an important role, and Vin2 continues to charge the left plate of C1, while Vin_vcm charges the right plate. The voltage difference on the capacitor is Vcm_bin, which is equivalent to maintaining the built-in common-mode voltage. From another point of view, when the charge is completed, the voltage difference on C1 is Vcm_bin, the left plate is Vin_2, and the right plate can always be maintained at Vin_2 + Vcm_bin, which is equal to the signal Vin_vcm that is input to the sigma delta modulator. Originally, Vin_vcm has no driving capability, so it cannot drive the sampling capacitor of the sigma delta modulator. But on account of C1 charge retaining, it actually enhances the driving ability of Vin_vcm.

Therefore, the charge-retaining circuit designed in this paper eliminates the influence of uncertain common-mode voltage of input Vin. OPA makes VP and VN equal by virtue of virtual short and break and uses the ability of feedback capacitor C1 to keep charge to increase driving ability, thus

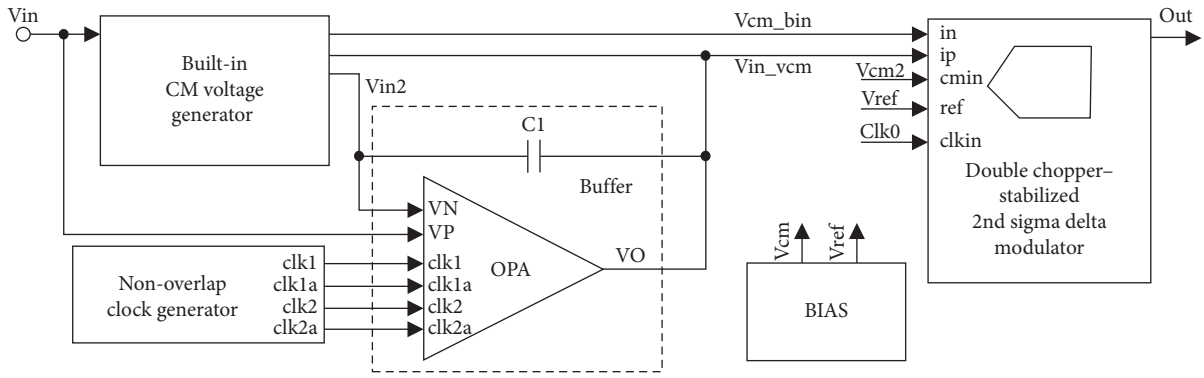

Figure 1: Transmitter diagram of optical isolation amplifier.

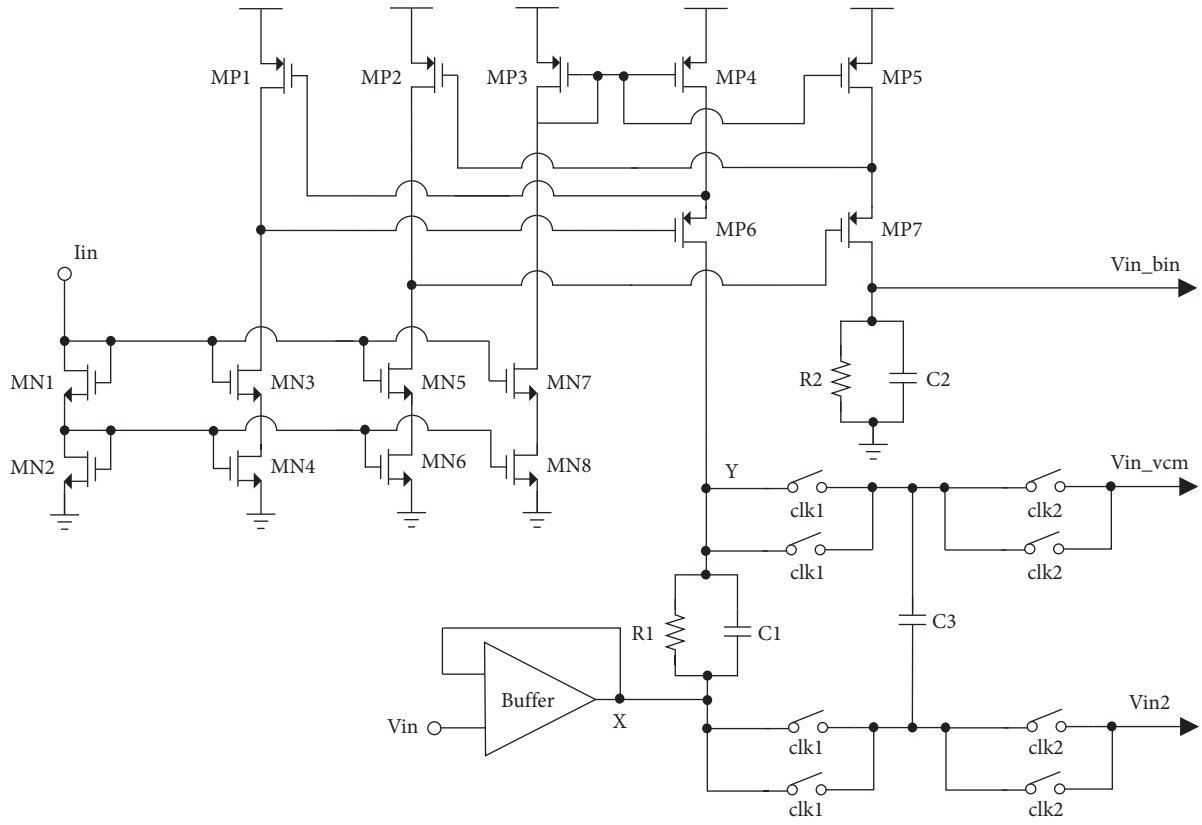

Figure 2: Built-in common-mode voltage generator.

maintaining the input signal Vin_vcm of the sigma delta modulator. The OPA in buffer is a two-stage chopper folded structure combined with the source follower, as shown in Figure 3.

To reduce flick noise and increase input swing, the input chopper S0 is implemented by CMOS switch, and the input signal is modulated to high-frequency band. The NMOS chopper S1 and the PMOS chopper S2 are placed on the low-resistance cascode node of the first-stage current path. Because the voltage swing on the low-resistance node is small, a simple four-transistor NMOS (PMOS) switch is adopted. The chopper S1 modulates the input signal back to the baseband, and at the same time, the OPA input equivalent noise and offset voltage are modulated to the odd harmonics of the chopper frequency. In order to eliminate offset and noise caused by the tail current source MP3/MP4, the chopper S2 is added to the source node of MN3/MN4 to match dynamically, which also further reduces the noise and offset of OPA. The capacitor C2 and C3 are used to stabilize the output voltage of the two nodes.

2.3. Double Chopper-Stabilized 2nd Sigma Delta Modulator. Figure 4 shows the double chopper-stabilized 2nd sigma delta modulator.

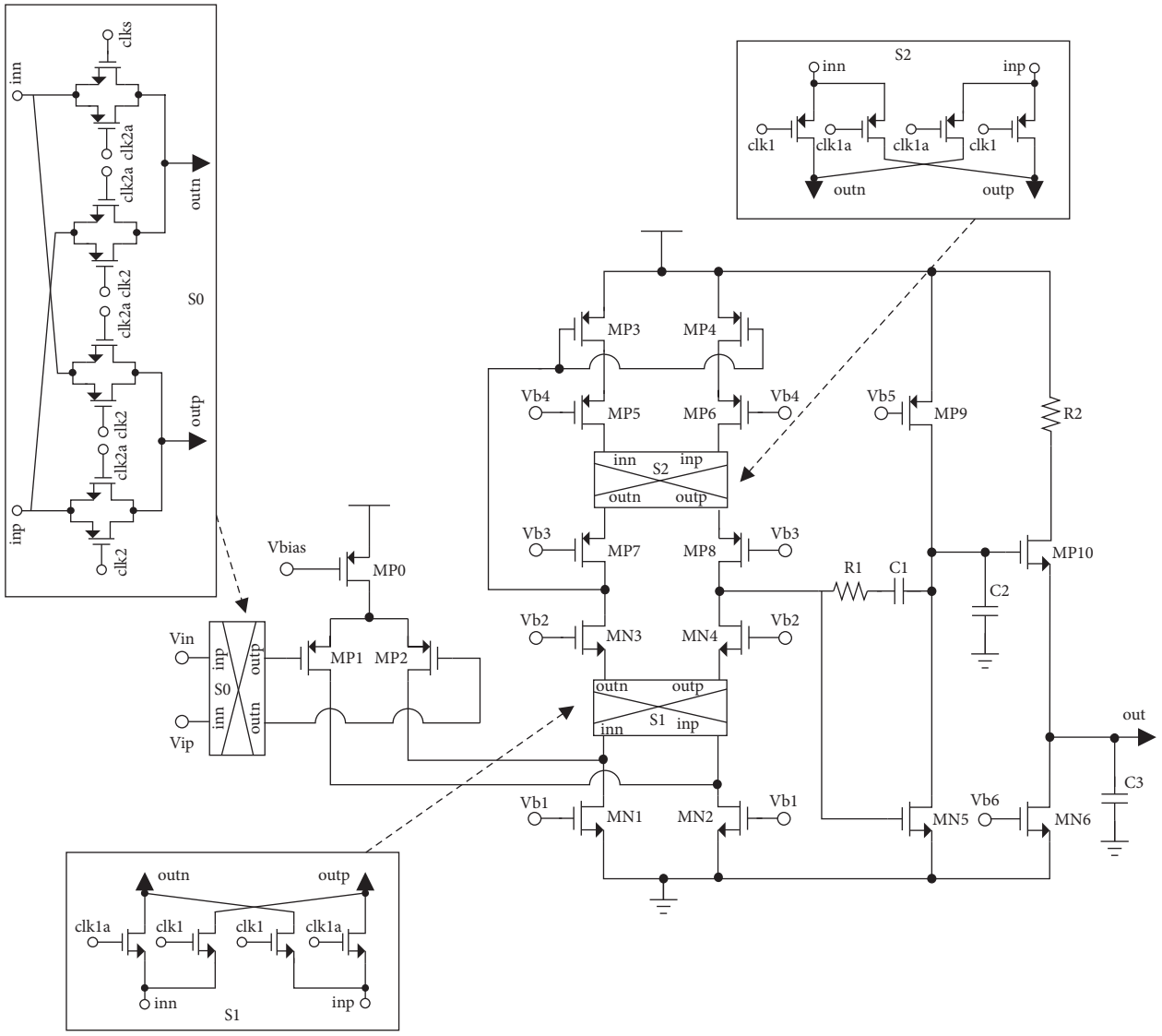

Figure 3: Two-stage chopper folded OPA.

For effectively suppressing low-frequency flick noise, chopper is added to the input end of the sigma delta modulator and the input and output of the first integrator and the feedback capacitor array, respectively. The noise of the sigma delta modulator mainly comes from the first integrator, so there is no need of chopper in the second integrator [8–10]. Since the quantization range of the sigma delta modulator is determined by reference voltage ref and ground potential GND in feedback capacitor array, the low-frequency noise and jitter of these two voltages will also affect the output accuracy. So, the feedback capacitor array also needs chopper. The chopper frequency is set to 1/16 of clock frequency of the sigma delta modulator, which is about 870 kHz. Slower chopper frequency is beneficial to reduce the power consumption, but too slow chopper frequency will reduce the noise suppression performance. Usually, 1/32 or 1/16 is the appropriate choice.

Considering the wide range of input signal amplitude, the gain of the first integrator is set to 0.05 to avoid overload of the second integrator. And the gain is mainly loaded into the second integrator, whose gain is 0.5. The behavioral model of the sigma delta modulator is established as shown in Figure 5. With the addition of nonideal factors such as KTC noise, jitter, OPA noise, limited gain, and slew rate, the output spectrum is shown in Figure 6, and the effective number of bit (ENOB) reaches 11.85 bit when the input frequency is 100 kHz. It demonstrates that a certain margin is needed for circuit design to meet the resolution requirement.

The power supply voltage is 5 V in our design, so the transistors' overdrive voltage has a large variable range. The operation transconductance amplifier (OTA) in integrators is realized by a fully differential single-stage telescope structure, which is conducive to reducing power consumption and noise. Common-mode feedback circuit uses a switched-capacitor structure as shown in Figure 7 to control the additional PMOS tail current source (MP1/MP2).

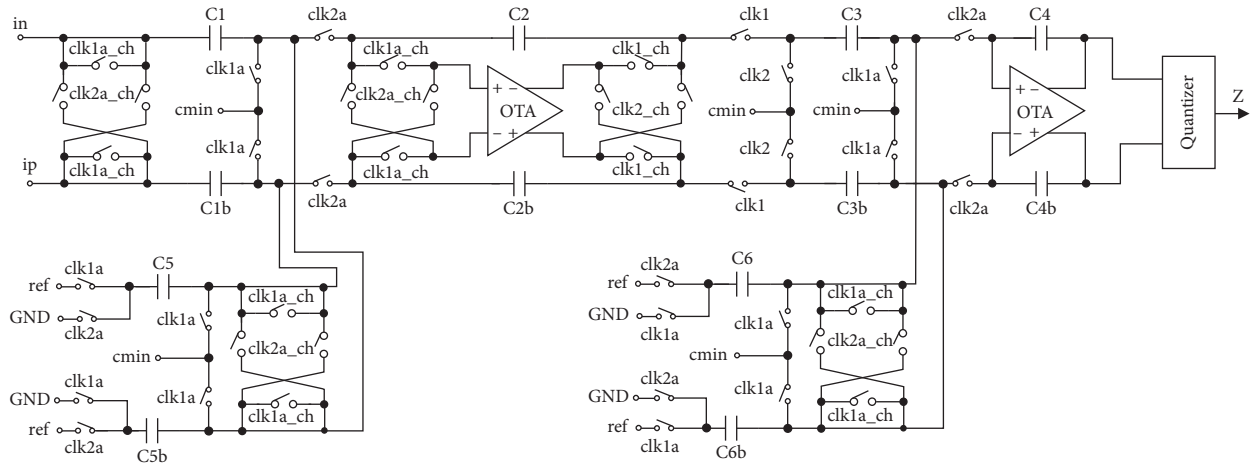

Figure 4: Double chopper-stabilized 2nd sigma delta modulator.

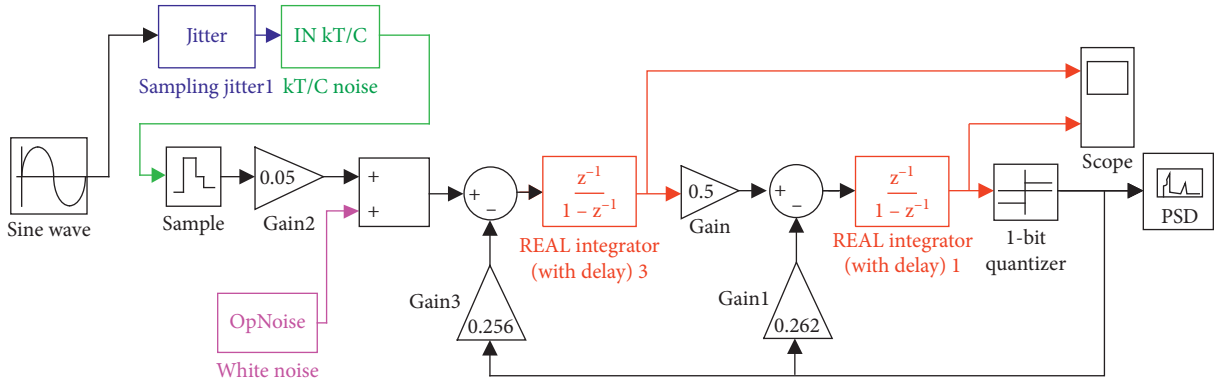

Figure 5: Behavioral model of the sigma delta modulator.

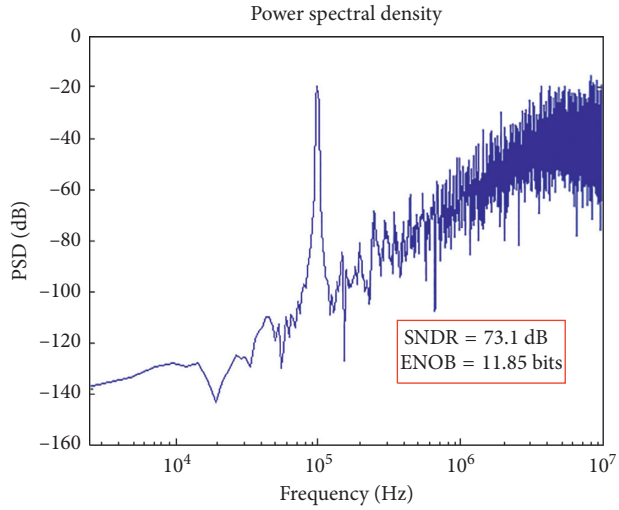

Figure 6: Output spectrum of the sigma delta modulator.

3. Experiment Result

The transmitter is tapeout by GF CMOS 0.18 μm 1P6M process with 5 V power supply voltage. The chip micrograph is shown in Figure 8. The signal is transmitted from top to bottom.

First, the output spectrum of transmitter is tested. When the clock frequency is 14 MHz, the input signal is 80 kHz and 110 kHz, respectively, with the peak-to-peak amplitude of 2 V, and the output spectrum results are shown in Figure 9. The signal-to-noise distortion ratio (SNDR) reaches 68.52 dB and 68.2 dB, respectively, and the corresponding

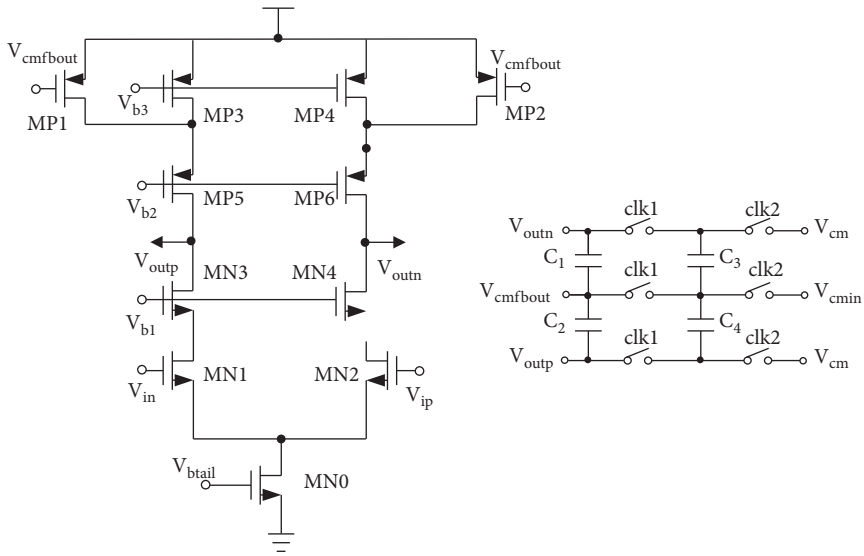

Figure 7: Fully differential single-stage telescope OTA.

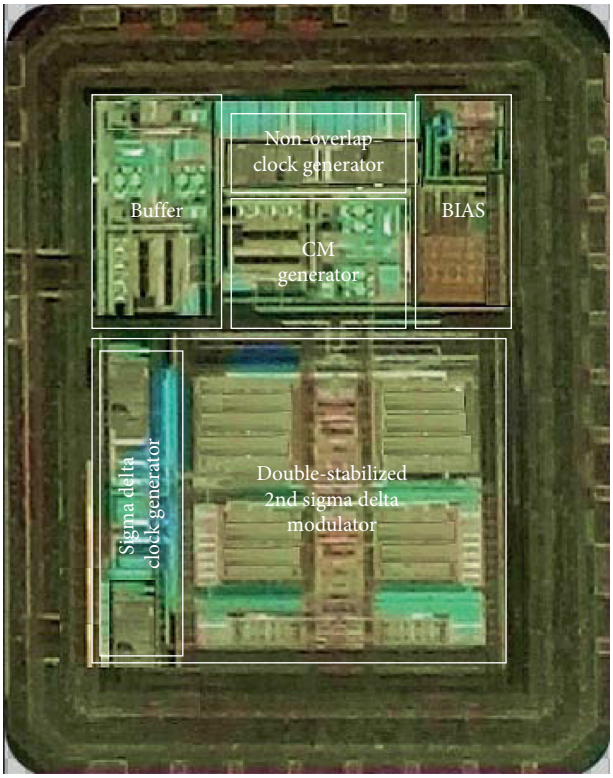

Figure 8: Micrograph of transmitter chip.

ENOB is 11.09 bit and 11.03 bit. When converted to DC nonlinear distortion, it is about 0.05%.

Then, the input swing is tested. While the clock frequency and input signal frequency are fixed, and the input signal amplitude is gradually increased. When the input amplitude increases to 2.2 V, as shown in Figure 10, SNDR begins to decrease, so the input swing of the transmitter is about 2 V.

Temperature characteristic is an important parameter of optical isolation amplifier. The ENOB of each temperature point is tested. The results are indicated in Figure 11. It can be seen that the output signal maintains above 10.6 bit in a wide temperature range.

Table 1 lists the performance comparison between our design and previous papers and products. The transmitter in this paper in terms of bandwidth, effective resolution, and

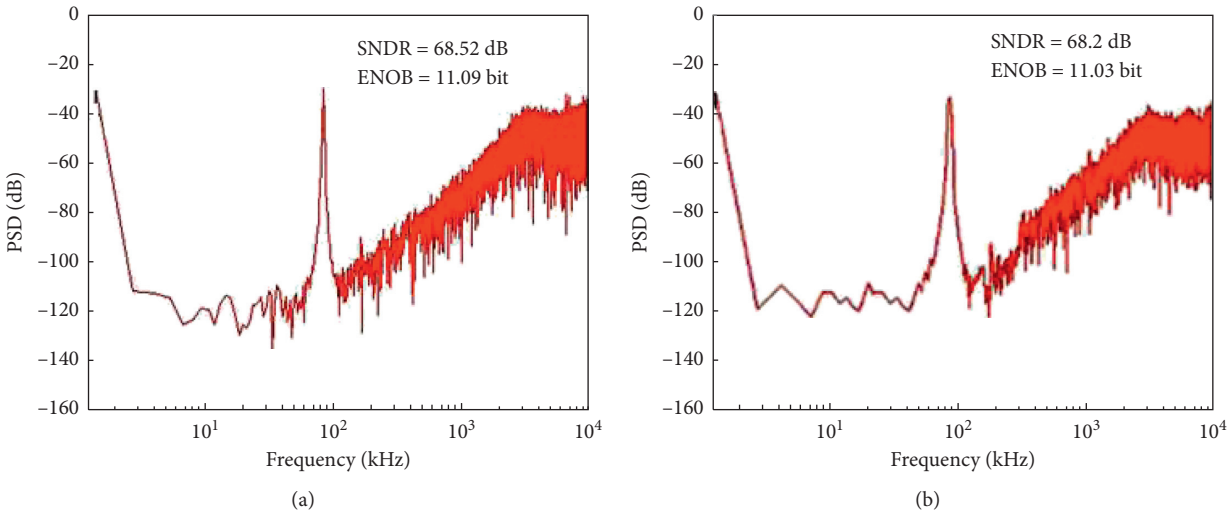

Figure 9: Output spectrum results: (a) input frequency is 80 kHz; (b) input frequency is 110 kHz.

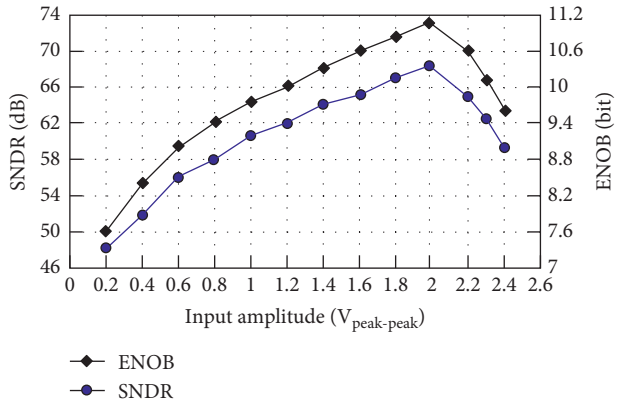

Figure 10: Output SNDR vs. input amplitude.

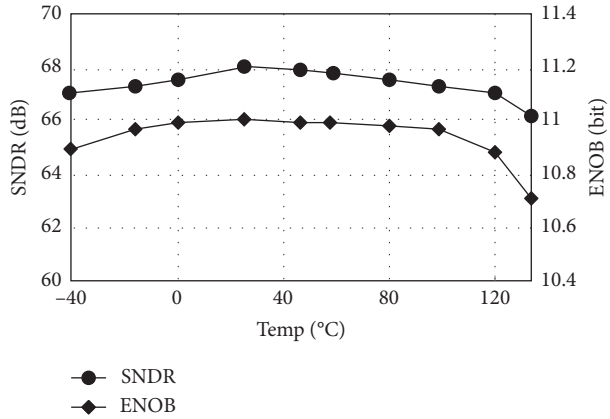

Figure 11: ENOB vs. temperature.

Table 1: Performance comparison.

Ref	Process (nm)	Supply voltage (V)	Bandwidth (kHz)	Input resistance (MΩ)	ADC structure	ENOB (bit)	Nonlinearity (%)
[11]	CMOS 350	3.3	70	337	—	—	—
[12]	CMOS 500	5	100	1000	Sigma delta	10	0.1
[13]	CMOS 500	5	230	0.078	Sigma delta	11	0.04
This paper	CMOS 180	5	110	1000	Sigma delta	11.09	0.046

nonlinear distortion has greater advantages than the reference paper. Meanwhile, the important parameters are comparable with the existing products, and the overall performance is good.

In order to obtain the spectrum of single-frequency signal, our test first uses AC signal for input. In static simulation, the minimum resolution is about 2 mV, which proves that the design meets the resolution requirement of 11 bit when the small step signal is input.

4. Conclusion

Based on the optical isolation amplifier used in DC-link voltage monitoring, switching power supply isolation, servo motor drive, and other fields, this paper proposes a wide-band, high-resolution transmitter circuit. The core circuit is implemented by a chopper-stabilized sigma delta modulator. Aiming at the problem that the input signal amplitude varies widely and the common-mode signal is uncertain, which affects the output signal quality, a built-in common-mode voltage generator of switched capacitor is proposed to ensure the stability of input DC common mode in the whole circuit. At the same time, the feedback capacitor retaining technology in buffer is used to increase the input driving ability, avoid using the buffer with large input swing, and optimize the circuit structure. The transmitter chip is realized by GF CMOS 0.18 μm 1P6M 5 V power supply voltage process. The experiment results show that when the power supply voltage is 5 V and the clock frequency is 14 MHz, the peak input amplitude reaches 2 V, and the effective signal bandwidth is 110 kHz. In frequency domain, the SNDR of output signal achieves 68.5 dB and ENOB reaches 11 bit. The transmitter designed in this paper has high comparability with the related design in terms of effective resolution, input swing, and nonlinearity, which can meet the application requirements of optical isolation amplifier.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest related to this paper.

Acknowledgments

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